

32-Channel Serial-to-Parallel Converter with Open-Drain Outputs

Features

- 100 mA Minimum Sink Current
- 16 MHz Shift Register Speed
- Polarity and Blanking Inputs
- CMOS-Compatible Inputs

Applications

- Inkjet and Electrostatic Print Heads
- AC-Electroluminescent Displays
- Microelectromechanical Systems (MEMS) Applications

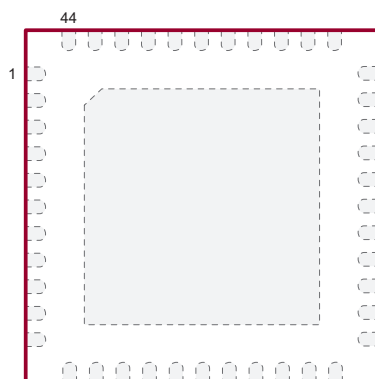
General Description

The HV5524 is a low-voltage serial to high-voltage parallel converter with open-drain outputs. This device is designed as a driver for AC electroluminescent displays. It can also be used in any application requiring multiple-output high-voltage current sinking capabilities, such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent and large matrix LCD displays.

This device consists of a 32-bit Shift register, 32 latches and control logic to perform the polarity selection and blanking of the outputs. Data are shifted through the Shift register on the high-to-low transition of the clock. The HV5524 shifts counter clockwise when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register. Operation of the Shift register is not affected by the $\overline{LE}$ (latch enable), the $\overline{BL}$ (blanking) and the $\overline{POL}$ (polarity) inputs. Transfer of data from the Shift register to the latch occurs when the $\overline{LE}$ input is high. The data in the latch are stored when $\overline{LE}$ is low.

Package Type

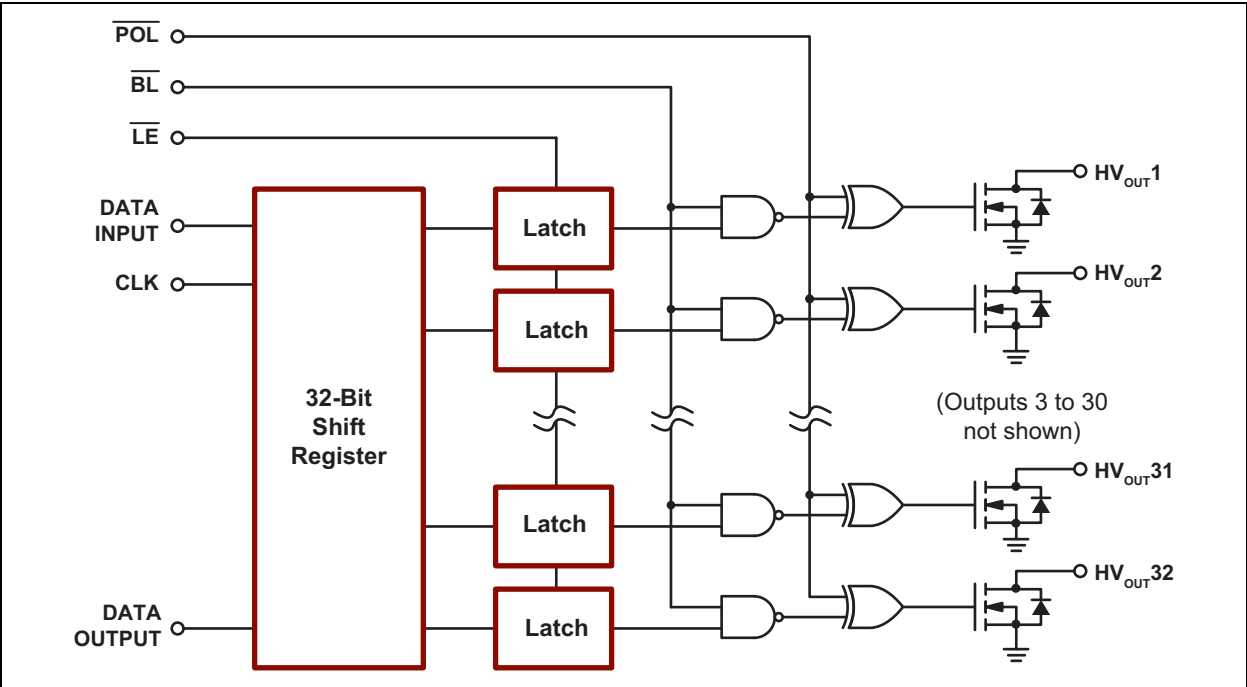
44-Lead WQFN
(Top View)



Note: See [Table 2-1](#) for pin information.

HV5524

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, V_{DD} (Note 1)	-0.5V to +7V
Output Voltage, HV_{OUT} (Note 1)	-0.5V to +230V
Logic Input Levels (Note 1)	-0.5V to $V_{DD} + 0.5V$
Ground Current (Note 2)	1.5A
Maximum Junction Temperature, $T_{J(MAX)}$	+125°C
Storage Temperature, T_S	-65°C to +150°C
Continuous Total Power Dissipation:	
44-lead WQFN (Note 3)	3.4W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Note 1:** All voltages are referenced to V_{SS} .
Note 2: Duty cycle is limited by the total power dissipated in the package.
Note 3: 1 oz. 4-layer 3" x 4" PCB.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	—	5.5	V	
High-Voltage Output	HV_{OUT}	-0.3	—	+220	V	
High-Level Input Voltage	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.2 V_{DD}	V	
Clock Frequency	f_{CLK}	—	—	16	MHz	
Operating Ambient Temperature	T_A	-40	—	+85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Supply Current	I_{DD}	—	—	25	mA	$f_{CLK} = 16$ MHz, $f_{DATA} = 8$ MHz
Quiescent V_{DD} Supply Current	I_{DDQ}	—	—	100	μA	$D_{IN} = 0V$, all input logic pins = 0V, all outputs off
OFF State Output Current	$I_{O(OFF)}$	—	—	10	μA	All outputs high, all switches parallel
High-Level Logic Input Current	I_{IH}	—	—	1	μA	$V_{IH} = V_{DD}$
Low-Level Logic Input Current	I_{IL}	—	—	-1	μA	$V_{IL} = 0V$
High-Level Output Data Out	V_{OH}	$V_{DD} - 1V$	—	—	V	$ID_{OUT} = -10$ mA
Low-Level Output Voltage	HV_{OUT}	V_{OL}	—	15	V	$I_{HV_{OUT}} = +100$ mA
	Data Out		—	1	V	$ID_{OUT} = +10$ mA
HV_{OUT} Clamp Voltage	V_{OC}	—	—	-1.5	V	$I_{OL} = -100$ mA

AC ELECTRICAL CHARACTERISTICS

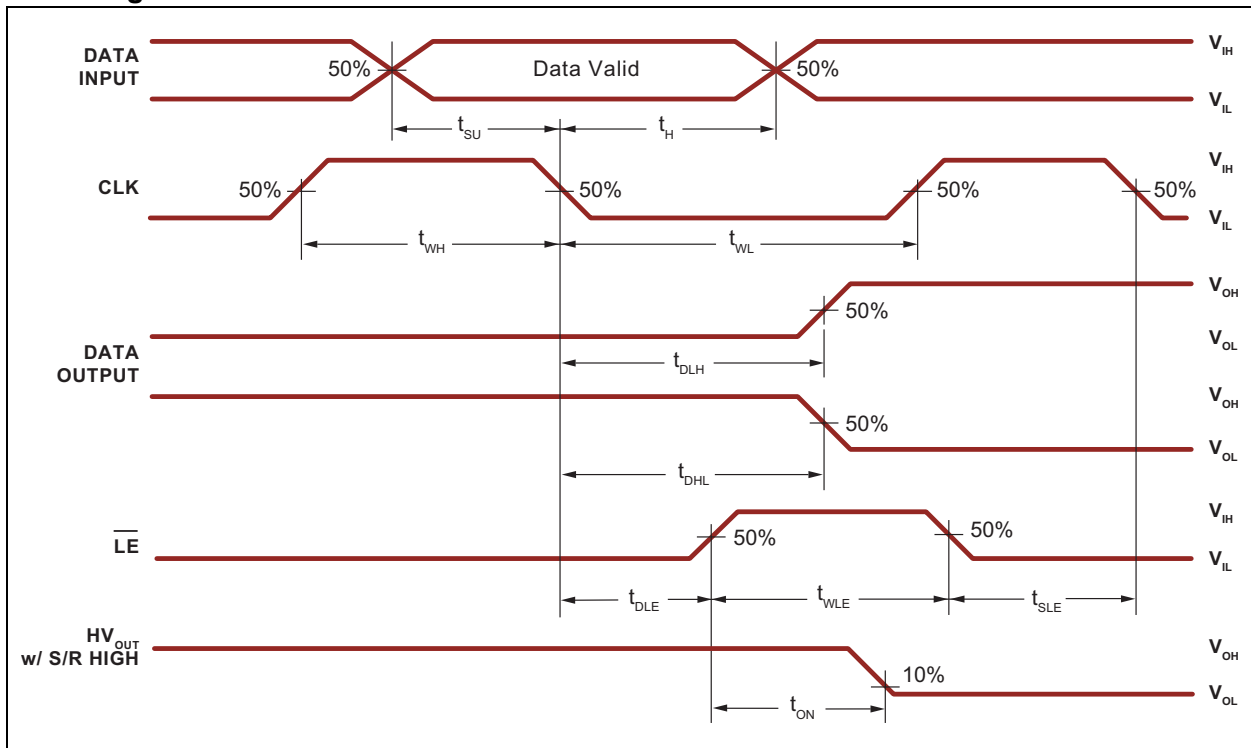
Electrical Specifications: $V_{DD} = 5V$, $T_J = +25^{\circ}C$						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	f_{CLK}	—	—	16	MHz	
Clock Pulse Width, High or Low	t_{WL}, t_{WH}	31	—	—	ns	
Data Setup Time Before CLK Falls	t_{SU}	25	—	—	ns	
Data Hold Time after CLK Falls	t_H	10	—	—	ns	
Turn-On Time, HV_{OUT} from Enable	t_{ON}	—	—	400	ns	$R_L = 2\text{ k}\Omega$ to V_{PP} maximum
Delay Time Clock to Data High to Low	t_{DHL}	—	—	35	ns	$C_L = 15\text{ pF}$
Delay Time Clock to Data Low to High	t_{DLH}	—	—	35	ns	$C_L = 15\text{ pF}$
Delay Time Clock to $\overline{LE}$ Low to High	t_{DLE}	20	—	—	ns	
Width of $\overline{LE}$ Pulse	t_{WLE}	20	—	—	ns	
$\overline{LE}$ Setup Time Before CLK Falls	t_{SLE}	20	—	—	ns	
Digital Logic Input Capacitance	C_{IN}	—	—	15	pF	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Temperature Ranges						
Operating Ambient Temperature	T_A	-40	—	+85	$^{\circ}C$	
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	$^{\circ}C$	
Storage Temperature	T_S	-65	—	+150	$^{\circ}C$	
Package Thermal Resistance						
44-lead WQFN	θ_{JA}	—	19	—	$^{\circ}C/W$	Note 1

Note 1: 1 oz. 4-layer 3" x 4" PCB.

Switching Waveforms



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).
Refer to [Package Type](#) for the location of the pins.

TABLE 2-1: 44-LEAD WQFN PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HV _{OUT} 11	High-voltage output
2	HV _{OUT} 12	High-voltage output
3	HV _{OUT} 13	High-voltage output
4	HV _{OUT} 14	High-voltage output
5	HV _{OUT} 15	High-voltage output
6	HV _{OUT} 16	High-voltage output
7	HV _{OUT} 17	High-voltage output
8	HV _{OUT} 18	High-voltage output
9	HV _{OUT} 19	High-voltage output
10	HV _{OUT} 20	High-voltage output
11	HV _{OUT} 21	High-voltage output
12	HV _{OUT} 22	High-voltage output
13	HV _{OUT} 23	High-voltage output
14	HV _{OUT} 24	High-voltage output
15	HV _{OUT} 25	High-voltage output
16	HV _{OUT} 26	High-voltage output
17	HV _{OUT} 27	High-voltage output
18	HV _{OUT} 28	High-voltage output
19	HV _{OUT} 29	High-voltage output
20	HV _{OUT} 30	High-voltage output
21	HV _{OUT} 31	High-voltage output
22	HV _{OUT} 32	High-voltage output
23	DATA OUT	Data output pin
24	NC	No internal connection
25	NC	No internal connection
26	NC	No internal connection
27	$\overline{\text{POL}}$	Inverts the polarity of the HV _{OUT} pins.
28	CLK	Clock pin. The Shift registers shift data on the falling edge of the input clock.
29	V _{SS}	Reference voltage, usually ground
30	V _{DD}	Logic supply voltage
31	$\overline{\text{LE}}$	Latch enable pin. Data are shifted from the Shift register to the latches on logic input high.
32	DATA IN	Data input pin
33	$\overline{\text{BL}}$	Blanking pin sets all HV _{OUT} pins ON or OFF, depending upon the state of polarity. See Table 3-2 .
34	NC	No internal connection
35	HV _{OUT} 1	High-voltage output
36	HV _{OUT} 2	High-voltage output

TABLE 2-1: 44-LEAD WQFN PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
37	HV _{OUT3}	High-voltage output
38	HV _{OUT4}	High-voltage output
39	HV _{OUT5}	High-voltage output
40	HV _{OUT6}	High-voltage output
41	HV _{OUT7}	High-voltage output
42	HV _{OUT8}	High-voltage output
43	HV _{OUT9}	High-voltage output
44	HV _{OUT10}	High-voltage output
Center Tab		Connect to V _{SS} .

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV5524.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-Up		Power-Down	
Step	Description	Step	Description
1	Connect ground.	1	Remove all inputs.
2	Apply V _{DD} .	2	Remove V _{DD} .
3	Set all inputs to a known state.	3	Disconnect ground.

TABLE 3-2: FUNCTION TABLE

Function	Inputs ⁽¹⁾					Outputs				
						Shift Register		High-Voltage Output		Data Out
	Data	CLK	$\overline{\text{LE}}$	$\overline{\text{BL}}$	$\overline{\text{POL}}$	1	2...32	1	2...32	
All On	X	X	X	L	L	Note 2	Note 2	On	On	Note 2
All Off	X	X	X	L	H	Note 2	Note 2	Off	Off	Note 2
Invert Mode	X	X	L	H	L	Note 2	Note 2	<u>Note 2</u>	<u>Note 2</u>	Note 2
Load S/R	H or L	↓	L	H	H	H or L	Note 2	Note 2	Note 2	Note 2
Load Latches	X	H or L	↑	H	H	Note 2	Note 2	Note 2	Note 2	Note 2
	X	H or L	↑	H	L	Note 2	Note 2	<u>Note 2</u>	<u>Note 2</u>	Note 2
Transparent Latch Mode	L	↓	H	H	H	L	Note 2	Off	Note 2	Note 2
	H	↓	H	H	H	H	Note 2	On	Note 2	Note 2

Note 1: H = High logic level
L = Low logic level
X = Don't care
↓ = High-to-low transition
↑ = Low-to-high transition

2: Dependent on the previous stage's state before the last CLK ↓ or last $\overline{\text{LE}}$ high.

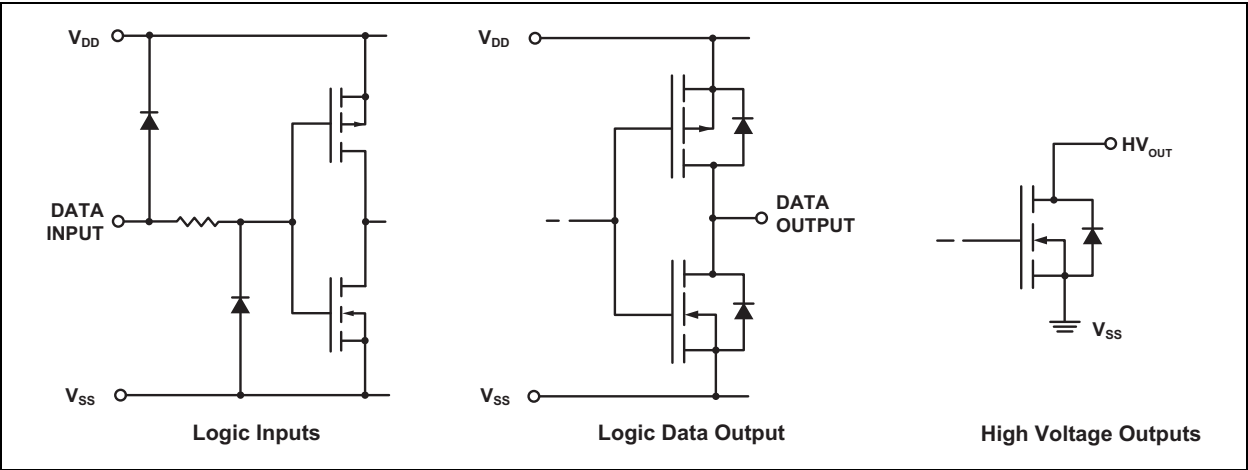
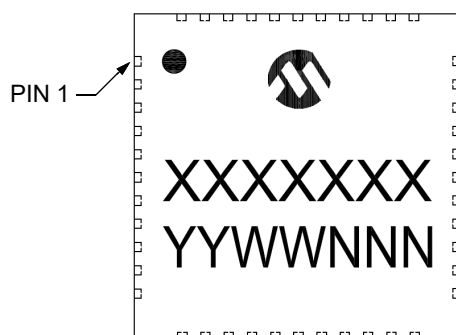


FIGURE 3-1: Input and Output Equivalent Circuits.

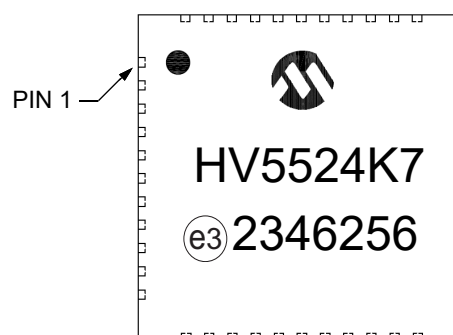
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

44-lead WQFN



Example

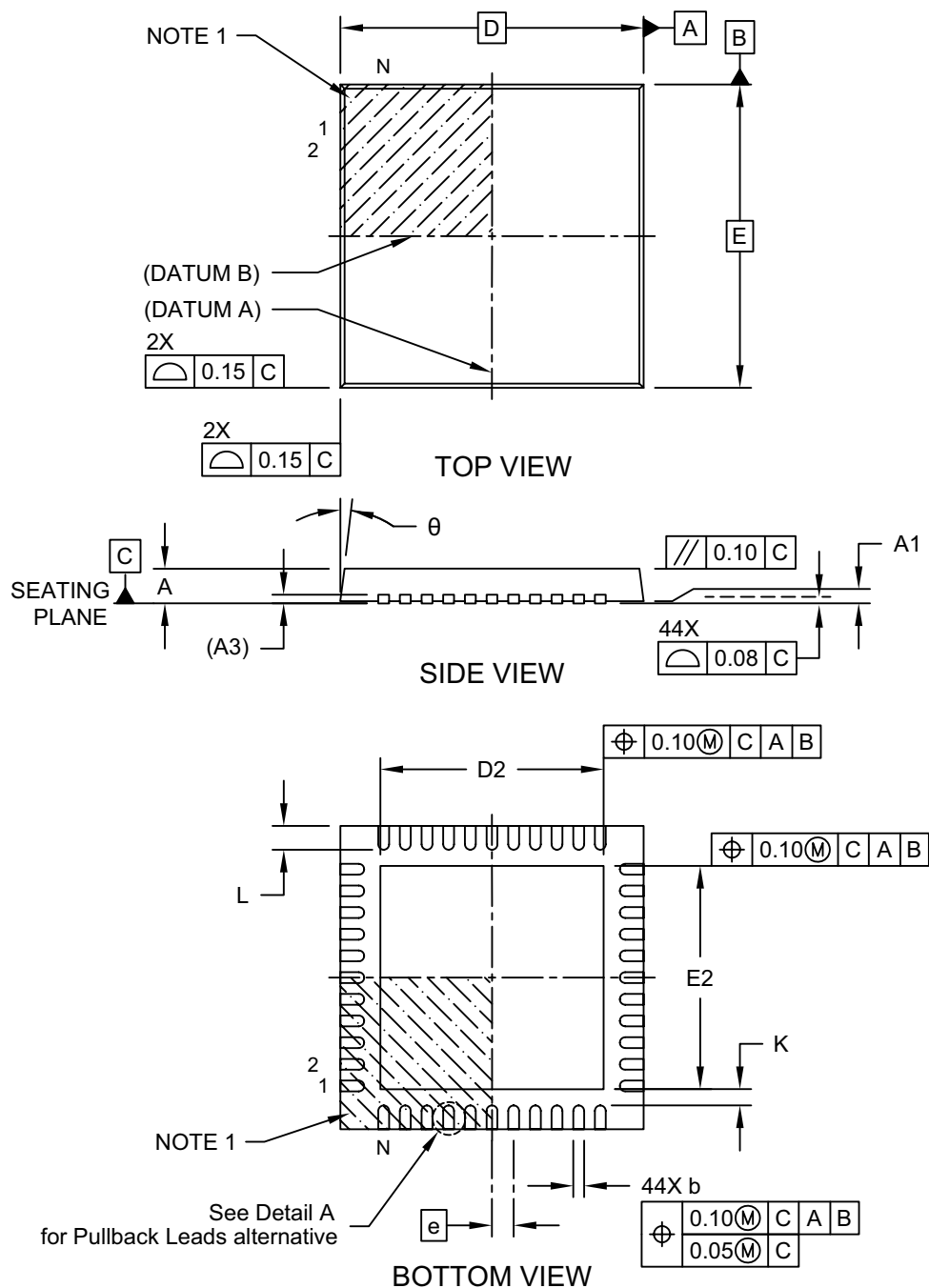


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC [®] designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or may not include the corporate logo.

44-Lead Very, Very Thin Plastic Quad Flat, No Lead Package (7P) - 7x7 mm Body [WQFN]; Supertex Legacy Package

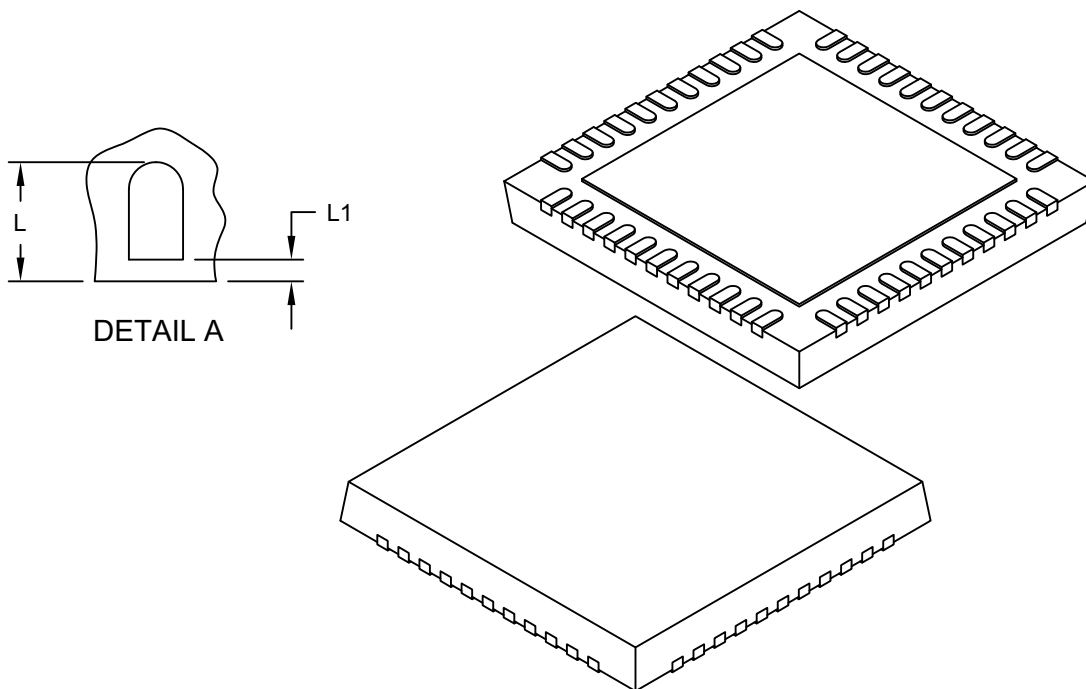
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-307A Sheet 1 of 2

44-Lead Very, Very Thin Plastic Quad Flat, No Lead Package (7P) - 7x7 mm Body [WQFN]; Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	44		
Pitch	e	0.50 BSC		
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	7.00 BSC		
Exposed Pad Length	D2	5.00	5.15	5.25
Overall Width	E	7.00 BSC		
Exposed Pad Width	E2	5.00	5.15	5.25
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.45	0.55	0.65
Pullback	L1	-	-	0.15
Mold Angle	θ	0°	7°	14°
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

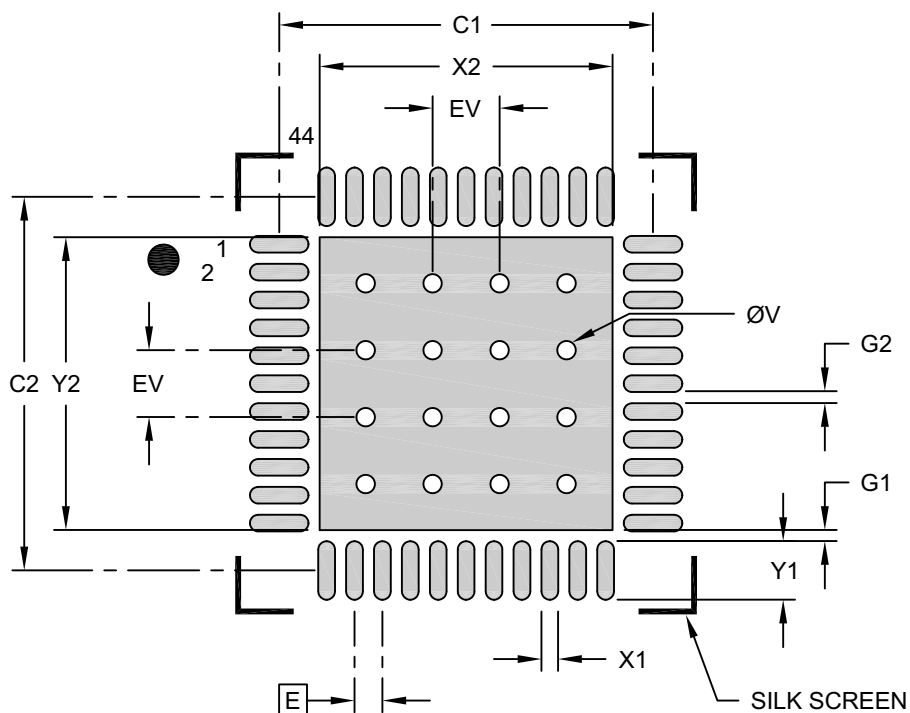
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-307A Sheet 2 of 2

44-Lead Very, Very Thin Plastic Quad Flat, No Lead Package (7P) - 7x7 mm Body [WQFN]; Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			5.25
Optional Center Pad Length	Y2			5.25
Contact Pad Spacing	C1		6.70	
Contact Pad Spacing	C2		6.70	
Contact Pad Width (X44)	X1			0.30
Contact Pad Length (X44)	Y1			1.05
Contact Pad to Center Pad (X44)	G1	0.20		
Contact Pad to Contact Pad (X44)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2307A

APPENDIX A: REVISION HISTORY

Revision A (December 2023)

- Original release of this document.

PRODUCT IDENTIFICATION SYSTEM

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<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	<u>X</u>
Device	Package Option		Environmental	Media Type
Device:	HV5524	=	32-Channel Serial-to-Parallel Converter with Open-Drain Outputs	
Package Option:	K7	=	44-lead (7 x 7 mm) WQFN	
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package	
Media Type:	(blank)	=	260/Tray for a K7 Package	

Example:

a) HV5524K7-G: 32-Channel Serial-to-Parallel Converter with Open-Drain Outputs, 44-lead (7 x 7 mm) WQFN, 260/Tray

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