

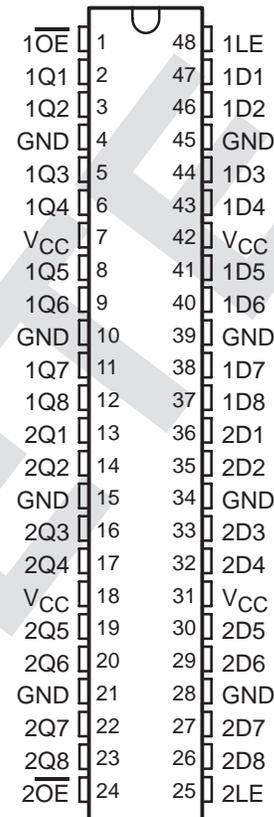
# SN74ALVC16373

## 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS257B – JANUARY 1993 – REVISED JULY 1995

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE  
(TOP VIEW)



### description

This 16-bit transparent D-type latch is designed for 3.3-V  $V_{CC}$  operation; it is tested at 2.5-V, 2.7-V, and 3.3-V  $V_{CC}$ .

The SN74ALVC16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high- or low-logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16373 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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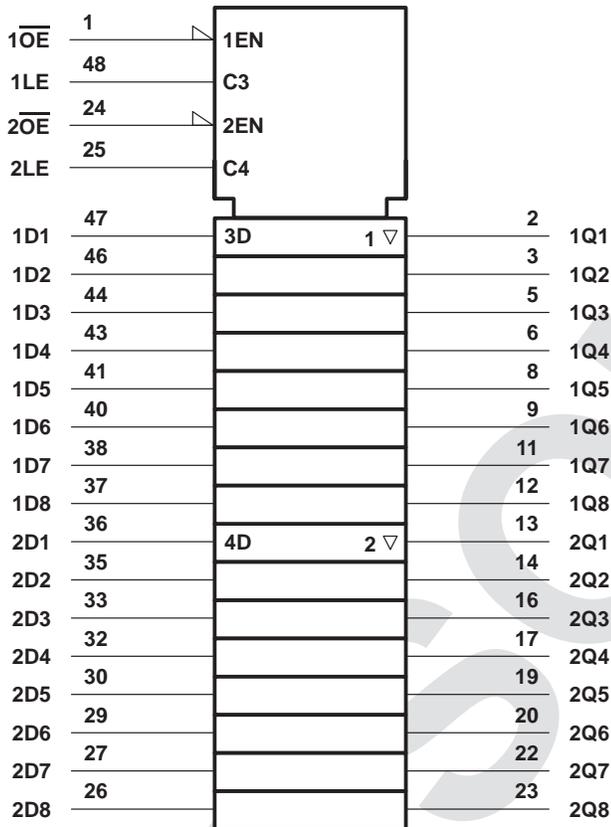
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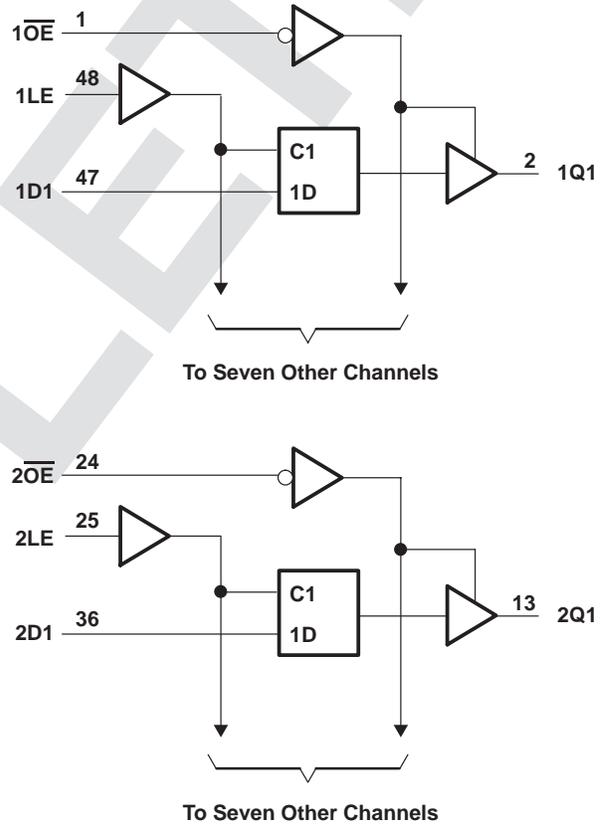
FUNCTION TABLE  
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

### logic symbol†



### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package .....	0.85 W
DL package .....	1.2 W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7	V
		$V_{CC} = 2.7$ V to 3.6 V	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	0.8	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.3$ V	–12	mA
		$V_{CC} = 2.7$ V	–12	
		$V_{CC} = 3$ V	–24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.3$ V	12	mA
		$V_{CC} = 2.7$ V	12	
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> †	T <sub>A</sub> = -40°C to 85°C			UNIT
			MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -6 mA	V <sub>IH</sub> = 1.7 V	2.3 V	2		
	I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7		
		V <sub>IH</sub> = 2 V	2.7 V	2.2		
	I <sub>OH</sub> = -24 mA	V <sub>IH</sub> = 2 V	3 V	2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	MIN to MAX	0.2			V
	I <sub>OL</sub> = 6 mA	V <sub>IL</sub> = 0.7 mA	2.3 V	0.4		
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 mA	2.3 V	0.7		
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.8 mA	2.7 V	0.4		
	I <sub>OL</sub> = 24 mA	V <sub>IL</sub> = 0.8 mA	3 V	0.55		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5			μA
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.7 V	2.3 V	45			μA
	V <sub>I</sub> = 1.7 V	3 V	-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V	3 V	-75			
	V <sub>I</sub> = 0 to 3.6 V	3.6 V	±500			
I <sub>OZ</sub> ‡	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	40			μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	750			μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3		pF
	Inputs			6		
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7		pF	

† For conditions shown as MIN or MAX use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE↓	1		1		1.1		ns
t <sub>h</sub>	Hold time, data after LE↓	1.5		1.7		1.4		ns



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	1	5.1	4.3	1.1	3.6	ns	
	LE	Q	1	5.5	4.6	1	3.9		
t <sub>en</sub>	$\overline{\text{OE}}$	Q	1	6.5	5.7	1	4.7	ns	
t <sub>dis</sub>	$\overline{\text{OE}}$	Q	1.9	5.3	4.5	1.4	4.1	ns	

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 10 MHz	19	22	pF
	Outputs enabled		4	5	
	Outputs disabled				



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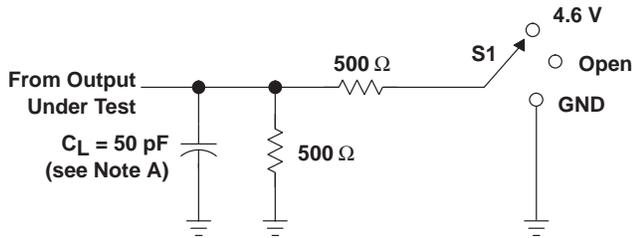
## 16-BIT TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

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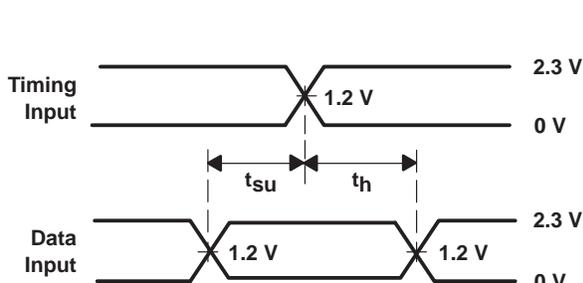
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

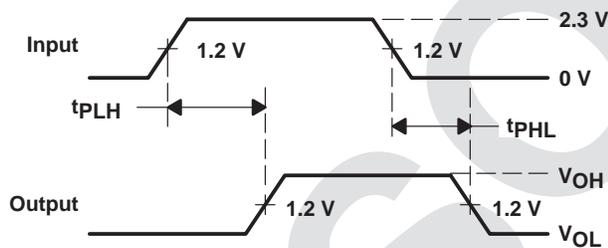


LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	4.6 V
$t_{PHZ}/t_{PZH}$	GND



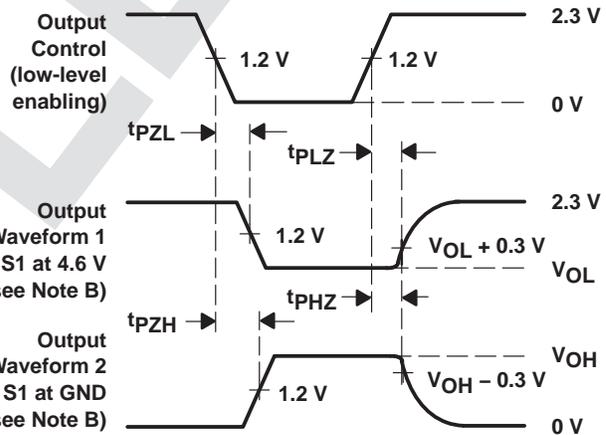
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION

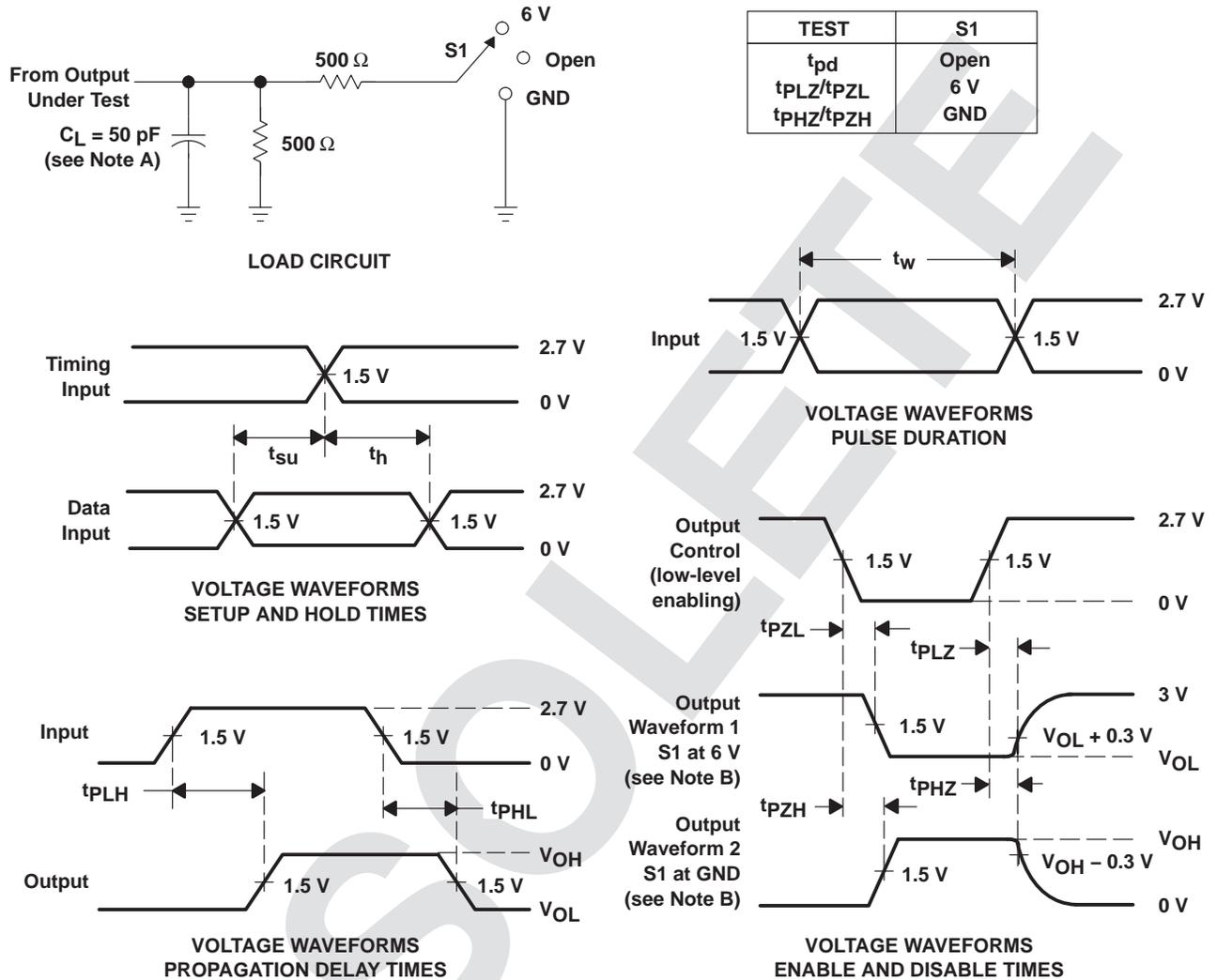


VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74ALVC16373DGGR	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85		
SN74ALVC16373DL	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85		
SN74ALVC16373DLR	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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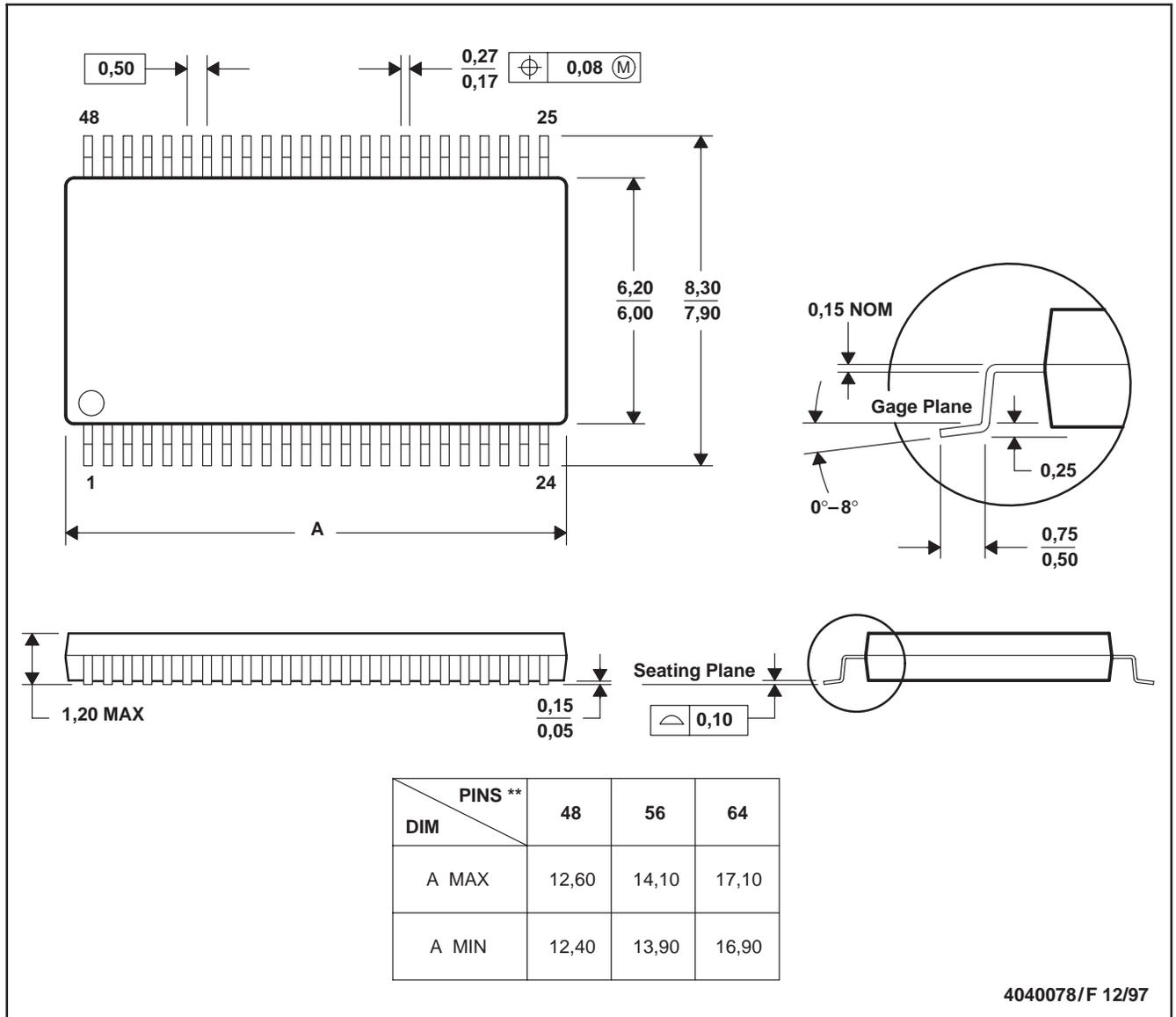
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DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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