D2804, MARCH 1984-REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability
- Totem-Pole Version of 'HC266

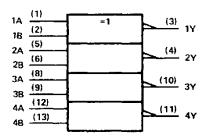
description

These devices are composed of four independent 2-input exclusive-NOR gates. They perform the Boolean functions:

$$Y = \overline{A \oplus B} = \overline{A}\overline{B} + AB$$
 in positive logic.

The SN54HC7266 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC7266 is characterized for operation from -40°C to 85°C.

logic symbol†



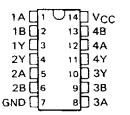
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J or N packages.

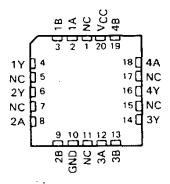
logic symbol (each gate, positive logic)



SN54HC7266 . . . J PACKAGE SN74HC7266 . . . D OR N PACKAGE (TOP VIEW)



SN54HC7266 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

INP	INPUTS			
Α	В	Y		
L	Ĺ	н		
L.	н	L		
н	L	L		
н	Н	Н _		

SN54HC7266, SN74HC7266 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES

absolute maximum ratings over operating free-air temperature range†

Supply voltage, VCC	-0.5	V to 7 V
Input clamp current, IjK (VI < 0 or VI > VCC)		± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)		±20 mA
Continuous output current, IQ (VQ = 0 to VCC)		±25 mA
Continuous current through VCC or GND pins		± 50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package		. 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package		. 260°C
Storage temperature range6	55°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These ere stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7266		SN74HC7266					
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		2	5	6	2	5	6	V	
		V _{CC} = 2 V	1.5			1.5				
ViH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			V	
	V _{CC} = 6 V	4.2			4.2					
		V _{CC} = 2 V	0		0.3	0		0.3]	
٧ _{IL}	V _{IL} Low-level input voltage	V _{CC} = 4.5 V) 0		0.9	0		0.9	V	
		V _{CC} = 6 V	0		1.2	0		1.2		
V _I	Input voltage		0		Vcc	0		Vcc_	V	
۷o	Output voltage		0		VCC	0		Vcc	V	
		V _{CC} = 2 V	0		1000	0		1000		
ŧŧ	Input transition (rise and fall) times	$V_{CC} = 4.5 V$	0		500	0		500	ns	
		V _{CC} = 6 V	0		400	0		400		
TA	Operating free-air temperature		- 55		125	-40		85	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Vcc	TA = 25°C			SN54HC7266		SN74HC7266		(10117
	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		2 V	1.9	1.998		1.9		1.9		
ľ	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4		4.4		
V _{OH}		6 V	5.9	5.999		5.9		5.9		٧
	VI = VIH or VIL, IOH = -4 mA	4.5 V	3.98	4.30		3.7		3.84		
Ì	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -5.2$ mA	6 V	5.48	5.80		5.2		5.34]	
		2 V		0.002	0.1		0.1		0.1	
	$V_{I} = V_{IH}$ or V_{IL} , $I_{OL} = 20 \mu A$	4.5 V	i	0.001	0.1		0.1]	0.1	
VOL		6 V		0.001	0.1		0.1	1	0.1	٧
	V ₁ = V _{1H} or V _{IL} , I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	VI = VIH or VIL, IOL = 5.2 mA .	6 V		0.15	0.26		0.4		0.33	
l ₁	VI = VCC or 0	6 V		±0.1	±100		± 1000		± 1000	nΑ
lcc	$V_I = V_{CC} \text{ or } 0, I_O = 0$	6 V			2		40		20	μA
Ci		2 to 6 V		3	10		10		10	pF

SN54HC7266, SN74HC7266 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L=50~\mathrm{pF}$ (see Note 1)

FROM TO			TA = 25°C	°C	SN54HC7266		SN74HC7266				
PARAMETER	(INPUT)	(OUTPUT)	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		40	100		150		125	
t _{pd}	A or B	Y	4.5 V		12	20	l	30]	25	ns
, .			6 V	1	10	17		25		21	
			2 V		28	75		1 10		95	
tt		Υ Υ	4.5 V		8	15	ļ	22	1	19	ns
			6 V	1	6	13	}	19	1	16	

C _{pd}	Power dissipation capacitance per gate	No load, T _A = 25°C	35 pF typ

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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