

# CDx4HC173, CDx4HCT173 High-Speed CMOS Logic Quad D-Type Flip-Flop, Three-State

## 1 Features

- Three-state buffered outputs
- Gated input and output enables
- Fanout (over temperature range)
  - Standard outputs : 10 LSTTL loads
  - Bus driver outputs : 15 LSTTL loads
- Wide Operating Temperature Range : -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power and reduction compared to LSTTL logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$
- HCT types
  - 4.5 V to 5.5 V Operation
  - Direct LSTTL input logic compatibility,  $V_{IL} = 0.8\text{ V (Max)}$ ,  $V_{IH} = 2\text{ V (Min)}$
  - CMOS input compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

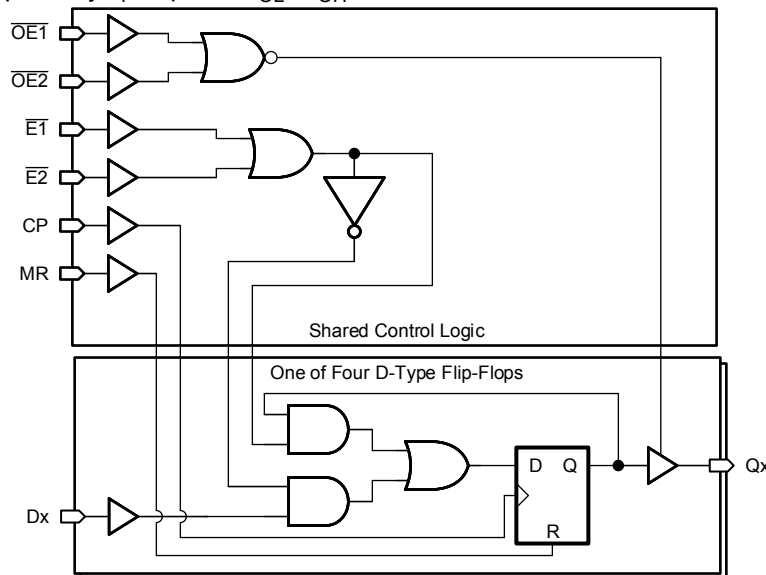
## 2 Description

The CDx4HC173 and CDx4HCT173 contains four independent D-type flip-flops with shared clock (CP), reset (MR), and data enable ( $\overline{E1}$ ,  $\overline{E2}$ ) pins.

### Device Information

| PART NUMBER   | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)    |
|---------------|------------------------|--------------------|
| CD54HC173F    | CDIP (16)              | 21.34 mm × 6.92 mm |
| CD54HCT173F3A | CDIP (16)              | 21.34 mm × 6.92 mm |
| CD74HC173E    | PDIP (16)              | 19.31mm × 6.35 mm  |
| CD74HCT173E   | PDIP (16)              | 19.31mm × 6.35 mm  |
| CD74HC173M    | SOIC (16)              | 9.90 mm × 3.90 mm  |
| CD74HCT173M   | SOIC (16)              | 9.90 mm × 3.90 mm  |
| CD74HC173PW   | TSSOP (16)             | 5.00 mm × 4.40 mm  |

(1) For all packages see the orderable addendum at the end of the data sheet..



**Functional Block Diagram**



## Table of Contents

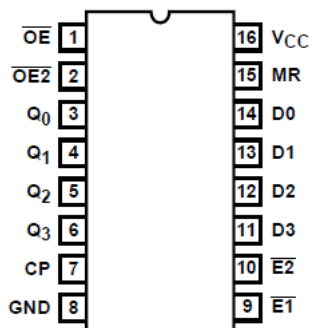
|                                                     |           |                                                                  |           |
|-----------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                             | <b>1</b>  | 7.2 Functional Block Diagram.....                                | <b>10</b> |
| <b>2 Description</b> .....                          | <b>1</b>  | 7.3 Device Functional Modes.....                                 | <b>11</b> |
| <b>3 Revision History</b> .....                     | <b>2</b>  | <b>8 Power Supply Recommendations</b> .....                      | <b>12</b> |
| <b>4 Pin Configuration and Functions</b> .....      | <b>3</b>  | <b>9 Layout</b> .....                                            | <b>12</b> |
| <b>5 Specifications</b> .....                       | <b>4</b>  | 9.1 Layout Guidelines.....                                       | <b>12</b> |
| 5.1 Absolute Maximum Ratings .....                  | <b>4</b>  | <b>10 Device and Documentation Support</b> .....                 | <b>13</b> |
| 5.2 Recommended Operating Conditions.....           | <b>4</b>  | 10.1 Documentation Support.....                                  | <b>13</b> |
| 5.3 Thermal Information.....                        | <b>4</b>  | 10.2 Receiving Notification of Documentation Updates..           | <b>13</b> |
| 5.4 Electrical Characteristics.....                 | <b>5</b>  | 10.3 Support Resources.....                                      | <b>13</b> |
| 5.5 Switching Characteristics.....                  | <b>6</b>  | 10.4 Trademarks.....                                             | <b>13</b> |
| 5.6 Prerequisite For Switching Characteristics..... | <b>7</b>  | 10.5 Electrostatic Discharge Caution.....                        | <b>13</b> |
| <b>6 Parameter Measurement Information</b> .....    | <b>8</b>  | 10.6 Glossary.....                                               | <b>13</b> |
| <b>7 Detailed Description</b> .....                 | <b>10</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>13</b> |
| 7.1 Overview.....                                   | <b>10</b> |                                                                  |           |

## 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision E (October 2003) to Revision F (March 2022)</b>                                                                                                                       | <b>Page</b> |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <ul style="list-style-type: none"> <li>Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....</li> </ul> | <b>1</b>    |

## 4 Pin Configuration and Functions



J, N, D, or PW Package  
16-Pin CDIP, PDIP, SOIC, or TSSOP  
Top View

## 5 Specifications

### 5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |                                                          | MIN                                                    | MAX | UNIT   |
|-----------|----------------------------------------------------------|--------------------------------------------------------|-----|--------|
| $V_{CC}$  | Supply voltage                                           | -0.5                                                   | 7   | V      |
| $I_{IK}$  | Input diode current <sup>(2)</sup>                       | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ |     | ±20 mA |
| $I_{OK}$  | Output diode current <sup>(2)</sup>                      | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ |     | ±20 mA |
| $I_O$     | Output source or sink current per output pin             | $V_O > -0.5\text{ V}$ or $V_O < V_{CC} + 0.5\text{ V}$ |     | ±25 mA |
|           | Continuous current through $V_{CC}$ or GND               |                                                        |     | ±70 mA |
| $T_J$     | Junction temperature                                     |                                                        |     | 150 °C |
|           | Lead temperature (soldering 10s) (SOIC - lead tips only) |                                                        |     | 300 °C |
| $T_{stg}$ | Storage temperature                                      | -65                                                    | 150 | °C     |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions

|          |                          |                         | MIN | MAX      | UNIT |
|----------|--------------------------|-------------------------|-----|----------|------|
| $V_{CC}$ | Supply voltage range     | HC types                | 2   | 6        | V    |
|          |                          | HCT types               | 4.5 | 5.5      |      |
| $V_I$    | Input voltage            |                         | 0   | $V_{CC}$ | V    |
| $V_O$    | Output voltage           |                         | 0   | $V_{CC}$ | V    |
| $t_t$    | Input rise and fall time | $V_{CC} = 2\text{ V}$   |     | 1000     | ns   |
|          |                          | $V_{CC} = 4.5\text{ V}$ |     | 500      |      |
|          |                          | $V_{CC} = 6\text{ V}$   |     | 400      |      |
| $T_A$    | Temperature range        |                         | -55 | 125      | °C   |

### 5.3 Thermal Information

| THERMAL METRIC  |                                                       | N (PDIP) | D (SOIC) | NS (SOP) | PW (TSSOP) | UNIT |
|-----------------|-------------------------------------------------------|----------|----------|----------|------------|------|
|                 |                                                       | 16 PINS  | 16 PINS  | 16 PINS  | 16 PINS    |      |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance <sup>(1)</sup> | 67       | 73       | 64       | 108        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report

## 5.4 Electrical Characteristics

| PARAMETER                           |                                            | TEST<br>CONDITIONS <sup>(1)</sup> | V <sub>CC</sub> | 25°C |     |       | –40°C to 85°C |       | –55°C to 125°C |     | UNIT |
|-------------------------------------|--------------------------------------------|-----------------------------------|-----------------|------|-----|-------|---------------|-------|----------------|-----|------|
|                                     |                                            |                                   |                 | MIN  | TYP | MAX   | MIN           | MAX   | MIN            | MAX |      |
| HC TYPES                            |                                            |                                   |                 |      |     |       |               |       |                |     |      |
| V <sub>IH</sub>                     | High-level input voltage                   |                                   | 2               | 1.5  |     | 1.5   |               | 1.5   |                | V   |      |
|                                     |                                            |                                   | 4.5             | 3.15 |     | 3.15  |               | 3.15  |                | V   |      |
|                                     |                                            |                                   | 6               | 4.2  |     | 4.2   |               | 4.2   |                | V   |      |
| V <sub>IL</sub>                     | Low-level input voltage                    |                                   | 2               | 0.5  |     | 0.5   |               | 0.5   |                | V   |      |
|                                     |                                            |                                   | 4.5             | 1.35 |     | 1.35  |               | 1.35  |                | V   |      |
|                                     |                                            |                                   | 6               | 1.8  |     | 1.8   |               | 1.8   |                | V   |      |
| V <sub>OH</sub>                     | High-level output voltage<br>CMOS loads    | I <sub>OH</sub> = – 20μA          | 2               | 1.9  |     | 1.9   |               | 1.9   |                | V   |      |
|                                     |                                            | I <sub>OH</sub> = – 20μA          | 4.5             | 4.4  |     | 4.4   |               | 4.4   |                | V   |      |
|                                     |                                            | I <sub>OH</sub> = – 20μA          | 6               | 5.9  |     | 5.9   |               | 5.9   |                | V   |      |
|                                     | High-level output voltage<br>TTL loads     | I <sub>OH</sub> = – 6mA           | 4.5             | 3.98 |     | 3.84  |               | 3.7   |                | V   |      |
|                                     |                                            | I <sub>OH</sub> = – 7.8mA         | 6               | 5.48 |     | 5.34  |               | 5.2   |                | V   |      |
| V <sub>OL</sub>                     | Low-level output voltage<br>CMOS loads     | I <sub>OL</sub> = 20μA            | 2               | 0.1  |     | 0.1   |               | 0.1   |                | V   |      |
|                                     |                                            | I <sub>OL</sub> = 20μA            | 4.5             | 0.1  |     | 0.1   |               | 0.1   |                | V   |      |
|                                     |                                            | I <sub>OL</sub> = 20μA            | 6               | 0.1  |     | 0.1   |               | 0.1   |                | V   |      |
|                                     | Low-level output voltage<br>TTL loads      | I <sub>OL</sub> = 6mA             | 4.5             | 0.26 |     | 0.33  |               | 0.4   |                | V   |      |
|                                     |                                            | I <sub>OL</sub> = 7.8mA           | 6               | 0.26 |     | 0.33  |               | 0.4   |                | V   |      |
| I <sub>I</sub>                      | Input leakage current                      | V <sub>CC</sub> or GND            | 6               | ±0.1 |     | ±1    |               | ±1    |                | μA  |      |
| I <sub>CC</sub>                     | Supply current                             | V <sub>CC</sub> or GND            | 6               | 8    |     | 80    |               | 160   |                | μA  |      |
| I <sub>OZ</sub>                     | Three-state leakage current                |                                   | 6               | ±0.5 |     | ±0.5  |               | ±10   |                | μA  |      |
| HCT TYPES                           |                                            |                                   |                 |      |     |       |               |       |                |     |      |
| V <sub>IH</sub>                     | High-level input voltage                   |                                   | 4.5 to 5.5      | 2    |     | 2     |               | 2     |                | V   |      |
| V <sub>IL</sub>                     | Low-level input voltage                    |                                   | 4.5 to 5.5      | 0.8  |     | 0.8   |               | 0.8   |                | V   |      |
| V <sub>OH</sub>                     | High-level output voltage<br>CMOS loads    | I <sub>OH</sub> = – 20μA          | 4.5             | 4.4  |     | 4.4   |               | 4.4   |                | V   |      |
|                                     | High-level output voltage<br>TTL loads     | I <sub>OH</sub> = – 6mA           | 4.5             | 3.98 |     | 3.84  |               | 3.7   |                | V   |      |
| V <sub>OL</sub>                     | Low-level output voltage<br>CMOS loads     | I <sub>OL</sub> = 20μA            | 4.5             | 0.1  |     | 0.1   |               | 0.1   |                | V   |      |
|                                     | Low-level output voltage<br>TTL loads      | I <sub>OL</sub> = 6mA             | 4.5             | 0.26 |     | 0.33  |               | 0.4   |                | V   |      |
| I <sub>I</sub>                      | Input leakage current                      | V <sub>CC</sub> and GND           | 5.5             | ±0.1 |     | ±1    |               | ±1    |                | μA  |      |
| I <sub>CC</sub>                     | Supply Current                             | V <sub>CC</sub> and GND           | 5.5             | 8    |     | 80    |               | 160   |                | μA  |      |
| ΔI <sub>CC</sub> <sup>(2) (3)</sup> | Additional supply current<br>per input pin | One of D0-D3                      | 4.5 to 5.5      | 15   | 54  | 67.5  |               | 73.5  |                | μA  |      |
|                                     |                                            | One of E1 and E2                  | 4.5 to 5.5      | 15   | 54  | 67.5  |               | 73.5  |                | μA  |      |
|                                     |                                            | CP                                | 4.5 to 5.5      | 25   | 90  | 112.5 |               | 122.5 |                | μA  |      |
|                                     |                                            | MR                                | 4.5 to 5.5      | 20   | 72  | 90    |               | 98    |                | μA  |      |
|                                     |                                            | One of OE1 and OE2                | 4.5 to 5.5      | 50   | 180 | 225   |               | 245   |                | μA  |      |

| PARAMETER       |                             | TEST CONDITIONS <sup>(1)</sup> | V <sub>CC</sub> | 25°C |     |      | –40°C to 85°C |      | –55°C to 125°C |     | UNIT |
|-----------------|-----------------------------|--------------------------------|-----------------|------|-----|------|---------------|------|----------------|-----|------|
|                 |                             |                                |                 | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |      |
| I <sub>OZ</sub> | Three-state leakage current |                                | 5.5             |      |     | ±0.5 |               | ±5.0 |                | ±10 | μA   |

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

(2) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(3) Inputs held at V<sub>CC</sub> – 2.1.

## 5.5 Switching Characteristics

Input t<sub>I</sub> = 6ns. Unless otherwise specified, C<sub>L</sub> = 50pF

| PARAMETER                          |                                                 | V <sub>CC</sub> (V) | 25°C              |     | -40°C to 85°C | -55°C to 125°C | UNIT |
|------------------------------------|-------------------------------------------------|---------------------|-------------------|-----|---------------|----------------|------|
|                                    |                                                 |                     | TYP               | MAX | MAX           | MAX            |      |
| HC TYPES                           |                                                 |                     |                   |     |               |                |      |
| t <sub>pd</sub>                    | Propagation delay, clock to output              | 2                   |                   | 200 | 250           | 300            | ns   |
|                                    |                                                 | 4.5                 | 17 <sup>(1)</sup> | 40  | 50            | 60             |      |
|                                    |                                                 | 6                   |                   | 34  | 43            | 51             |      |
| t <sub>pd</sub>                    | Propagation delay, MR to output                 | 2                   |                   | 175 | 220           | 265            | ns   |
|                                    |                                                 | 4.5                 | 12 <sup>(1)</sup> | 35  | 44            | 53             |      |
|                                    |                                                 | 6                   |                   | 30  | 37            | 45             |      |
| t <sub>pd</sub>                    | Propagation delay output enable to Q (Figure 6) | 2                   |                   | 150 | 190           | 225            | ns   |
|                                    |                                                 | 4.5                 | 12 <sup>(1)</sup> | 30  | 38            | 45             |      |
|                                    |                                                 | 6                   |                   | 26  | 33            | 38             |      |
| t <sub>t</sub>                     | Output transition times                         | 2                   |                   | 60  | 75            | 90             | ns   |
|                                    |                                                 | 4.5                 |                   | 12  | 15            | 18             |      |
|                                    |                                                 | 6                   |                   | 10  | 13            | 15             |      |
| f <sub>MAX</sub>                   | Maximum clock frequency                         | 5                   | 60 <sup>(1)</sup> |     |               |                | MHz  |
| C <sub>i</sub>                     | Input capacitance                               |                     |                   | 10  | 10            | 10             | pF   |
| C <sub>O</sub>                     | Three-state output capacitance                  |                     |                   | 10  | 10            | 10             | pF   |
| C <sub>pd</sub> <sup>(2) (3)</sup> | Power dissipation capacitance                   | 5                   | 29                |     |               |                | pF   |
| HCT TYPES                          |                                                 |                     |                   |     |               |                |      |
| t <sub>pd</sub>                    | Propagation delay, clock to output              | 4.5                 | 17 <sup>(1)</sup> | 40  | 50            | 60             | ns   |
| t <sub>pd</sub>                    | Propagation delay, MR to output                 | 4.5                 | 18 <sup>(1)</sup> | 44  | 55            | 66             | ns   |
| t <sub>pd</sub>                    | Propagation delay output enable to Q (Figure 6) | 2                   |                   | 150 | 190           | 225            | ns   |
|                                    |                                                 | 4.5                 | 14 <sup>(1)</sup> | 30  | 38            | 45             |      |
|                                    |                                                 | 6                   |                   | 26  | 33            | 38             |      |
| t <sub>t</sub>                     | Output transition times                         | 4.5                 |                   | 15  | 19            | 22             | ns   |
| f <sub>MAX</sub>                   | Maximum clock frequency                         | 5                   | 60 <sup>(1)</sup> |     |               |                | MHz  |
| C <sub>i</sub>                     | Input capacitance                               |                     |                   | 10  | 10            | 10             | pF   |
| C <sub>pd</sub> <sup>(2) (3)</sup> | Power dissipation capacitance                   | 5                   | 34                |     |               |                | pF   |

(1) Typical value tested at 5V, C<sub>L</sub> = 15pF.

(2) C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

(3) P<sub>D</sub> = V<sub>CC</sub><sup>2</sup>f<sub>i</sub> + Σ (C<sub>L</sub> V<sub>CC</sub><sup>2</sup> + f<sub>O</sub>) where f<sub>i</sub> = Input Frequency, C<sub>L</sub> = Output Load Capacitance, V<sub>CC</sub> = Supply Voltage.

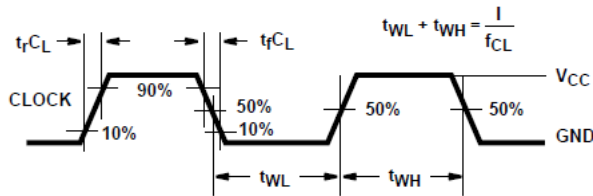
## 5.6 Prerequisite For Switching Characteristics

| PARAMETER                     |                                                   | V <sub>CC</sub> (V) | 25°C |     | -40°C to 85°C |     | -55°C to 125°C |     | UNITS |
|-------------------------------|---------------------------------------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
|                               |                                                   |                     | MIN  | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                      |                                                   |                     |      |     |               |     |                |     |       |
| f <sub>MAX</sub>              | Maximum clock frequency                           | 2                   | 6    | 5   | 4             | MHz |                |     |       |
|                               |                                                   | 4.5                 | 30   | 24  | 20            |     |                |     |       |
|                               |                                                   | 6                   | 35   | 28  | 24            |     |                |     |       |
| t <sub>W</sub>                | MR pulse width                                    | 2                   | 80   | 100 | 120           | ns  |                |     |       |
|                               |                                                   | 4.5                 | 16   | 20  | 24            |     |                |     |       |
|                               |                                                   | 6                   | 14   | 17  | 20            |     |                |     |       |
| t <sub>W</sub>                | Clock pulse width                                 | 2                   | 80   | 100 | 120           | ns  |                |     |       |
|                               |                                                   | 4.5                 | 16   | 20  | 24            |     |                |     |       |
|                               |                                                   | 6                   | 14   | 17  | 20            |     |                |     |       |
| t <sub>SU</sub>               | Set-up time, data to clock and $\bar{E}$ to clock | 2                   | 60   | 75  | 90            | ns  |                |     |       |
|                               |                                                   | 4.5                 | 12   | 15  | 18            |     |                |     |       |
|                               |                                                   | 6                   | 10   | 13  | 15            |     |                |     |       |
| t <sub>H</sub>                | Hold time, data to clock                          | 2                   | 3    | 3   | 3             | ns  |                |     |       |
|                               |                                                   | 4.5                 | 3    | 3   | 3             |     |                |     |       |
|                               |                                                   | 6                   | 3    | 3   | 3             |     |                |     |       |
| t <sub>H</sub>                | Hold time, $\bar{E}$ to clock                     | 2                   | 0    | 0   | 0             | ns  |                |     |       |
|                               |                                                   | 4.5                 | 0    | 0   | 0             |     |                |     |       |
|                               |                                                   | 6                   | 0    | 0   | 0             |     |                |     |       |
| t <sub>REM</sub>              | Removal time, MR to clock                         | 2                   | 60   | 75  | 90            | ns  |                |     |       |
|                               |                                                   | 4.5                 | 12   | 15  | 18            |     |                |     |       |
|                               |                                                   | 6                   | 10   | 13  | 15            |     |                |     |       |
| HCT TYPES                     |                                                   |                     |      |     |               |     |                |     |       |
| f <sub>MAX</sub>              | Maximum clock frequency                           | 4.5                 | 20   | 16  | 13            | MHz |                |     |       |
| t <sub>W</sub> t <sub>W</sub> | MR pulse width                                    | 4.5                 | 15   | 19  | 22            | ns  |                |     |       |
| t <sub>W</sub>                | Clock pulse width                                 | 4.5                 | 25   | 31  | 38            | ns  |                |     |       |
| t <sub>SU</sub>               | Set-up Time, $\bar{E}$ to clock                   | 4.5                 | 12   | 15  | 18            | ns  |                |     |       |
| t <sub>SU</sub>               | Set-up time, data to clock                        | 4.5                 | 18   | 23  | 27            | ns  |                |     |       |
| t <sub>H</sub>                | Hold time, data to clock                          | 4.5                 | 0    | 0   | 0             | ns  |                |     |       |
| t <sub>H</sub>                | Hold time, $\bar{E}$ to clock                     | 4.5                 | 0    | 0   | 0             | ns  |                |     |       |
| t <sub>REM</sub>              | Removal time, MR to clock                         | 4.5                 | 12   | 15  | 18            | ns  |                |     |       |

## 6 Parameter Measurement Information

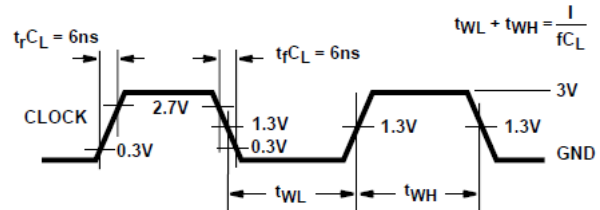
$t_{PD}$  is the maximum between  $t_{PLH}$  and  $t_{PHL}$

$t_t$  is the maximum between  $t_{TLH}$  and  $t_{THL}$



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%

Figure 6-1. HC clock pulse rise and fall times and pulse width



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%

Figure 6-2. HCT clock pulse rise and fall times and pulse width

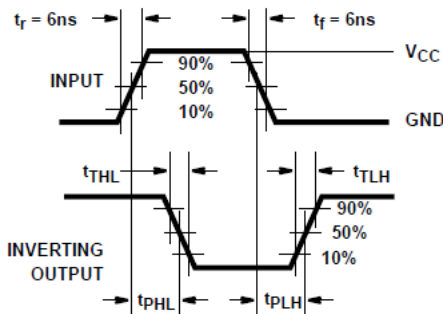


Figure 6-3. HC and HCU transition times and propagation delay times, combination logic

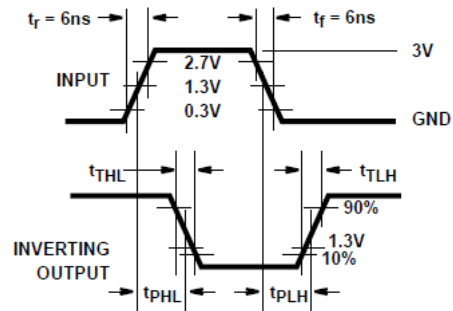


Figure 6-4. HCT transition times and propagation delay times, combination logic

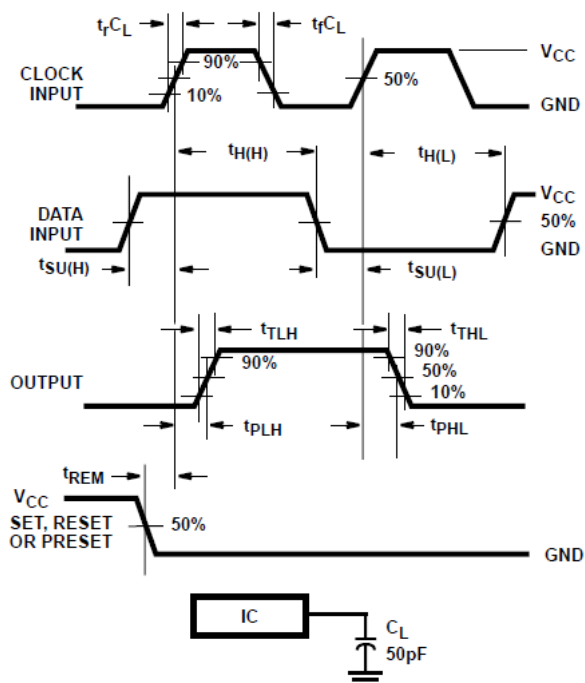


Figure 6-5. HC setup times, hold times, removal time, and propagation delay times for edge triggered sequential logic circuits

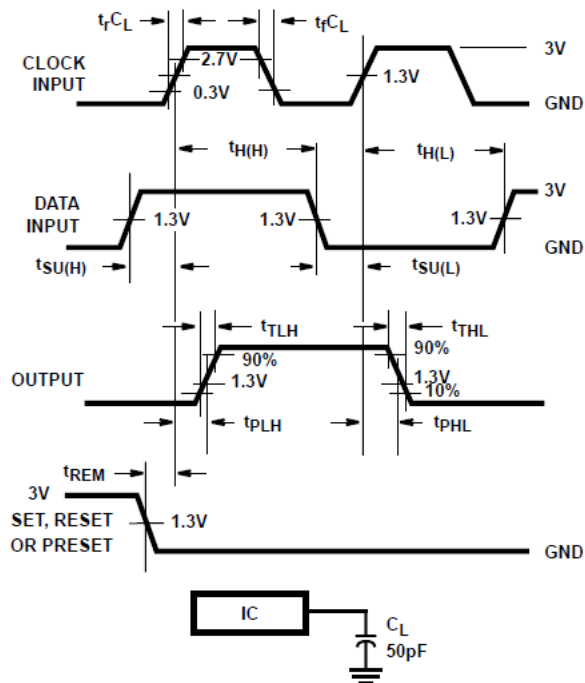


Figure 6-6. HCT setup times, hold times, removal time, and propagation delay times for edge triggered sequential logic circuits

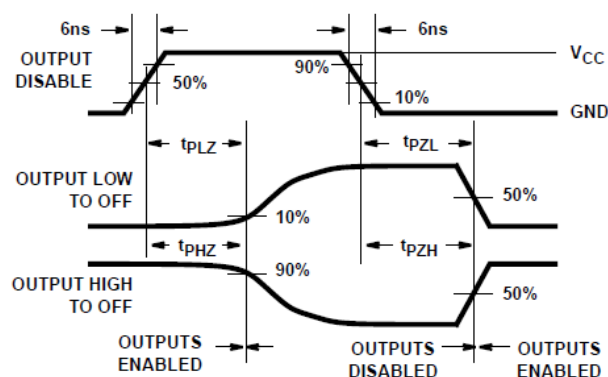


Figure 6-7. HC three-state propagation delay waveform

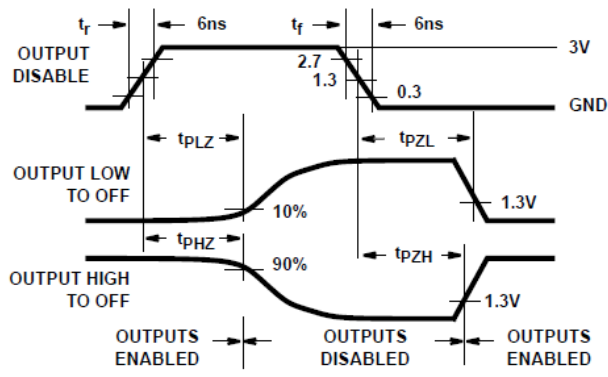
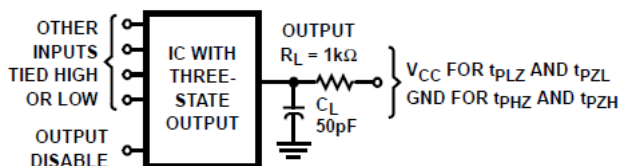


Figure 6-8. HCT three-state propagation delay waveform



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$

Figure 6-9. HC and HCT three-state propagation delay test circuit

## 7 Detailed Description

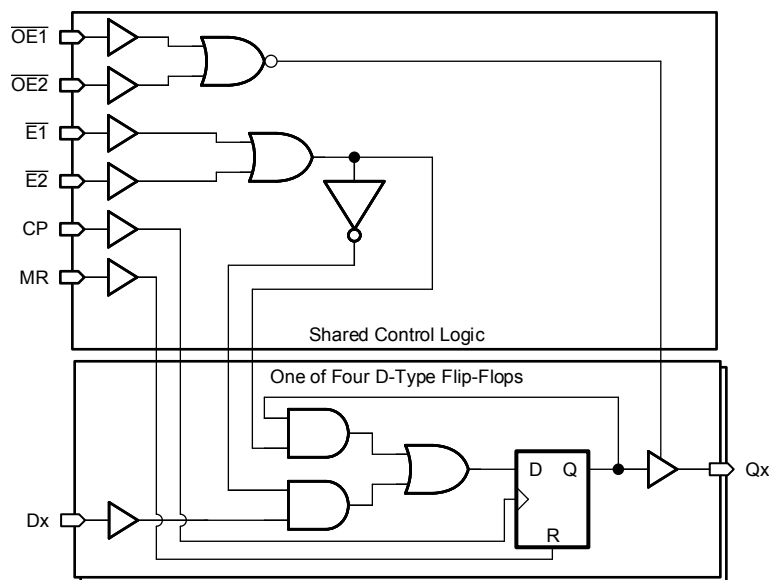
### 7.1 Overview

The CDx4HC173 or CDx4HCT173 high speed three-state quad D-type flip-flops are fabricated with silicon gate CMOS technology. They possess the low power consumption of standard CMOS Integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky devices. The buffered outputs can drive 15 LSTTL loads. The large output drive capability and three-state feature make these parts ideally suited for interfacing with bus lines in bus oriented systems

The four D-type flip-flops operate synchronously from a common clock. The outputs are in the three-state mode when either of the two output disable pins are at the logic "1" level. The input ENABLES allow the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input ENABLES are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Reset is enabled by taking the RESET (MR) input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

The 'HCT173 logic family is functionally, as well as pin compatible with the standard LS logic family.

### 7.2 Functional Block Diagram



## 7.3 Device Functional Modes

**Table 7-1. Truth Table**<sup>(1)(2)</sup>

| INPUTS |    |             |    | DATA | OUTPUT         |
|--------|----|-------------|----|------|----------------|
| MR     | CP | DATA ENABLE |    |      |                |
|        |    | E1          | E2 | D    | Q <sub>n</sub> |
| H      | X  | X           | X  | X    | L              |
| L      | L  | X           | X  | X    | Q <sub>0</sub> |
| L      | ↑  | H           | X  | X    | Q <sub>0</sub> |
| L      | ↑  | X           | H  | X    | Q <sub>0</sub> |
| L      | ↑  | L           | L  | L    | L              |
| L      | ↑  | L           | L  | H    | H              |

- (1) H = High voltage level. L = Low voltage level. X = Irrelevant. ↑ = Transition from low to high level. Q<sub>0</sub> = Level before the indicated steady-state input conditions were established.
- (2) When either OE1 or OE2 (or both) is (are) high, the output is disabled to the high-impedance stat, however, sequential operation of the flip-flops is not affected.

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.4 Trademarks

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### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)         | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 5962-8682501EA   | ACTIVE        | CDIP         | J                  | 16   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8682501EA<br>CD54HC173F3A  | <a href="#">Samples</a> |
| 5962-8875901EA   | ACTIVE        | CDIP         | J                  | 16   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8875901EA<br>CD54HCT173F3A | <a href="#">Samples</a> |
| CD54HC173F       | ACTIVE        | CDIP         | J                  | 16   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | CD54HC173F                      | <a href="#">Samples</a> |
| CD54HC173F3A     | ACTIVE        | CDIP         | J                  | 16   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8682501EA<br>CD54HC173F3A  | <a href="#">Samples</a> |
| CD54HCT173F3A    | ACTIVE        | CDIP         | J                  | 16   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8875901EA<br>CD54HCT173F3A | <a href="#">Samples</a> |
| CD74HC173E       | ACTIVE        | PDIP         | N                  | 16   | 25             | RoHS & Green        | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD74HC173E                      | <a href="#">Samples</a> |
| CD74HC173M       | ACTIVE        | SOIC         | D                  | 16   | 40             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HC173M                          | <a href="#">Samples</a> |
| CD74HC173M96     | ACTIVE        | SOIC         | D                  | 16   | 2500           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HC173M                          | <a href="#">Samples</a> |
| CD74HC173PWR     | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | RoHS & Green        | NIPDAU   SN                          | Level-1-260C-UNLIM   | -55 to 125   | HJ173                           | <a href="#">Samples</a> |
| CD74HCT173E      | ACTIVE        | PDIP         | N                  | 16   | 25             | RoHS & Green        | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD74HCT173E                     | <a href="#">Samples</a> |
| CD74HCT173M      | ACTIVE        | SOIC         | D                  | 16   | 40             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HCT173M                         | <a href="#">Samples</a> |
| CD74HCT173M96    | ACTIVE        | SOIC         | D                  | 16   | 2500           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | HCT173M                         | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- <sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- <sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- <sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- <sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC173, CD54HCT173, CD74HC173, CD74HCT173 :**

- Catalog : [CD74HC173](#), [CD74HCT173](#)
- Military : [CD54HC173](#), [CD54HCT173](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

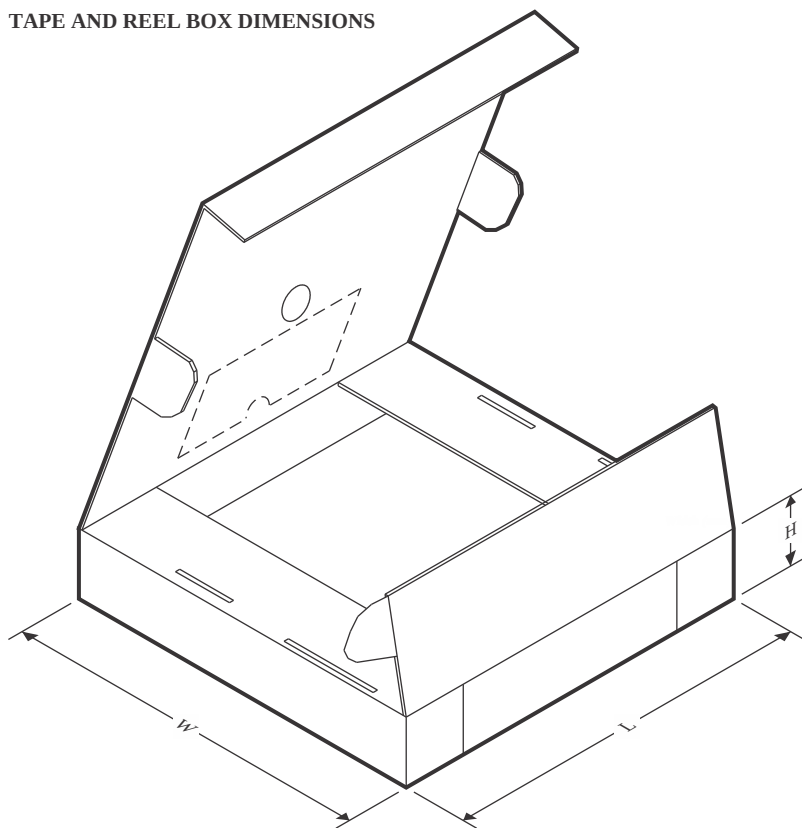
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC173M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC173PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.85    | 5.45    | 1.6     | 8.0     | 12.0   | Q1            |
| CD74HC173PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD74HC173PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD74HCT173M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC173M96  | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| CD74HC173PWR  | TSSOP        | PW              | 16   | 2000 | 366.0       | 364.0      | 50.0        |
| CD74HC173PWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| CD74HC173PWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| CD74HCT173M96 | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |

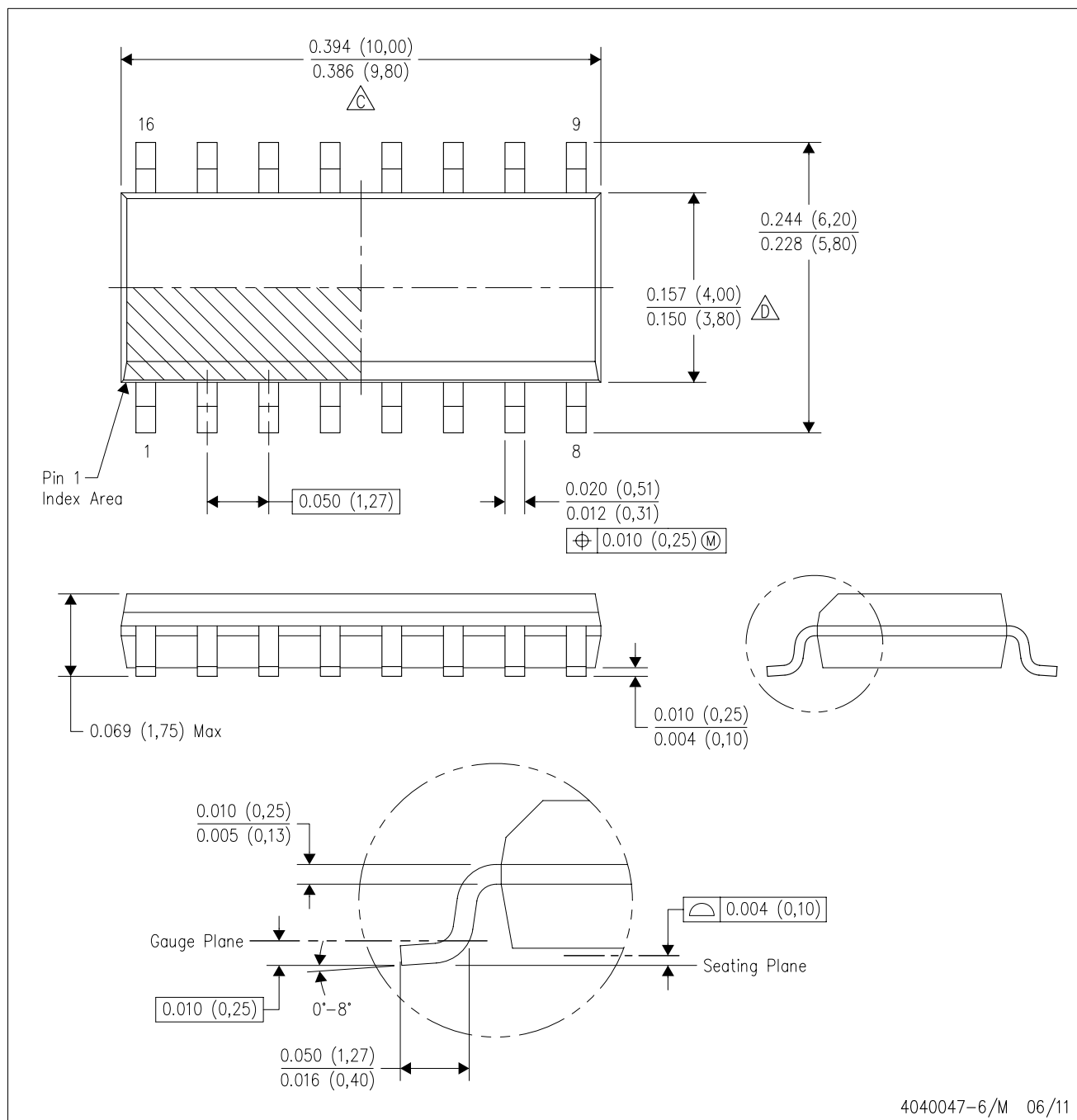
**TUBE**


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC173E  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC173E  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC173M  | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| CD74HCT173E | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT173E | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT173M | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |

D (R-PDSO-G16)

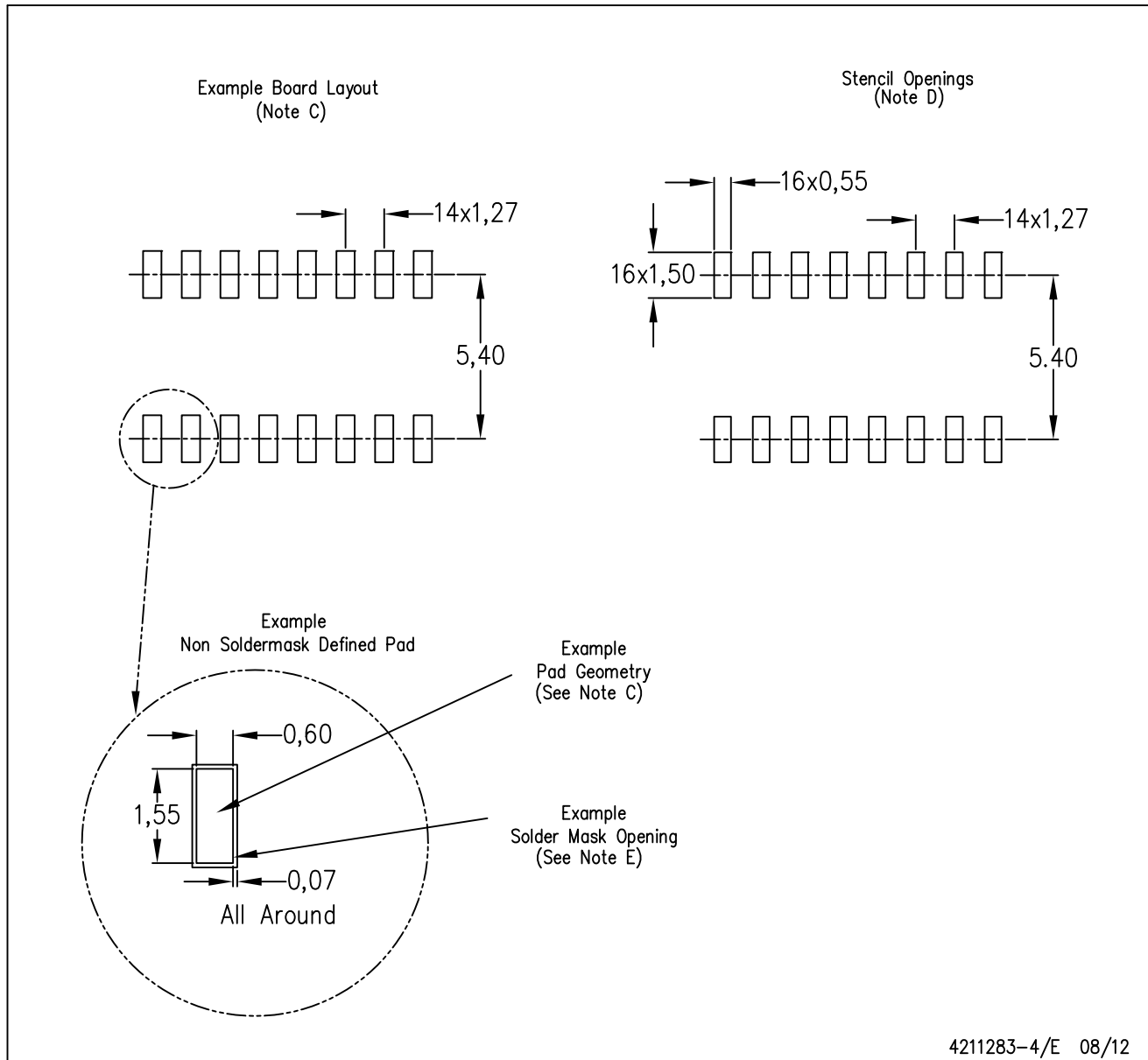
PLASTIC SMALL OUTLINE



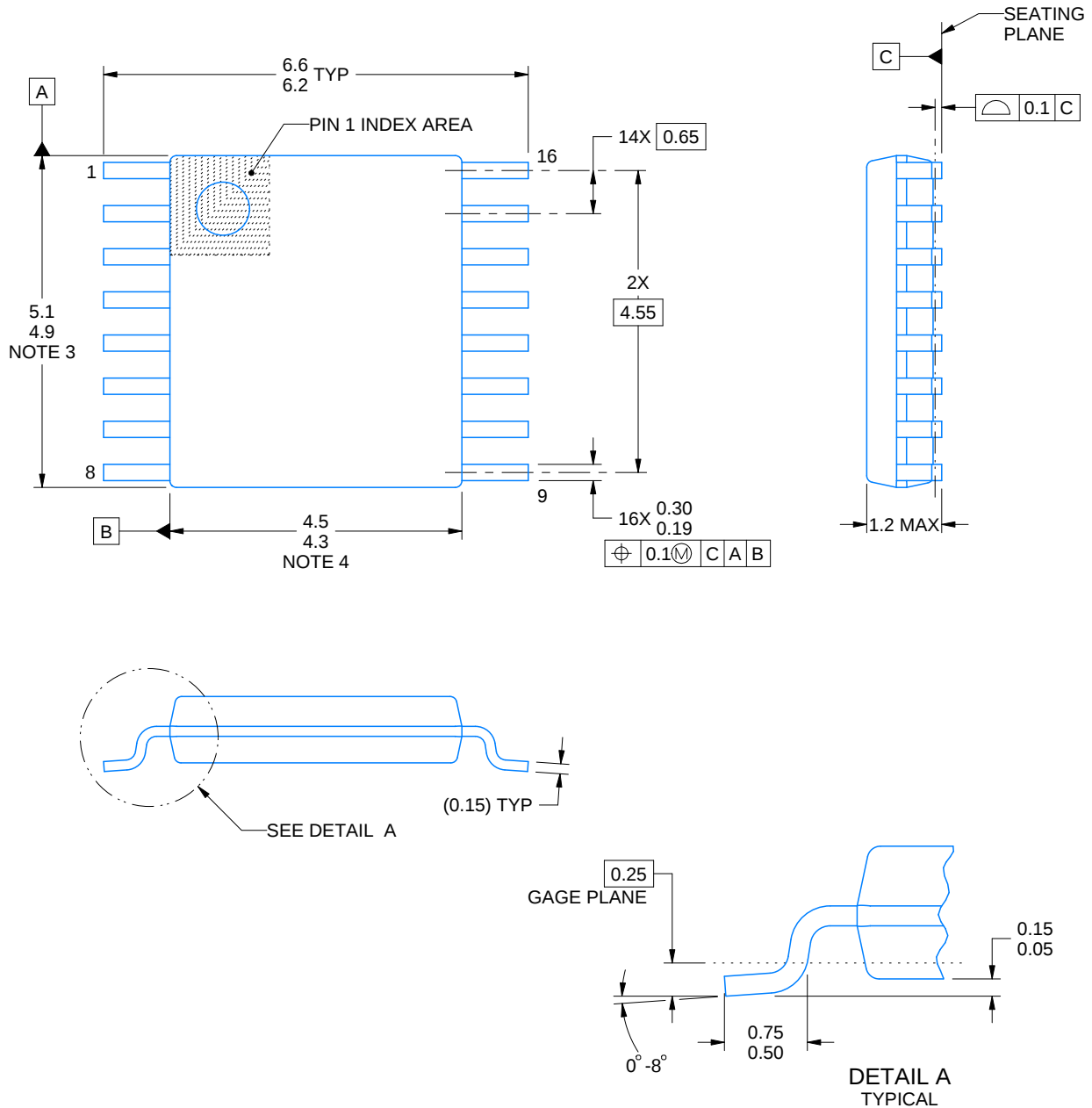
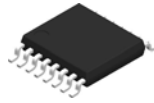
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

## NOTES:

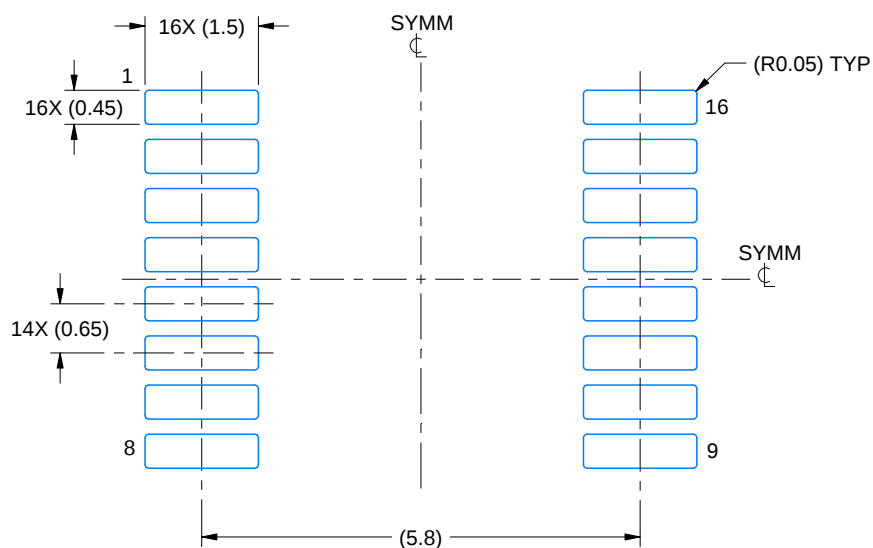
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

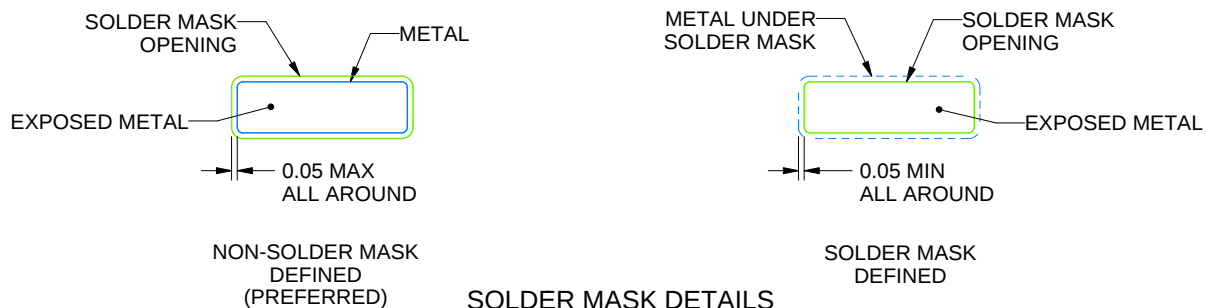
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

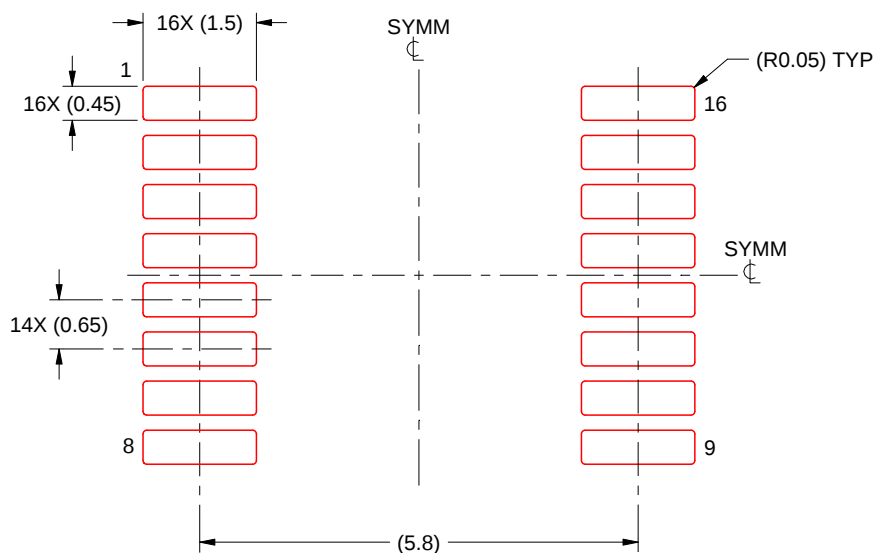
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

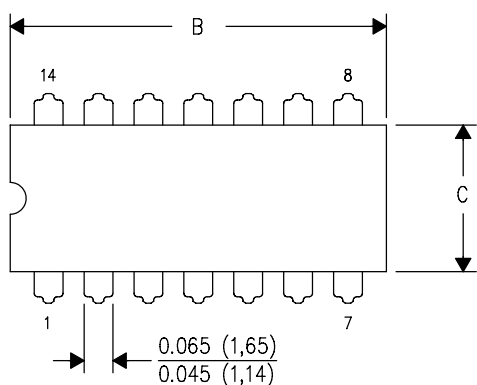
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

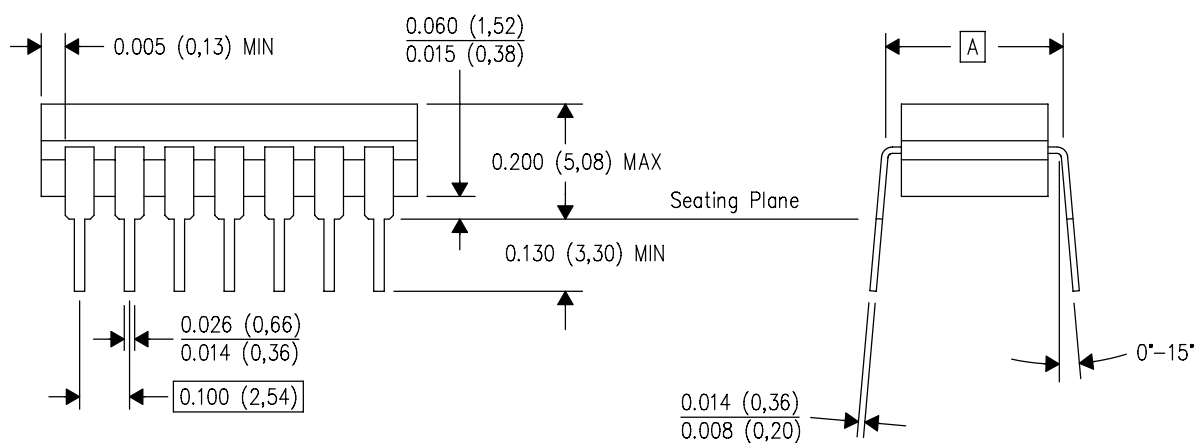
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



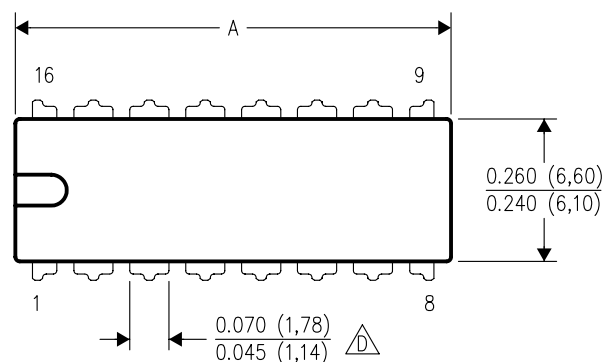
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

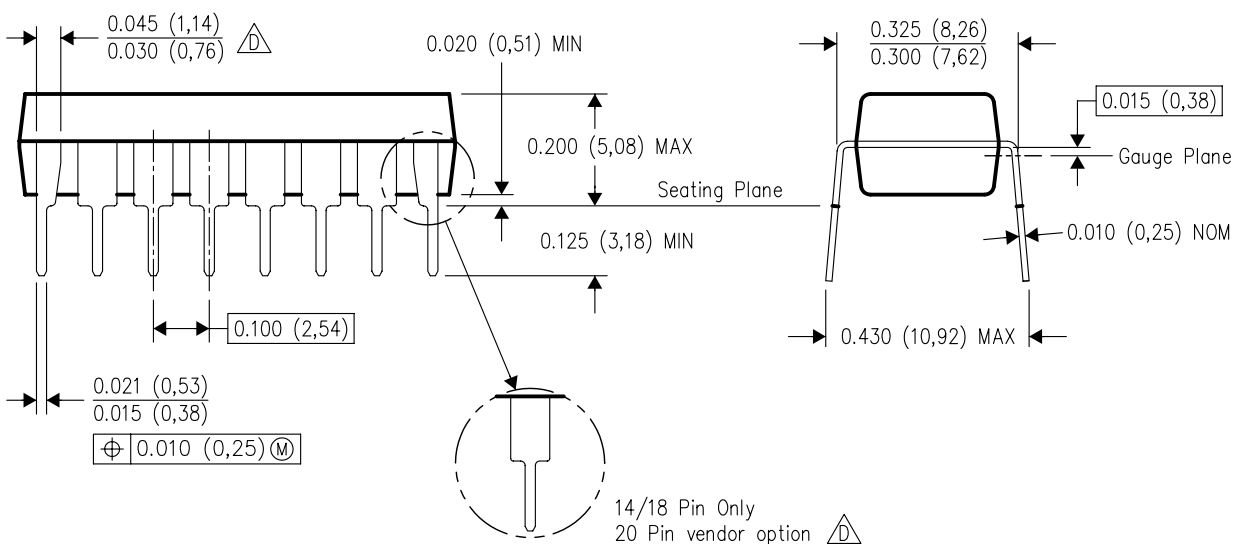
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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