

## Description

The LAN8650/1 combines a Media Access Controller (MAC) and an Ethernet PHY to enable low-cost microcontrollers, including those without an on-board MAC, to access 10BASE-T1S networks. The common standard Serial Peripheral Interface (SPI) of the LAN8650/1 allows interfacing with nearly any microcontroller, so that the transfer of Ethernet packets and LAN8650/1 control/status commands are performed over a single, serial interface. SPI also requires only 4 pins, enabling a simpler hardware interface with fewer pins than MII or RMII.

Ethernet packets are segmented and transferred over the serial interface according to the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification. The serial interface protocol can simultaneously transfer both transmit and receive packets between the station controller and the LAN8650/1, using either store and forward or cut-through packet handling.

### Highlights

- High-performance 10BASE-T1S single-pair Ethernet PHY designed to IEEE Std. 802.3cg -2019
  - 10 Mbit/s over a single balanced pair
    - Half-duplex multidrop mixing segments up to at least 25m with up to at least 8 PHYs
    - Half-duplex point-to-point link segments up to at least 15m
- Physical Layer Collision Avoidance (PLCA)
  - Burst mode for transmission of multiple packets for latency-sensitive applications
  - Minimize latency for time-sensitive applications by assigning multiple PLCA IDs per node
- Carrier Sense Multiple Access / Collision Detection (CSMA/CD) media access control
- Application Controlled Media Access (ACMA) for implementation of collision-free Time-Division Multiple Access (TDMA) methods
- Integrated Media Access Controller (MAC)
- Industry standard Serial Peripheral Interface (SPI), designed to the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification, V1.1

- Support for Time Sensitive Networks (IEEE Std 802.1AS™ / IEEE 1588™)
  - Internal wall clock
  - Event generation and event capture synchronized to the wall clock
  - Phase adjuster for the wall clock to minimize microcontroller overhead
  - Packet timestamping
- Credit-based traffic shaping
- EtherGREEN™ Energy Efficiency
  - Ultra-low power sleep mode
  - Wake up triggered by either MDI activity or local WAKE\_IN
  - WAKE\_OUT pulse assertion; INH output for enable/disable of ECU supply
- Over-temperature and under-voltage protection
- Cable fault diagnostics and Signal Quality Indication (SQI) support
- Enhanced electromagnetic compatibility / electromagnetic interference (EMC/EMI) performance
- Single 3.3V supply with integrated 1.8V regulator (LAN8651)
- Small footprint 32-pin (5 x 5 mm) VQFN package with wettable flanks
- -40°C to +125°C extended temperature range
- AEC-Q100 qualification
- Functional Safety Support: Functional Safety Manual, FMEDA, Dependent Failure Analysis (DFA)

### Target Applications

- In-vehicle networking and automotive zonal architecture
- Sensor/actuator networks and machine control
- Industrial control cabinets and building automation
- LED lighting

This page intentionally left blank.

## Conformity

[Table 1](#) shows the conformity relationship between data sheet, silicon, and product revisions. This data sheet applies to silicon revision 2 (0010b) as shown below.

**Table 1.** Conformity Table

| Product Revision <sup>1</sup>                                                                                                                                                                       | Silicon Revision <sup>2</sup> | Data Sheet Revision |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|---------------------|
| B0                                                                                                                                                                                                  | Rev 1 (0001b)                 | DS60001734C         |
| B1                                                                                                                                                                                                  | Rev 2 (0010b)                 | DS60001734D         |
| <b>Notes:</b><br>1. The product revision is noted in the package top marking.<br>2. The silicon revision is obtained by reading the Revision field from the Device Identification (DEVID) register. |                               |                     |

### Related Links

[10.2. Package Marking Information](#)

[11.6.6. DEVID](#)

## Table of Contents

|                                                      |    |
|------------------------------------------------------|----|
| Description.....                                     | 1  |
| Conformity.....                                      | 3  |
| 1. Preface.....                                      | 6  |
| 1.1. General Terms.....                              | 6  |
| 1.2. Buffer Types.....                               | 7  |
| 1.3. Register Bit Types.....                         | 7  |
| 1.4. Reference Documents.....                        | 8  |
| 2. Introduction.....                                 | 9  |
| 2.1. General Description.....                        | 9  |
| 2.2. The LAN8650/1 Family.....                       | 10 |
| 2.3. Example Systems.....                            | 11 |
| 3. Pin Descriptions and Assignments.....             | 13 |
| 3.1. LAN8650 Pin Assignments.....                    | 13 |
| 3.2. LAN8651 Pin Assignments.....                    | 15 |
| 3.3. Pin Descriptions.....                           | 17 |
| 3.4. Configurable DIO Pins.....                      | 19 |
| 4. Global Functional Descriptions.....               | 20 |
| 4.1. Reset and Startup.....                          | 20 |
| 4.2. Clock Manager.....                              | 23 |
| 4.3. Interrupt Sources.....                          | 23 |
| 4.4. Sleep Mode.....                                 | 24 |
| 4.5. Synchronization Support.....                    | 30 |
| 4.6. Safety Features.....                            | 39 |
| 5. Serial Peripheral Interface (SPI).....            | 50 |
| 5.1. SPI Format.....                                 | 50 |
| 5.2. MAC Frame Data Transactions.....                | 50 |
| 5.3. Control Transactions.....                       | 58 |
| 6. Ethernet MAC.....                                 | 61 |
| 6.1. Description.....                                | 61 |
| 6.2. Embedded Characteristics.....                   | 61 |
| 6.3. Block Diagram.....                              | 61 |
| 6.4. Functional Description.....                     | 61 |
| 6.5. Programming Interface.....                      | 66 |
| 7. Integrated PHY.....                               | 69 |
| 7.1. Interrupt Management.....                       | 69 |
| 7.2. Physical Layer Collision Avoidance (PLCA).....  | 69 |
| 7.3. Application Controlled Media Access (ACMA)..... | 73 |
| 7.4. Credit Based Traffic Shaping.....               | 74 |
| 7.5. Signal Quality Indicator (SQI).....             | 76 |
| 7.6. Cable Fault Diagnostics.....                    | 78 |

|                                                                |     |
|----------------------------------------------------------------|-----|
| 8. Application Information.....                                | 79  |
| 8.1. SPI Connectivity.....                                     | 79  |
| 8.2. System Configuration without Sleep Mode.....              | 79  |
| 8.3. Power Connectivity.....                                   | 80  |
| 8.4. Electromagnetic Compatibility (EMC) Considerations.....   | 84  |
| 8.5. PLCA Collision Detection.....                             | 85  |
| 8.6. Crystal Oscillator Selection.....                         | 86  |
| 8.7. Reference Schematics.....                                 | 86  |
| 9. Operational Characteristics.....                            | 91  |
| 9.1. Absolute Maximum Ratings.....                             | 91  |
| 9.2. Operating Conditions.....                                 | 92  |
| 9.3. Power Consumption.....                                    | 93  |
| 9.4. Package Thermal Specifications.....                       | 94  |
| 9.5. DC Specifications (other than 10BASE-T1S PMA).....        | 94  |
| 9.6. AC Specifications.....                                    | 95  |
| 9.7. Crystal Specifications.....                               | 103 |
| 10. Packaging Information.....                                 | 104 |
| 10.1. 32-VQFN.....                                             | 104 |
| 10.2. Package Marking Information.....                         | 107 |
| 11. Register Descriptions.....                                 | 108 |
| 11.1. Open Alliance 10BASE-T1x MAC-PHY Standard Registers..... | 109 |
| 11.2. MAC Registers.....                                       | 147 |
| 11.3. PHY PCS Registers.....                                   | 191 |
| 11.4. PHY PMA/PMD Registers.....                               | 196 |
| 11.5. PHY Vendor Specific Registers.....                       | 203 |
| 11.6. Miscellaneous Register Descriptions.....                 | 273 |
| 12. Data Sheet Revision History.....                           | 347 |
| Microchip Information.....                                     | 348 |
| The Microchip Website.....                                     | 348 |
| Product Change Notification Service.....                       | 348 |
| Customer Support.....                                          | 348 |
| Product Identification System.....                             | 349 |
| Microchip Devices Code Protection Feature.....                 | 350 |
| Legal Notice.....                                              | 350 |
| Trademarks.....                                                | 350 |
| Quality Management System.....                                 | 351 |
| Worldwide Sales and Service.....                               | 352 |

# 1. Preface

## 1.1 General Terms

**Table 1-1.** General Terms

| Term       | Description                                                                                                                  |
|------------|------------------------------------------------------------------------------------------------------------------------------|
| 10BASE-T   | 10 Mbit/s Ethernet over twisted pair, IEEE Std 802.3™ Clause 14                                                              |
| 10BASE-T1L | 10 Mbit/s Ethernet over long-reach single pair of conductors, IEEE Std 802.3 Clause 146                                      |
| 10BASE-T1S | 10 Mbit/s Ethernet over short-reach single pair of conductors, IEEE Std 802.3 Clause 147                                     |
| ACMA       | Application Controlled Media Access                                                                                          |
| CSMA/CD    | Carrier Sense Multiple Access with Collision Detection                                                                       |
| CSR        | Control and Status Register                                                                                                  |
| BT         | Bit Time, 100 ns for 10 Mbps Ethernet                                                                                        |
| LDO        | Low Dropout Regulator                                                                                                        |
| MAC        | Media Access Controller                                                                                                      |
| MDI        | Medium Dependent Interface                                                                                                   |
| MII        | Media Independent Interface, IEEE Std 802.3 Clause 22                                                                        |
| PCS        | Physical Coding Sublayer                                                                                                     |
| PLCA       | Physical Layer Collision Avoidance, IEEE Std 802.3 Clause 148                                                                |
| PMA        | Physical Medium Attachment sublayer                                                                                          |
| PMD        | Physical Medium Dependent sublayer                                                                                           |
| POR        | Power-on Reset                                                                                                               |
| RS         | Reconciliation Sublayer                                                                                                      |
| SFD        | Start-of-Frame Delimiter. This is the 8-bit value indicating the end of the preamble and the beginning of an Ethernet frame. |
| SPI        | Serial Peripheral Interface                                                                                                  |
| SQI        | Signal Quality Indicator                                                                                                     |
| STA        | Station management entity                                                                                                    |
| TSSI       | Time Synchronization Service Interface, IEEE Std 802.3 Clause 90                                                             |

## 1.2 Buffer Types

**Table 1-2.** LAN8650/1 Buffer Type Descriptions

| Buffer     | Description                                                                                                                                                                                                                                                                        |
|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AI         | Analog input                                                                                                                                                                                                                                                                       |
| AIO        | Analog bi-directional                                                                                                                                                                                                                                                              |
| ICLK       | Crystal oscillator input                                                                                                                                                                                                                                                           |
| OCLK       | Crystal oscillator output                                                                                                                                                                                                                                                          |
| PU         | 55k $\Omega$ (typical) internal pull-up.<br>Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added. |
| VI-VDDAU   | 3.3V input (VDDAU continuous power domain)                                                                                                                                                                                                                                         |
| VIS-VDDP   | 3.3V Schmitt-triggered input (VDDP power domain)                                                                                                                                                                                                                                   |
| VO-VDDP    | 3.3V output with configurable output drive (VDDP power domain)                                                                                                                                                                                                                     |
| VOH-VDDP   | 3.3V high-speed output with configurable output drive (VDDP power domain)                                                                                                                                                                                                          |
| VODL-VDDP  | 3.3V N-channel open-drain sink output drive (VDDP power domain)                                                                                                                                                                                                                    |
| VODH-VDDAU | 3.3V P-channel open-drain source output drive (VDDAU power domain)                                                                                                                                                                                                                 |

**Note:** Digital signals are not 5V tolerant.

## 1.3 Register Bit Types

The following table describes the register bit attributes used throughout this document.

**Table 1-3.** Register Bit Types

| Register Bit Type Notation | Register Bit Description                                                                                                                                                                           |
|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R                          | <b>Read:</b> A register or bit with this attribute can be read.                                                                                                                                    |
| W                          | <b>Write:</b> A register or bit with this attribute can be written.                                                                                                                                |
| RO                         | <b>Read Only:</b> A register or bit with this attribute is read only; writing has no effect.                                                                                                       |
| WO                         | <b>Write Only:</b> If a register or bit is write-only, reads will return unspecified data.                                                                                                         |
| W1S                        | <b>Write One to Set:</b> Writing a one sets the value. Writing a zero has no effect.                                                                                                               |
| W1C                        | <b>Write One to Clear:</b> Writing a one clears the value. Writing a zero has no effect.                                                                                                           |
| RC                         | <b>Read to Clear:</b> Content is cleared after the read. Writes have no effect.                                                                                                                    |
| SC                         | <b>Self Clearing:</b> A bit with this attribute will be cleared to '0' after being written as '1'. Hardware often clears such bits following the completion of some action initiated by the write. |
| NASR                       | <b>Not Affected by Software Reset:</b> The state of NASR bits do not change on assertion of a software reset.                                                                                      |

Many of these register bit notations can be combined. Some examples of this are:

- R/W: Can be written. Will return current setting on a read.
- R/W SC: Bit is readable. When set, it will automatically be cleared by hardware once some action is complete.
- R/W1C: Bit is readable. Write a '1' to this bit to clear.

## 1.4 Reference Documents

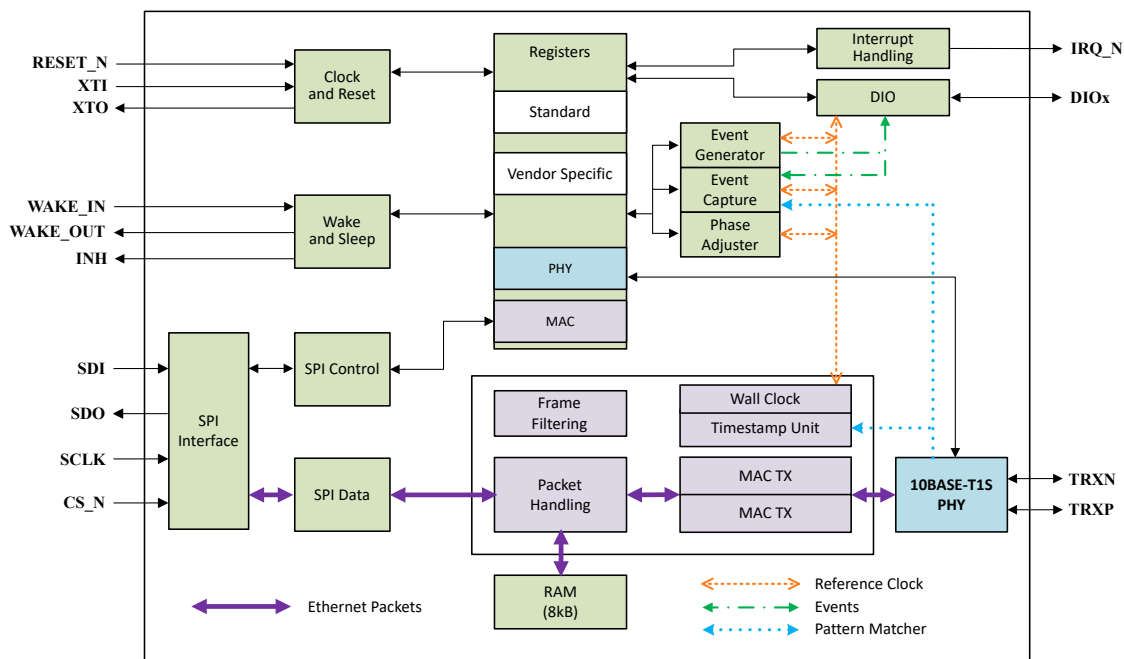
1. IEEE Std 802.3cg™-2019, IEEE Standard for Ethernet, Amendment 5: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors.  
[standards.ieee.org/standard/802\\_3cg-2019.html](https://standards.ieee.org/standard/802_3cg-2019.html)
2. IEEE Std 802.3™-2018, IEEE Standard for Ethernet.  
[standards.ieee.org/standard/802\\_3-2018.html](https://standards.ieee.org/standard/802_3-2018.html)
3. IEEE Std 1588™-2008, IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems.  
[standards.ieee.org/standard/1588-2008.html](https://standards.ieee.org/standard/1588-2008.html)
4. IEEE Std 802.1AS™-2011, IEEE Standard for Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks.  
[standards.ieee.org/standard/802\\_1AS-2011.html](https://standards.ieee.org/standard/802_1AS-2011.html)
5. Microchip, LAN86xx Bus Interface Network (BIN) Reference Design Application Note, DS60001718, Microchip  
[www.microchip.com/DS60001718](http://www.microchip.com/DS60001718)
6. Microchip, LAN8650/1 Configuration Application Note, DS60001760.  
[www.microchip.com/DS60001760](http://www.microchip.com/DS60001760)
7. OPEN Alliance, 10BASE-T1x MAC-PHY Serial Interface, Version 1.1.  
[opensig.org/about/specifications/](http://opensig.org/about/specifications/)
8. OPEN Alliance, 10BASE-T1S Implementation Specification.  
[opensig.org/about/specifications/](http://opensig.org/about/specifications/)
9. OPEN Alliance, Advanced Diagnostic Features for 10BASE-T1S Automotive Ethernet PHYs.  
[opensig.org/about/specifications/](http://opensig.org/about/specifications/)
10. OPEN Alliance, 10BASE-T1S Sleep/Wake-up Specification.  
[opensig.org/about/specifications/](http://opensig.org/about/specifications/)



## 2.1 General Description

The Microchip LAN8650/1 is a 32-pin, stand-alone Ethernet Controller which includes a 10BASE-T1S Ethernet physical layer transceiver (PHY), a Medium Access Controller (MAC) and an industry standard Serial Peripheral Interface (SPI) to enable low-cost microcontrollers to support standard networking software stacks over one inexpensive balanced pair of conductors. A block diagram is shown below.

### Figure 2-1. Block Diagram



The 10BASE-T1S PHY is designed according to the IEEE Std 802.3cg™-2019 specification and provides 10 Mbit/s half-duplex transmit and receive capability over a single balanced pair of conductors such as Unshielded Twisted Pair (UTP) cable. It allows for the creation of both half-duplex multidrop and point-to-point network topologies. Point-to-point link segments of up to at least 15m in length are supported. The multidrop mode can support up to at least 8 nodes on one mixing segment, which can be up to at least 25m long. The ability to connect multiple PHYs to a common mixing segment reduces weight and implementation costs by reducing cabling, connectors and switch ports.

The LAN8650/1 includes an Ethernet MAC to enable low-cost microcontrollers to communicate over 10BASE-T1S via an ordinary SPI interface; there is no need for an on-chip MAC or a high pin count MII. The MAC is 802.3 compliant and includes frame filtering to limit incoming packets.

A host microcontroller communicates with the MAC using a SPI port, according to the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification, which describes not only transfer of Ethernet data, but also configuration and management of control and status registers. The LAN8650/1 can accommodate a SPI clock of up to 25 MHz. The host controller can receive an interrupt from the LAN8650/1 or trigger a reset via the reset pin.

Access to the physical medium is managed by CSMA/CD and optionally supplemented by Physical Layer Collision Avoidance (PLCA) in which the LAN8650/1 may be configured with up to 9 transmit

opportunities in each bus cycle. Additionally, Application Controlled Media Access (ACMA) allows implementation of time-division multiple access (TDMA) to the physical media.

Microchip's LAN8650/1 EtherGREEN energy efficient technology provides low power 10BASE-T1S PHY operation along with an ultra-low power sleep mode with flexible wake options.

Advanced PHY diagnostics are provided, which enable troubleshooting and monitoring capabilities such as cable defect detection of shorts or opens, a receiver Signal Quality Indicator (SQI), PLCA diagnostics, over-temperature, under-voltage detection, comprehensive status interrupt support, and various loopback and test modes.

In addition, the LAN8650/1 can be used to implement high-precision clock synchronization. This enables implementation of the IEEE Std 802.1AS profile, among others, of IEEE Std 1588 for applications utilizing AVB or other Time Sensitive Networking (TSN) standards.

An internal timestamp wallclock enables time stamping frame ingress and egress as described in the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification. This clock can be used for time stamping external events or for generating synchronized pulses using the internal event generator. The device also contains a phase adjuster, which enables smoother clock adjustments with fewer controller write accesses. The reference clock can either be derived from the local crystal or provided by an external source.

The LAN8650/1 is designed to be used in ISO 26262 Functional Safety applications. A Functional Safety Package is available, including Safety Manual; Failure Modes, Effects, and Diagnostic Analysis (FMEDA); and Dependent Failure Analysis (DFA). Please contact Microchip support for additional information.

The LAN8651 includes an integrated low-dropout (LDO) regulator to simplify designs where only 3.3V supplies are available.

## 2.2 The LAN8650/1 Family

The Microchip LAN8650/1 family includes the following devices:

- LAN8650
- LAN8651

Device specific features that do not pertain to the entire LAN8650/1 family are called out independently throughout this document. [Table 2-1](#) below provides a summary of the feature differences between family members.

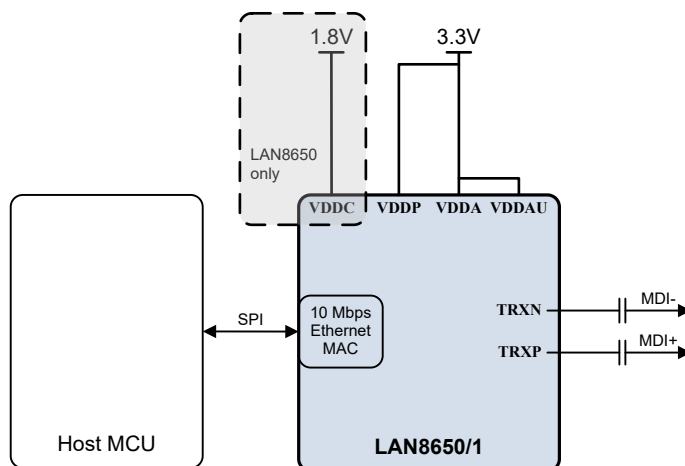
**Table 2-1.** LAN8650/1 Family Feature Matrix

| Part Number | Package | SPI Support | Integrated 1.8V LDO | PLCA Support | ACMA Support | IEEE 802.1AS / TSSI Support | INH Pin Support | WAKE_IN Pin Support | WAKE_OUT Pin Support | AEC-Q100 -40° to +125°C |
|-------------|---------|-------------|---------------------|--------------|--------------|-----------------------------|-----------------|---------------------|----------------------|-------------------------|
| LAN8650     | 32-VQFN | ✓           |                     | ✓            | ✓            | ✓                           | ✓               | ✓                   | ✓                    | ✓                       |
| LAN8651     | 32-VQFN | ✓           | ✓                   | ✓            | ✓            | ✓                           | ✓               | ✓                   | ✓                    | ✓                       |

## 2.3 Example Systems

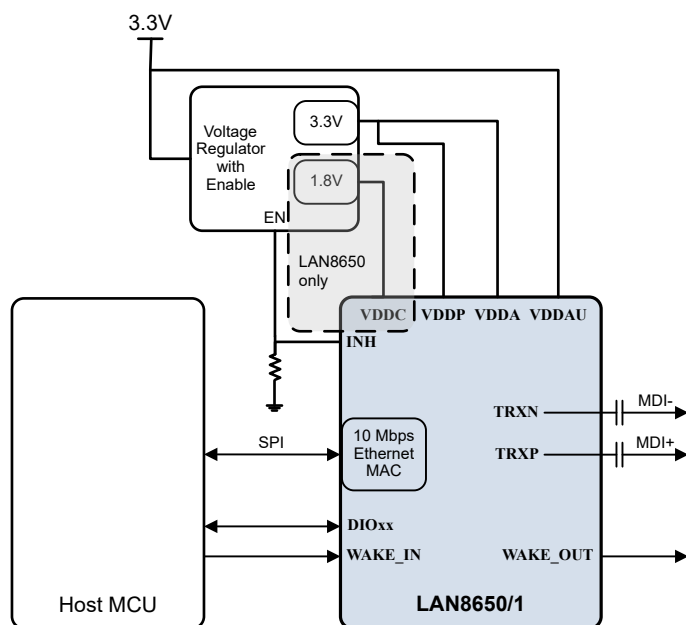
A simple system-level block diagram for the LAN8650/1 is shown in [Figure 2-2](#), below. This system does not use sleep mode, so VDDA and VDDAU can be treated as the same supply and VDDP must only be properly isolated from the analog supplies. When using the LAN8651 which has an internal voltage regulator, no external 1.8V supply is needed.

**Figure 2-2.** Simple System Using LAN8650/1



[Figure 2-3](#) shows a system which is designed to use the low power sleep mode so the constant voltage supply VDDAU is separate from the other voltage supplies. VDDA and VDDP will be disabled in sleep mode as is the 1.8V supply, required when using the LAN8650. In this particular system, the host will initiate sleep mode and then ensure that all inputs to the LAN8650/1 are high-impedance. In a system where external power supplies are required to remain active while other devices shut down, the LAN8650/1 can drive the INH pin for a programmable delay period before entering sleep mode. In this example, the host will bring the LAN8650/1 out of sleep using WAKE\_IN and other devices can then be awakened via WAKE\_OUT. The advanced features available on the DIO pins are also available to the host microcontroller in this system.

**Figure 2-3.** System with Sleep Mode and Advanced Features Using LAN8650/1



### 3. Pin Descriptions and Assignments

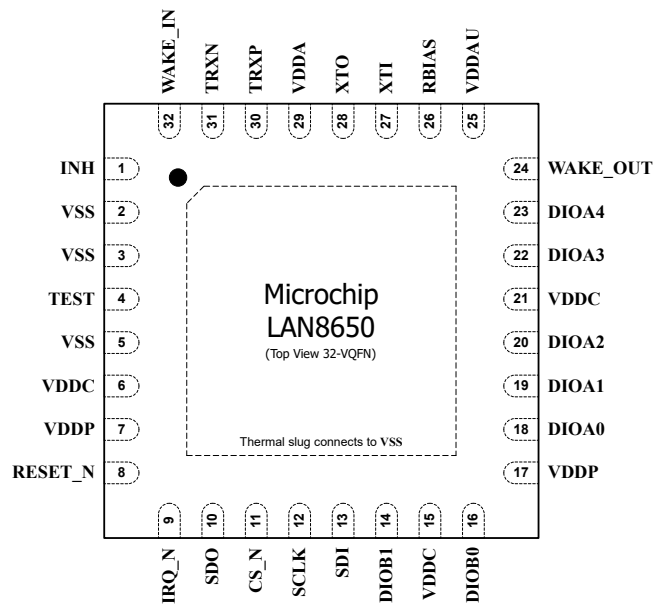
The pin assignments for the LAN8650/1 are detailed in the following sections. Pin descriptions are detailed in the Pin Descriptions section. Pin buffer type definitions are provided in the Buffer Types section.

#### Related Links

- [1.2. Buffer Types](#)
- [3.3. Pin Descriptions](#)

#### 3.1 LAN8650 Pin Assignments

Figure 3-1. LAN8650 32-VQFN Pin Assignments



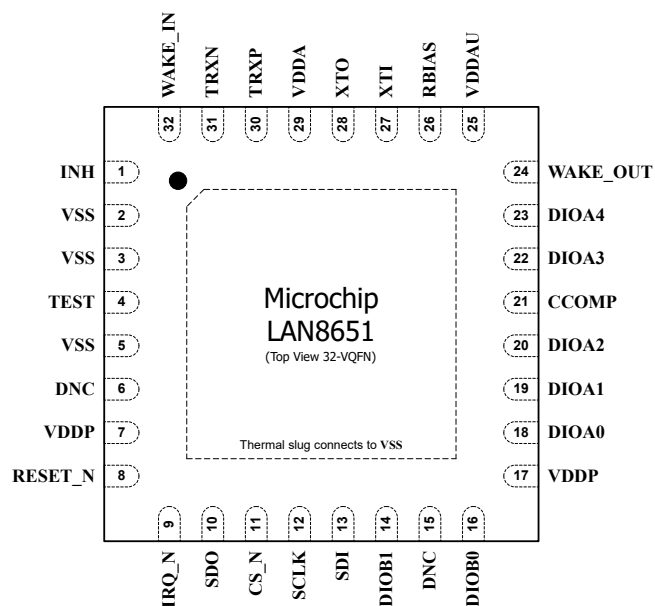
**Note:** Exposed pad (VSS) on bottom of package must be connected to ground.

**Table 3-1.** LAN8650 32-VQFN Pin Assignments

| Pin Num                                        | Pin Name | Pin Num | Pin Name |
|------------------------------------------------|----------|---------|----------|
| 1                                              | INH      | 17      | VDDP     |
| 2                                              | VSS      | 18      | DIOA0    |
| 3                                              | VSS      | 19      | DIOA1    |
| 4                                              | TEST     | 20      | DIOA2    |
| 5                                              | VSS      | 21      | VDDC     |
| 6                                              | VDDC     | 22      | DIOA3    |
| 7                                              | VDDP     | 23      | DIOA4    |
| 8                                              | RESET_N  | 24      | WAKE_OUT |
| 9                                              | IRQ_N    | 25      | VDDAU    |
| 10                                             | SDO      | 26      | RBIAS    |
| 11                                             | CS_N     | 27      | XTI      |
| 12                                             | SCLK     | 28      | XTO      |
| 13                                             | SDI      | 29      | VDDA     |
| 14                                             | DIOB1    | 30      | TRXP     |
| 15                                             | VDDC     | 31      | TRXN     |
| 16                                             | DIOB0    | 32      | WAKE_IN  |
| Exposed Pad (VSS) must be connected to ground. |          |         |          |

## 3.2 LAN8651 Pin Assignments

Figure 3-2. LAN8651 32-VQFN Pin Assignments



**Note:** Exposed pad (VSS) on bottom of package must be connected to ground.

**Table 3-2.** LAN8651 32-VQFN Pin Assignments

| Pin Num                                        | Pin Name | Pin Num | Pin Name |
|------------------------------------------------|----------|---------|----------|
| 1                                              | INH      | 17      | VDDP     |
| 2                                              | VSS      | 18      | DIOA0    |
| 3                                              | VSS      | 19      | DIOA1    |
| 4                                              | TEST     | 20      | DIOA2    |
| 5                                              | VSS      | 21      | CCOMP    |
| 6                                              | DNC      | 22      | DIOA3    |
| 7                                              | VDDP     | 23      | DIOA4    |
| 8                                              | RESET_N  | 24      | WAKE_OUT |
| 9                                              | IRQ_N    | 25      | VDDAU    |
| 10                                             | SDO      | 26      | RBIAS    |
| 11                                             | CS_N     | 27      | XTI      |
| 12                                             | SCLK     | 28      | XTO      |
| 13                                             | SDI      | 29      | VDDA     |
| 14                                             | DIOB1    | 30      | TRXP     |
| 15                                             | DNC      | 31      | TRXN     |
| 16                                             | DIOB0    | 32      | WAKE_IN  |
| Exposed Pad (VSS) must be connected to ground. |          |         |          |



### 3.3 Pin Descriptions

This section contains descriptions of the various LAN8650/1 pins. The “\_N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, RESET\_N indicates that the reset signal is active low. When “\_N” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

**Table 3-3.** Serial Peripheral Interface (SPI) Pins

| Name               | Symbol | Buffer Type   | Description                                                                                                                                      |
|--------------------|--------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Serial Clock       | SCLK   | VIS-VDDP      | Serial clock input                                                                                                                               |
| Serial Data In     | SDI    | VIS-VDDP      | Serial data input                                                                                                                                |
| Serial Data Out    | SDO    | VOH-VDDP      | Serial data output                                                                                                                               |
| Serial Chip Select | CS_N   | VIS-VDDP (PU) | Serial peripheral chip select                                                                                                                    |
| Interrupt          | IRQ_N  | VO-VDDP (PU)  | Device interrupt (Active low)<br><b>Note:</b> In some cases, the host controllers may require a 10 kΩ (typical) pull-up to its I/O power supply. |

**Table 3-4.** Ethernet Transceiver Pins

| Name                             | Symbol | Buffer Type | Description                                   |
|----------------------------------|--------|-------------|-----------------------------------------------|
| Ethernet TX/RX Positive Terminal | TRXP   | AIO         | Positive terminal for transmit/receive signal |
| Ethernet TX/RX Negative Terminal | TRXN   | AIO         | Negative terminal for transmit/receive signal |

**Table 3-5.** Power Management Pins

| Name       | Symbol  | Buffer Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------|---------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Inhibit    | INH     | VODH-VDDAU  | Inhibit. Used to switch on/off the main external voltage regulators.<br>This pin operates in the VDDAU domain.<br>RESET_N assertion does not affect the state of this pin.<br>This signal is an active high, P-channel open-drain source output. The pin will be driven to VDDAU to inhibit the shutdown of external voltage regulators. When the external regulators may be shutdown, this pin will become high impedance.<br><b>Note:</b> When used, this pin requires a pull-down resistor.<br>When not used, this pin should be left unconnected. |
| Wake Input | WAKE_IN | VI-VDDAU    | Wakeup Input. Asserted to move the part out of sleep. This pin implements the optional wake input described in the TC10 specification.<br><b>Note:</b> When used, this pin requires a pull-up or pull-down resistor, depending on the software configured assertion polarity.<br><b>Note:</b> This pin operates in the VDDAU domain.<br>When not used, this pin should be connected to VSS.                                                                                                                                                           |

.....continued

| Name        | Symbol   | Buffer Type | Description                                                                                                                                                                                                                                                                                                               |
|-------------|----------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Wake Output | WAKE_OUT | VO-VDDP     | Wake Output. Asserted when the part wakes out of sleep. This pin implements the optional wake output described in the TC10 specification.<br><b>Note:</b> When used, this pin requires a pull-down resistor.<br><b>Note:</b> This pin operates in the VDDP domain.<br>When not used, this pin should be left unconnected. |

**Table 3-6.** Configurable Pins

| Name                                                                                                                                                                                                                         | Symbol                                             | Buffer Type       | Description                                                                                                                          |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------|
|  Reserved bits of the pad control register must not be written with any values other than their default without instruction from Microchip. |                                                    |                   |                                                                                                                                      |
| Configurable Pins                                                                                                                                                                                                            | DIOA0<br>DIOA1<br>DIOA2<br>DIOA3<br>DIOA4<br>DIOB0 | VIS-VDDP, VO-VDDP | These pins may be configured as input or output for various purposes. When not used, these pins may be connected directly to ground. |
| Reserved                                                                                                                                                                                                                     | DIOB1                                              |                   | This pin is reserved for Microchip test use. It is recommended that this pin is connected directly to ground.                        |

**Table 3-7.** Miscellaneous Pins

| Name                           | Symbol  | Buffer Type | Description                                                                                                                                                                                                             |
|--------------------------------|---------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| External 25 MHz Crystal Input  | XTI     | ICLK        | External 25 MHz crystal input                                                                                                                                                                                           |
| External 25 MHz Crystal Output | XTO     | OCLK        | External 25 MHz crystal output                                                                                                                                                                                          |
| System Reset                   | RESET_N | VIS-VDDP    | System reset. This pin is active low. When not used, this pin may be connected directly to VDDP.                                                                                                                        |
| Bias Resistor                  | RBIAS   | AI          | External bias resistor connection pin. This pin requires connection of a 12.4 kΩ resistor to ground.<br><b>Note:</b> The resistor must be within ± 1% tolerance across the entire expected operating temperature range. |
| Reserved for Test              | TEST    | VIS-VDDP    | This pin should be connected to VDDP.                                                                                                                                                                                   |
| Do Not Connect                 | DNC     | -           | The pin must be left floating externally unless otherwise directed by Microchip.                                                                                                                                        |

**Table 3-8.** Power Pins

| Name                                     | Symbol | Description                                                                                                                                                                 |
|------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Core LDO Supply Compensation             | CCOMP  | Internal +1.8V LDO core compensation<br><b>Note:</b> This pin requires a 4.7 μF low ESR capacitor to the PCB ground plane.<br><b>Note:</b> This pin is only on the LAN8651. |
| +1.8V Switchable Core Power Supply Input | VDDC   | +1.8V core power supply input. When in sleep mode, this supply must be disabled.<br><b>Note:</b> These pins are only on the LAN8650.                                        |

| .....continued                             |        |                                                                                                                                                                                                                   |
|--------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name                                       | Symbol | Description                                                                                                                                                                                                       |
| +3.3V Switchable I/O Power Supply Input    | VDDP   | +3.3V I/O power supply input. When in sleep mode, this supply must be disabled.                                                                                                                                   |
| +3.3V Continuous VDDAU Power Supply Input  | VDDAU  | +3.3V continuous VDDAU power supply input.<br><b>Note:</b> This supply must be provided during sleep mode.<br><b>Note:</b> When wake/sleep support is not used, this pin is connected to the same supply as VDDA. |
| +3.3V Switchable Analog Power Supply Input | VDDA   | +3.3V analog power supply input. When in sleep mode, this supply must be disabled.                                                                                                                                |
| Ground                                     | VSS    | Common ground<br><b>Note:</b> The exposed pad must be connected to the ground plane with a via array.                                                                                                             |

### 3.4 Configurable DIO Pins

The digital IO pins (DIO) are pins which can be configured to enable additional features. The available options are summarized in the table below and can be selected in the Pad Control register. The default configuration of each pin is indicated with **bold** text. All of the default configurations permit unused pins to be wired directly to ground.

**Note:**

In order to use any functions that can be selected over these pins, the function must be configured in other registers. See the appropriate section for the desired function for additional details.

**Table 3-9.** Configurable Pin Functions

| Pin Name | Direction     | Description                            |
|----------|---------------|----------------------------------------|
| DIOA0    | <b>Input</b>  | <b>Event Capture</b>                   |
|          | Output        | Event Generator 0                      |
| DIOA1    | <b>Input</b>  | <b>Event Capture</b>                   |
|          | Output        | Event Generator 1                      |
| DIOA2    | <b>Input</b>  | <b>ACMA or Event Capture</b>           |
|          | Output        | Event Generator 2                      |
| DIOA3    | <b>Input</b>  | <b>Event Capture</b>                   |
|          | Output        | Event Generator 3                      |
| DIOA4    | <b>Input</b>  | <b>Reserved for Microchip test use</b> |
|          | Output        | One Pulse-per-second Signal            |
|          | Output        | Event Generator 2                      |
|          | Output        | Event Generator 3                      |
| DIOB0    | Input         | Synchronization Reference Clock        |
|          | <b>Output</b> | <b>Reference Clock Out</b>             |

## 4. Global Functional Descriptions

The following sections provide detailed information on functions, such as reset, power management and clock management, that affect the device as a whole. Features that are specific to the SPI, MAC, or PHY blocks are described in later chapters.

### 4.1 Reset and Startup

After the LAN8650/1 leaves reset, it must be configured before it can be used to transmit and receive data over the 10BASE-T1S MDI. This section describes the various reset modes and the startup sequence.

#### 4.1.1 Resets

The device provides the chip-level reset sources described in the following sections.

##### 4.1.1.1 Power-On Reset (POR)

A Power-On Reset occurs when power is initially applied to the device, or if any power supply drops below a falling threshold. The device will remain in reset until all power supplies have passed the appropriate rising threshold, and the LAN8650/1 is fully operational. The IRQ\_N pin will be asserted and the RESETC (Reset Completed) bit of the OA\_STATUS0 Register will be set to 1, as specified by the Open Alliance. This indicates to the station controller that the device has been reset and requires configuration. The rising and falling thresholds are listed below in [Table 4-1](#).

For more information about waking from low-power sleep mode, see the Sleep Mode Section of this document.

**Table 4-1.** POR Supply Thresholds

| Supply            | Rising Threshold <sup>1</sup> | Falling Threshold <sup>1</sup> |
|-------------------|-------------------------------|--------------------------------|
| VDDAU             | 2.5V                          | 2.3V                           |
| VDDA              | 2.5V                          | 2.3V                           |
| VDDP              | 1.9V                          | 1.9V                           |
| VDDC <sup>2</sup> | 1.5V                          | 1.4V                           |

**Notes:**

1. Rising and falling threshold voltages are design parameters and are neither tested nor characterized.
2. The LAN8651 internal 1.8V supply may be monitored externally at the CCOMP pin.

#### Related Links

[11.1.6. OA\\_STATUS0](#)

[4.4. Sleep Mode](#)

##### 4.1.1.2 External Pin Reset (RESET\_N)

A hardware reset will occur when the RESET\_N pin is asserted. Once the RESET\_N input is deasserted, the LAN8650/1 will restart operation. The device will indicate to the station's controller that it has been reset and must be configured in the same way as if a Power-On Reset had occurred: the IRQ\_N pin will be asserted and the RESETC (Reset Completed) bit of the OA\_STATUS Register will be set to 1.

The RESET\_N pin must be connected externally to VDDP if unused. If used, the RESET\_N pin must be driven for a minimum period as defined in the RESET\_N Timing section.

#### Related Links

[11.1.6. OA\\_STATUS0](#)

[9.6.3. RESET\\_N Timing](#)

#### 4.1.1.3 Software Reset

A software reset of the LAN8650/1 is available via the Soft Reset (SW\_RESET) bit in the standard OA\_CONFIG0 register.

**Note:** The SW\_RESET bit of the Clause 22 Basic Control register will reset only the internal PHY, not the entire device. This PHY only reset is not recommended for use. If such a reset is detected, by reading the RESETC bit of the STS2 register, reset the entire device.

##### Related Links

[11.1.5. OA\\_CONFIG0](#)

[11.1.17. BASIC\\_CONTROL](#)

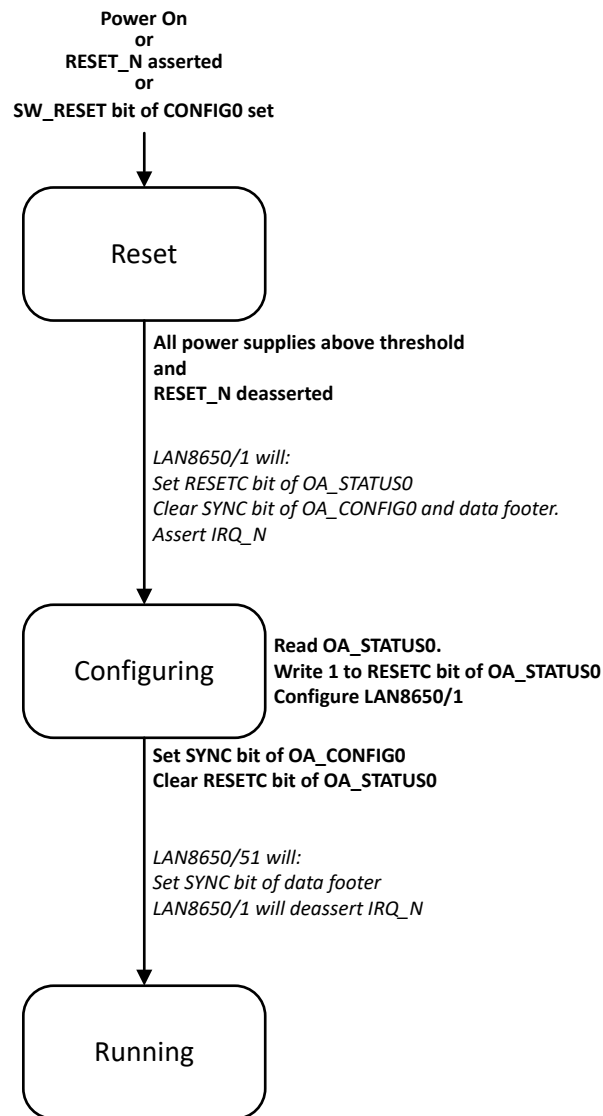
[11.5.3. STS2](#)

#### 4.1.2 Startup Sequence

After a reset, the LAN8650/1 indicates to the host that a reset has occurred by asserting the IRQ\_N pin, and setting the RESETC bit of the OA\_STATUS0 register. The device is now ready to be configured by the host controller before it can be used to transmit and receive data. When the host accesses the LAN8650/1 via SPI, it will also see that the SYNC bit of the OA\_CONFIG0 register and of the data footer are cleared.

Once the host reads the OA\_STATUS0, and determines that the cause of the interrupt was a reset, it should configure the LAN8650/1. As part of this configuration, there are two bits that must be written: the SYNC bit of the OA\_CONFIG0 register must be set to indicate that the device is configured and ready to transmit and the RESETC bit of the OA\_STATUS0 must be cleared so that IRQ\_N line will stop asserting.

**Figure 4-1.** LAN8650/1 Startup and Configuration Sequence



The latest recommended startup configuration can be found in the [LAN8650/1 Configuration Application Note AN1760](#). Additional details for customizing use of the MAC can be found in the Initialization section.

#### Related Links

[1.4. Reference Documents](#)

[6.5.1. Initialization](#)

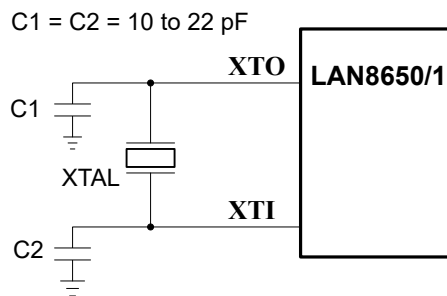
## 4.2 Clock Manager

The Clock Manager generates the internal clocks from an external reference source.

### 4.2.1 Crystal Pins (XTI/XTO)

The XTI and XTO crystal oscillator pins are used to connect a 25.0 MHz clock source. The crystal oscillator should be in a fundamental, parallel resonant mode. [Figure 4-2](#) depicts the external circuitry connected to the LAN8650/1 oscillator circuit. Since the internal inverter/amplifier is operated in its linear region, external series resistors should not be used as they will lower the gain and could cause start-up problems. The device contains an internal  $\sim 1\text{ M}\Omega$  resistance in parallel with the crystal amplifier to initiate oscillation, therefore an external resistance between XTO and XTI should not be used. Several factors must be considered when selecting a crystal including load capacitance, oscillator margin, cut, and operating temperature. The crystal frequency must be 25.0 MHz.

**Figure 4-2.** Crystal Oscillator Input



#### Related Links

[9.7. Crystal Specifications](#)

## 4.3 Interrupt Sources

The OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification requires that the interrupt is asserted on the following conditions if the conditions were not already reported in the most recent data footer:

- Receive data available
- Transmit buffer space available
- Extended status bit set

The specification then requires that the SPI controller initiate a data block transaction in order to obtain the current receive data block footer and determine the reason for the interrupt. See the section MAC Frame Receive Data Block Footer for more details on the footer. If the extended status (EXST) bit of the footer is set, the controller should then read the OA\_STATUS0 register and, if needed, the OA\_STATUS1 register to determine which status bit or bits are set.

The Open Alliance specification defines the operation of these registers. The OA\_STATUS0 contains interrupt bits that are defined by the standard, and the SPI host can select which of these bits will cause the extended status bit to be set by modifying the OA\_IMASK0 register.

The OA\_STATUS1 register contains vendor specific sources; its mask register is OA\_IMASK1. This register contains the following bits that can trigger the extended status bit to be set and, if needed an interrupt.

- SEV - This bit is asserted when bits in the Synchronization Event Status (SEVSTS) register are set. Details are available in the Synchronization Support section.

- TTSCMA/B/C - These bits are asserted when the SPI host requested that a timestamp be captured when a packet is transmitted, but the transmit timestamp capture was not triggered.
- TTSCOFAB/C - These bits are asserted when a timestamp was captured for a transmit packet as requested by the SPI host, but the previously captured transmit timestamp had not been read from the associated transmit timestamp capture register. The previously captured transmit timestamp was therefore overwritten and lost.
- UV18 - This bit is asserted when an 1.8V supply under voltage condition is detected. Details are available in the Under Voltage Detection (1.8V Supply) section.
- ECC - This bit is asserted when an SRAM ECC error has been detected. Details are available in the SRAM Error Correction Code (ECC) section.
- BUSER - This bit is asserted when an internal bus error status has been detected. This may be due to an SRAM error or internal bus parity error. Details are in the SRAM Error Correction Code (ECC) and Bus Parity sections.
- FSMSTER - This bit is asserted when an internal state machine has been detected making an invalid transition or transitioning into an invalid state. Details are available in the Internal Fault Detection section.
- TXNER, RXNER - These bits are asserted when a non-recoverable transmit or receive error has occurred. Details are available in the Internal Fault Detection section.

#### Related Links

[5.2.2. MAC Frame Receive Data Block Footer](#)

[11.1.6. OA\\_STATUS0](#)

[11.1.7. OA\\_STATUS1](#)

[11.1.9. OA\\_IMASK0](#)

[11.1.10. OA\\_IMASK1](#)

[4.5.6. Synchronization Events](#)

[4.6.1.1.2. Under Voltage Detection \(1.8V Supply\)](#)

[4.6.2.1. SRAM Error Correction Code \(ECC\)](#)

[4.6.2.2. Bus Parity](#)

[4.6.2. Internal Fault Detection](#)

## 4.4 Sleep Mode

The LAN8650/1 provides an ultra-low power (typically less than 140  $\mu$ W) sleep mode based on the OPEN Alliance TC10 specifications. In this mode, it will release the INH pin to allow shutdown of most external power supplies. Only the uninterrupted supply VDDAU remains active to monitor and react to user selectable wake events. After a wake event, INH is asserted and the remaining power supplies are re-enabled. Since the INH pin can control power supplies shared with other devices, this feature allows for an entire node to enter a low power state, and be awakened by external events.

This section will describe

- how the INH pin can be used to control the shutdown of power supplies, including using a delay feature
- how to select what events will wake the LAN8650/1 from sleep
- how to enter sleep mode, including how to configure activity timeouts, when used
- how the LAN8650/1 will behave upon wake and what actions are required

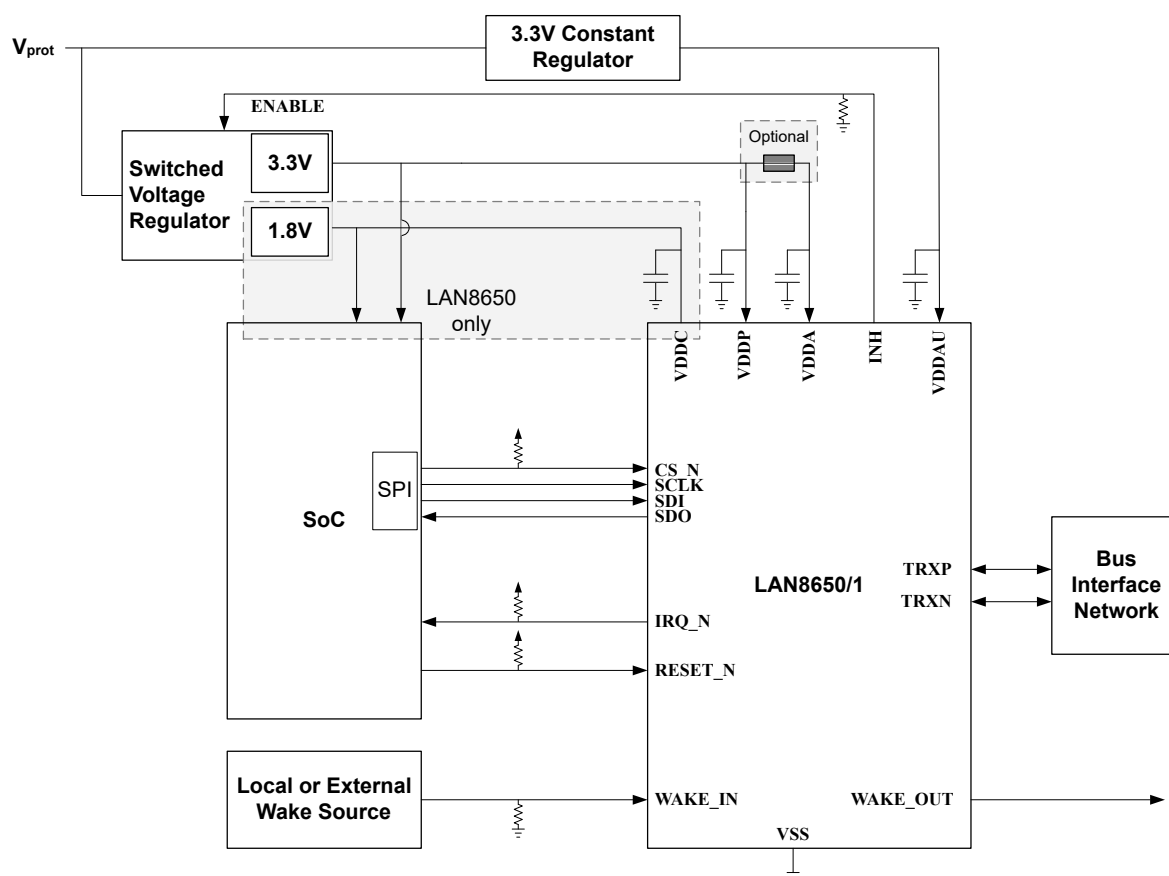
### 4.4.1 Sleep Mode and System Power Management

Figure 4-3 shows an example of how power should be supplied in a system that will use the low-power sleep mode of the LAN8650/1. In this diagram, VDDAU is provided by a constant supply, so that it is always enabled, even during sleep mode. On system power-up, once this supply is active,



the INH pin will be asserted so that its active high output can drive the enable pins of the external switchable supplies for VDDA, VDDP and, for the LAN8650, VDDC.

**Figure 4-3. Sleep Mode Example System**



After the device enters sleep mode, the INH pin will enter a high-impedance state. The external resistor will pull the signal down to ground, which will then disable any voltage sources controlled by INH. This can be used to disable power to additional devices, including, when needed, the station controller.

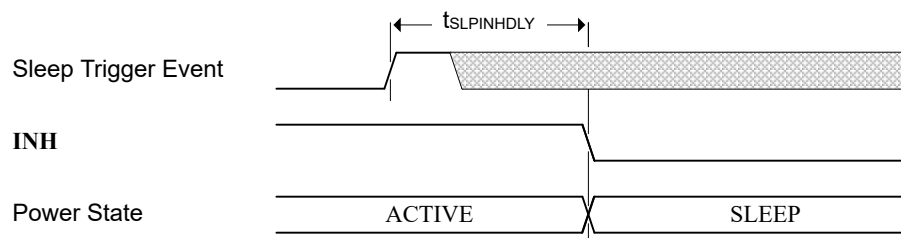


**Important:** Before entering SLEEP mode, the desired wake configuration must be configured in the LAN8650/1. It is recommended that this mode is configured immediately after a reset. Details can be found in the Configuring Wake section.

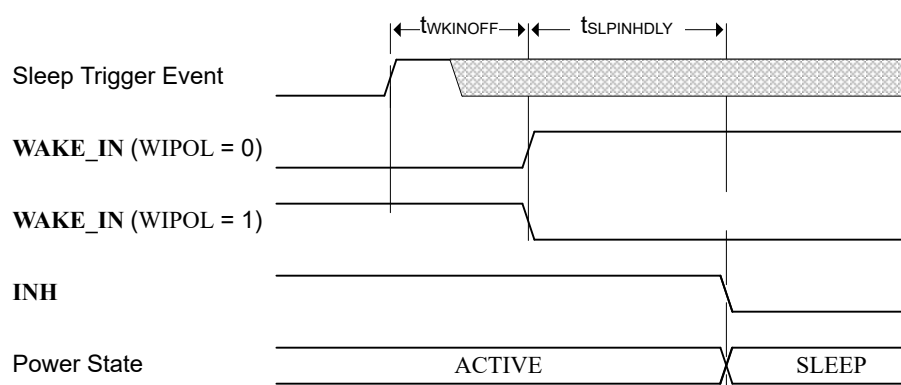
Some systems may require a delay between the trigger for the start of sleep mode and disable of the local power supplies, for example, to allow for other nodes on the mixing segment to go quiet. Delay timing is configured with the Sleep Inhibit Delay (SLPINHDLY) field of the Sleep Control 0 (SLPCTL0) register. If wake from the WAKE\_IN pin is enabled (WKIEN=1), the WAKE\_IN pin must be deasserted before the Sleep Inhibit Delay timer will be started. See [Figure 4-4](#) for a diagram illustrating the timing from when SLEEP state is commanded until the INH pin is released and the SLEEP state is entered.

**Figure 4-4. Sleep Timing**

WKIEN = 0 or **WAKE\_IN** not asserted when sleep triggered



WKIEN = 1 and **WAKE\_IN** asserted when sleep triggered



In sleep mode, a small amount of current is drawn from VDDAU to monitor for a wake condition. The wake condition can be a **WAKE\_IN** pulse provided from another device, or a signal on the wire harness from another node on 10BASE-T1S network. After a wake condition is detected, INH is actively driven high, enabling the external power supplies, which should be fully powered within 1 ms of INH being driven high according to the OPEN Alliance TC10 Wake/Sleep specification. Once all power supplies are above their thresholds, the LAN8650/1 will behave as if it had been reset by the RESET\_N pin, and will assert IRQ\_N to signal that the device is ready to be configured as described in the Startup Sequence section.



**Important:** To achieve maximum power savings and allow TC10 power goals to be met when in the SLEEP state, all power supplies except for VDDAU must be powered down.

#### Related Links

[11.5.49. SLPCTL0](#)

#### 4.4.2 Configuring Wake-up

The sleep/wake module is powered by the externally protected continuous VDDAU supply and detects a wake condition when the device is in the SLEEP state. This module monitors activity energy on the MDI interface and/or wake pulses on the WAKE\_IN pin to determine if the device has received wake-up signaling. Once wake-up signaling has been received and validated, this module will drive the INH pin high to the VDDAU supply to enable the external switched power supplies.

Prior to entering the SLEEP state, the station controller must configure the device to select one or both of these wake methods.

##### 4.4.2.1 MDI Wake-up

The device may be configured to wake from activity on the MDI interface when in the SLEEP state. The device monitors activity energy on TRXP/TRXN. Continuous activity must be detected for a minimum amount of time to ensure that false positive wake events are not caused by impulse noise; this time is documented in the Wake Event Timing section. Once a valid wake event is detected, the INH pin is driven high to the VDDAU supply to re-enable external power supplies and wake the system.

Wake from MDI is enabled by writing a '1' to the MDI Wake Enable (MDIWKEN) bit in the Sleep Control 0 (SLPCTL0) register prior to entering the SLEEP state.

**Note:** In the LAN8650/1, MDI wake detection was not designed to meet the OPEN Alliance 10BASE-T1S Sleep/Wake-up Specification, version 1.0. Received energy that is of sufficient length that is detected either from other nodes transmitting onto the segment or from noise will trigger the device to wake when MDI wake-up is enabled.

#### Related Links

[11.5.49. SLPCTL0](#)

##### 4.4.2.2 WAKE\_IN Pin Wake-up

The device may be configured to wake from SLEEP when a valid pulse on the WAKE\_IN pin is detected. As specified by the OPEN Alliance TC10 Wake/Sleep specification, pulses with durations of less than 10  $\mu$ s are ignored while pulses greater than 40  $\mu$ s in duration are recognized. Recognition of wake pulses between 10  $\mu$ s and 40  $\mu$ s is undefined. After determination of a valid pulse, the INH pin is driven high to the VDDAU supply to re-enable external power supplies and wake the system.

Wake-up from detection of a valid WAKE\_IN pulse must be enabled by writing a '1' to the WAKE\_IN Enable (WKINEN) bit in the Sleep Control 0 (SLPCTL0) register prior to entering the SLEEP state. The assertion level of the detected wake pulse is configured by setting the Wake In Polarity (WIPOL) bit in the Sleep Control 1 (SLPCTL1) register.



**Restriction:** Assertion of the WAKE\_IN pin is only detectable when the device is in the SLEEP state. When awake and in ACTIVE state the device will not detect pulse assertions on the WAKE\_IN pin.



**Important:** When wake from WAKE\_IN is enabled, the device will not enter the SLEEP state while the WAKE\_IN input is asserted. The WAKE\_IN pin must be deasserted before the Sleep Inhibit Delay will occur followed by the INH pin being released and the SLEEP state entered. See Sleep Mode and System Power Management for more details.

#### Related Links

[11.5.49. SLPCTL0](#)

[11.5.50. SLPCTL1](#)

[4.4.1. Sleep Mode and System Power Management](#)

### 4.4.3 Entering Sleep Mode

After wake-up has been configured, the device may at any time be commanded to enter the SLEEP state. This may be done in one of two ways. The station controller may initiate a transition to SLEEP by writing a '1' to the Sleep Enable (SLPEN) bit in the Sleep Control 0 (SLPCTL0) register. Alternatively, the device may be configured to enter SLEEP automatically upon expiration of an inactivity watchdog as detailed below.

#### Related Links

[11.5.49. SLPCTL0](#)

#### 4.4.3.1 Inactivity Watchdog

The device includes an inactivity watchdog timer that can be used to automatically command the device into the SLEEP state. The inactivity watchdog can be used to allow the system to reduce its power consumption when no activity is present on the network. It can also be used to detect when the controller has malfunctions and is no longer managing the device; in this case, the watchdog can be used to force the device into the SLEEP state to prevent the malfunctioning node from consuming power on an inactive network segment.

The inactivity watchdog can be configured to trigger on inactivity of three sources: no receive packets from the network, no transmit packets from the MAC, and no PHY register access by the controller. Each of these three inactivity sources may be enabled separately or together in any combination. Once enabled, the watchdog timer will be reset upon detected activity on any of the selected watchdog sources. When the watchdog expires, the Inactivity Watchdog Timeout (IWDTO) bit in the Status 2 (STS2) register will be set commanding the transition to the SLEEP state and initiating the Sleep Inhibit Delay timer. The Inactivity Watchdog Timeout Interrupt Mask (IWDTOM) bit in the Interrupt Mask 2 (IMSK2) register should be set to assert the PHY Interrupt (PHYINT) status bit in the OPEN Alliance Status 0 (OA\_STATUS0) to immediately notify the station controller when the inactivity watchdog expiration occurs. Once the Inactivity Watchdog Timeout status bit is set, the controller may halt the pending SLEEP transition by clearing the Inactivity Watchdog Timeout status bit any time before the Sleep Inhibit Delay expires.

Before enabling the inactivity watchdog timer, the inactivity sources to be used for resetting the watchdog timer when activity occurs must be configured by setting the appropriate bits within the Port Management 2 (PRTMGMT2) register:

- Network packet receive inactivity - Media Interface Receive Watchdog Enable (MIRXWDEN)
- MAC packet transmit inactivity - Media Interface Transmit Watchdog Enable (MITXWDEN)
- PHY register access inactivity - PHY Register Inactivity Watchdog Enable (PRIWDEN)

The 32-bit Inactivity Watchdog Timeout (TIMEOUT) field in the Inactivity Watchdog Timeout High/Low (IWDTOH/IWDTOL) registers configures how long the enabled inactivity sources must show no activity before the watchdog timer expires. The default setting for the Inactivity Watchdog Timeout yields an inactivity timeout of 2 seconds. When activity is detected on the inactivity sources, the watchdog timer is reset to the value in the TIMEOUT field. The watchdog timer then decrements every 200 ns. Should the watchdog timer decrement to zero, the Inactivity Watchdog Timer expires causing the Inactivity Watchdog Timeout (IWDTO) status bit to become set.

The watchdog is enabled by setting the Inactivity Watchdog Enable (IWDE) bit in the Control 1 (CTRL1) register after configuring the inactivity sources, the watchdog timeout, and enabling the Inactivity Watchdog Timeout Interrupt Mask.

**Related Links**

[11.5.1. CTRL1](#)  
[11.5.3. STS2](#)  
[11.5.6. IMSK2](#)  
[11.5.17. PRTMGMT2](#)  
[11.5.18. IWDT0H](#)  
[11.5.19. IWDTOL](#)  
[11.5.49. SLPCTL0](#)

**4.4.4 Wake-up**

After all of the power supplies of the LAN8650/1 are above thresholds, the device will be in a state similar to a power-on reset; this includes asserting IRQ\_N to indicate that the device is ready for configuration. Unlike a power-on reset, after wake-up two registers will contain information about the wake event, and, if configured, wake forwarding will automatically send wake signals to additional devices. As after any reset, the device must be reconfigured, as described in the section Startup Sequence.

The host controller can identify that the device was powered up from a wake event, by examining the Wake Indication (WAKEIND) bit in the Sleep Control 1 (SLPCTL1) register. This bit will be set to '1' if the device was powered up from a wake event, otherwise it will be '0'. The Wake-up MDI (WKEMDI) and Wake-up WAKE\_IN (WKEWI) status bits in the Status 2 (STS2) register are also set indicating the source of the wake event. Once the device has awakened, it will continue to drive the INH pin high causing the ECU to remain awake until the controller initiates a new transition into the SLEEP state. The device may optionally be configured to forward a received wake event to other devices by driving a wake pulse on WAKE\_OUT and/or activity signaling on the MDI. The device wake/sleep configuration is reset to its default state upon wake-up and must be reconfigured as desired prior to sleeping again.



**Important:** After the LAN8650/1 has awakened, the controller must clear the Wake Indication (WAKEIND) bit to reset the wake activity detector prior to enabling entry into the SLEEP state again. This is accomplished by first writing the Clear Wake Indication (CLRWKI) bit in the Sleep Control 1 register to a '1' followed with a second write back to '0'.

**Related Links**

[11.5.50. SLPCTL1](#)  
[11.5.3. STS2](#)

**4.4.4.1 MDI Wake Forwarding**

The device may be configured to generate activity signaling on the MDI upon wake from SLEEP due to a wake pulse on WAKE\_IN. The wake signaling consists of a 1 ms transmission of differential Manchester encoded pseudo-random binary data. The device will not listen for activity on the network prior to transmitting the wake signaling.

Enabling of MDI wake activity forwarding is accomplished by setting the MDI Forward Enable (MDIFWDEN) bit of the Sleep Control 1 (SLPCTL1) register. Automatic forwarding of WAKE\_IN wake events to the MDI must be configured prior to entering the SLEEP state.

**Note:** MDI wake signaling was not designed to meet the OPEN Alliance 10BASE-T1S Sleep/Wake-up Specification, version 1.0.

**Related Links**

[11.5.50. SLPCTL1](#)

#### 4.4.4.2 WAKE\_OUT Pin Wake Forwarding

The WAKE\_OUT pin may be configured to assert for 90  $\mu$ s upon wake from SLEEP due to MDI activity or a wake pulse on WAKE\_IN. Enabling of WAKE\_OUT pin forwarding is accomplished by setting the WAKE\_OUT Forward Enable (WKOFWDEN) bit of the Sleep Control 1 (SLPCTL1) register prior to entering the SLEEP state. Automatic forwarding of wake events to the WAKE\_OUT pin must be configured prior to entering the SLEEP state.



**Important:** The WAKE\_OUT pin operates from the VDDP power domain and therefore will only be asserted once the external VDDP supply has been powered.

#### Related Links

[11.5.50. SLPCTL1](#)

#### 4.4.4.3 Manual Wake Assertion

While powered up in the ACTIVE state, the station controller may wish to initiate a wake-up event to the network and/or additional devices. This may be accomplished by triggering a manual wake forward event by writing a '1' to the Manual Wake Forward (MWKFWD) bit in the Sleep Control 1 (SLPCTL1) register. Once set, the device will initiate wake activity on the MDI if the MDI Wake Forward Enable (MDIWFWD) bit is set. Additionally, or alternatively, a wake pulse may be initiated to the WAKE\_OUT pin if the WAKE\_OUT Forward Enable (WKOFWDEN) bit is set. Once the wake events have completed, the device will clear the Manual Wake Forward bit.

#### Related Links

[11.5.50. SLPCTL1](#)

### 4.5 Synchronization Support

The LAN8650/1 contains several features to support system synchronization, including time sensitive networking. These features include

- Wall Clock - derives the time from the reference clock
- Packet Timestamping - provides timestamping of packets on ingress and egress
- Event Capture - captures timestamps of events from DIO pins or selected network events
- Event Generation - generates signals synchronized to the reference clock
- Phase Adjust - enable adjustments of the wallclock smoothly and with minimal SPI cycles

The event capture, event generation and phase adjust features have a common interface that can be used for monitoring status and, where desired, triggering an interrupt to the station controller.

The reference clock for synchronization can be either the local 25 MHz clock, as described in the Clock Manager Section, or an external clock provided on pin DIOB0. The reference clock can be selected using the Reference Clock Select Bit (REFCLKSEL) of the Pad Control Register (PADCTRL).

#### Related Links

[4.2. Clock Manager](#)

[11.6.3. PADCTRL](#)

#### 4.5.1 Wall Clock

The wall clock is used for timestamps for inbound and outbound packets in the MAC and in the event capture unit, as well as for the time references used in the event generator. It is implemented as part of the MAC, so it can be configured and adjusted via accesses in MMS1.

The wall clock is implemented as a timer which increments each tick of the reference clock. The timer contains 94 bits where:

- The 48 upper bits [93:46] represent seconds
- The 30 lower bits [45:16] represent nanoseconds. This field resets to 0 at the end of each second.
- The lowest 16 bits [15:0] of the timer count sub-nanoseconds. This field resets to 0 at the end of each nanosecond.

Event capture and event generation use all 48 seconds bits and all 30 nanoseconds bits. Packet time stamps accessed using the built-in features of the SPI protocol will use the least significant seconds bits, as shown in the Ethernet Frame Timestamping Section.

To set the wallclock,

- Set the upper 16 bits of the wall clock seconds in the TSU Timer Seconds High (MAC\_TSH) register
- Set the lower 32 bits of the wall clock seconds in the TSU Timer Seconds Low (MAC\_TSL) register.
- Set the wall clock nanoseconds in the TSU Timer Nanoseconds (MAC\_TN) register.
- The wall clock sub-nanosecond portion is not set or read directly.

In addition to setting the clock time, it is also necessary to set the amount of time the clock increments on each tick of the reference clock. The nanosecond portion of the increment is set in the TSU Timer Increment (MAC\_TI) register, while the sub-nanosecond portion is set using the TSU Timer Increment Sub-Nanoseconds (MAC\_TISUBN) register. The LAN8650/1 uses a 25.0 MHz timer clock source and requires that the timer increment by 40.0 ns for each clock period. This is programmed by writing the value 0x00000028 to the TSU Timer Increment (MAC\_TI) register. The sub-nanosecond register is not needed on initial configuration, but can be used when synchronizing the wall clock to an external clock source.

#### Related Links

[5.2.5. Ethernet Frame Timestamping](#)

[11.2.20. MAC\\_TSH](#)

[11.2.21. MAC\\_TSL](#)

[11.2.22. MAC\\_TN](#)

[11.2.24. MAC\\_TI](#)

[11.2.19. MAC\\_TISUBN](#)

## 4.5.2 Packet Timestamps

IEEE Std 1588 describes the Precision Time Protocol (PTP), which enables synchronization of clocks over a network. In order to use PTP to synchronize the wall clock of the LAN8650/1 to an external clock source, or to use the wall clock as a clock source for other devices, it is necessary to have accurate timestamps for the receipt and transmission of packets.

### 4.5.2.1 Introduction to IEEE 802.1AS / IEEE 1588

Many end applications that are run on a network require a common sense of time; these are often called time-aware. Input sensor data needs timestamping for processing and analysis; motor and brake controls must be synchronized to control machines; chimes and lights are coordinated for a better user experience. IEEE Std 1588 describes the PTP protocol, which is used to synchronize clocks across a network. PTPv2 is a feature rich standard that allows for many variations, not all of which are compatible. IEEE Std 802.1AS specifies a subset of PTP, a *PTP profile*, called generalized Precision Time Protocol (gPTP) which is increasingly used in embedded systems. gPTP uses only layer 2 (Ethernet) synchronization, which relies on the precise timestamping of specific packets used to distribute clock and delay information across a network.

In a time-aware network, any given network segment, including a 10BASE-T1S multidrop segment, has one clock source. This source can be any element on the segment or it can be a time-aware bridge, which is synchronized to the main system clock elsewhere on the network. The clock source periodically broadcasts the current system time using the PTP SYNC message and captures the exact time that the message is transmitted. The timestamp for the SYNC message is then provided to the clock followers, either directly in the SYNC packet, or in a separate FOLLOWUP packet. Other time



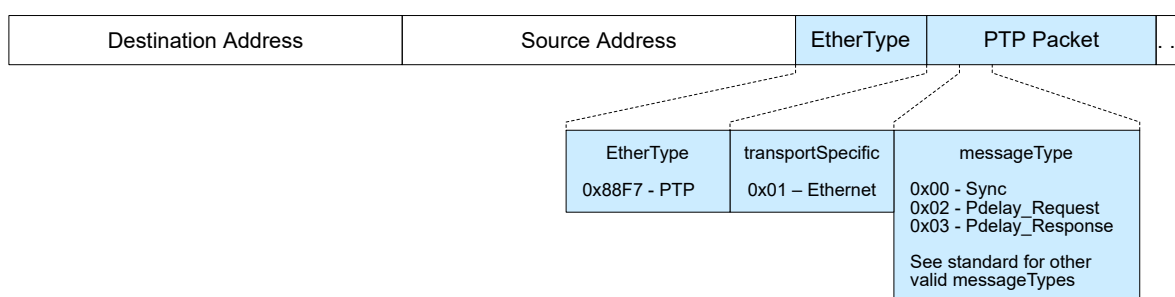
aware devices on the network segment capture the time that the SYNC message arrives and use that, along with the information from the FOLLOWUP message when needed, to adjust their local clocks to match that of the clock source. In a time aware system with known, fixed network delays, it is possible to achieve very accurate clock synchronization with just these messages.

To account for network delays when they are not known, PTP includes peer delay message types, which are used in a similar manner to calculate the delay between the local clock source and each element on the segment. One of these messages, PDELAY\_REQUEST requires precision timestamping on egress from the network element and ingress to the local clock master, similar to that required on the SYNC message. The algorithm which calculates the delay between peers assumes that the delays are constant and symmetric; it can compensate for any fixed delay, including timestamping a packet at a fixed point later than the standard end of Start-of-Frame Delimiter (SFD).

#### 4.5.2.1.1 PTP Message Format

PTP messages are transmitted in a standard Ethernet frame, which starts after the SFD with 6 bytes of Destination Address, and 6 bytes of source address. The next 2 bytes are the EtherType field, which indicates which protocol the payload represents. An EtherType field of 0x88F7 indicates that the packet is PTP over Ethernet. The next byte is fixed at 0x01 for PTP over Ethernet. The byte that follows is the PTP message type; the message types of interest are shown in [Figure 4-5](#)

**Figure 4-5.** Start of a PTP over Ethernet Frame



#### 4.5.2.1.2 PTP and 10BASE-T1S

Effective time synchronization can be run over 10BASE-T1S networks. There are two issues that need to be considered during implementation.

- When using delay calculations, timestamps need to be taken where the delay is constant. The timestamp for packet transmission normally occurs at the end of the SFD on the internal MII interface. When the MAC delivers the packet to a 10BASE-T1S PHY, however, there is a variable delay through the PHY when PLCA is enabled. PLCA requires the PHY to delay transmission of a packet until the next PLCA transmit opportunity. To have a constant delay, the transmit timestamp needs to be taken after the PLCA. Considering the receive timestamp, the MAC will only be able to create a timestamp to the resolution of the clock for the inbound data signal from the PHY, which is 400 ns on the internal MII. The solution to both of these problems is to use the signal on the MDI to determine when to timestamp. The remainder of this section will discuss features of the LAN8650/1 which enable this type of timestamping.
- While 802.1AS clearly defines the Sync and PDelay methods for full-duplex Ethernet links, there is not yet a clear definition for a shared medium, like 10BASE-T1S when used with PLCA in multidrop mode. All of the message types above are currently defined as multicast. Software workarounds to existing PTP processing are required until the standards are adapted for multidrop segments. These workarounds are beyond the scope of this document.

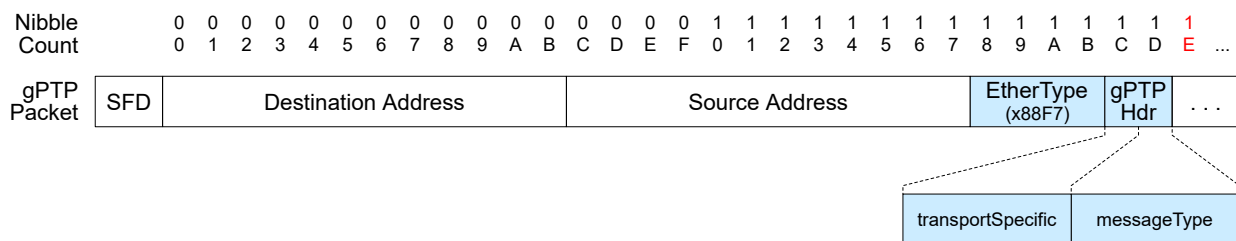


#### 4.5.2.2 PHY Timestamping

To ensure that the variable delay is not captured in the timestamp of the LAN8650/1, the MAC does not capture a timestamp based on the time that the Start-of-Frame Delimiter (SFD) crosses the MII interface to the PHY. Instead, it receives a signal from the PHY indicating that the end of the SFD has been transmitted or received on the MDI and uses that to capture the timestamp for all packets when enabled using the SPI protocol. In a busy network, or when using an inexpensive microcontroller, it may not be desirable to timestamp every packet. The LAN8650/1 adds the ability to selectively timestamp on packets that match a desired pattern, such as PTP Sync or other PTP messages.

The pattern matcher will indicate a match for a bit pattern of up to 24 bits at a configured number of nibbles after the SFD. As an example for configuring the pattern matcher, consider the SYNC message format within a MAC frame. As shown above in PTP Message Format, the EtherType field will contain 0x88F7, followed by the transport specific nibble containing 0x1 and a messageType nibble of 0x0. The 24 bit pattern to be matched is then 0x88F710. These will be located immediately after the Destination Address, and Source Address Fields of the Ethernet packet, which means that they are found in nibbles 24 through 29 of the packet. The pattern matcher location is configured as the first nibble after the location of the desired match, so for any gPTP messageType, the location will be 30.

**Figure 4-6. PTP Packet Pattern Matching**



To configure a match on SYNC message in a transmitted packet:

- Write the location value of 30 into the Transmit Match Location (TXMLOC) register.
- Write the top 8 bits of the desired pattern, 0x88, into the Transmit Match Pattern High (TXMPATH) register.
- Write the bottom 24 bits of the desired pattern, 0xF710, into the Transmit Match Pattern Low (TXMPATL) register,
- Write all 0's into the Transmit Match Mask High and Low (TXMMSKH/TXMMSKL) register mask fields so that all 24 bits of the pattern are matched.
  - Setting bits to a '1' will cause the corresponding pattern bit to be ignored during a match. This can be used to allow for multiple messageTypes, for example.
- Enable the pattern matcher by setting the Transmit Packet Match Enable (TXME) bit in the Transmit Match Control (TXMCTL) register.
- Request time stamps via the SPI protocol.

Matching receive packets operates in a similar manner, except the receive case uses the Receive Match Location (RXMLOC) register, Receive Match Pattern High (RXMPATH) register, Receive Match Pattern Low (RXMPATL) register, Receive Match Mask High (RXMSKH) Register, Receive Match Mask Low (RXMSKL) register, and Receive Packet Match Enable (RXME) bit in the Receive Match Control (RXMCTL) register.

When the pattern match location is set to zero and the 24-bit pattern match mask is to all 1's (0xFFFFFFFF), then every packet will be matched at the SFD and will be timestamped when requested by the SPI protocol. This configuration is not the default configuration of the hardware, but is the default configuration set by all Microchip drivers and in the LAN8650/1 Configuration Application

Note, [www.microchip.com/DS60001760](http://www.microchip.com/DS60001760). When using the packet filter, these register values may be configured as needed.

### Related Links

[11.5.25. TXMLOC](#)  
[11.5.21. TXMPATH](#)  
[11.5.22. TXMPATL](#)  
[11.5.23. TXMMSKH](#)  
[11.5.24. TXMMSKL](#)  
[11.5.20. TXMCTL](#)  
[11.5.32. RXMLOC](#)  
[11.5.28. RXMPATH](#)  
[11.5.29. RXMPATL](#)  
[11.5.30. RXMMSKH](#)  
[11.5.31. RXMMSKL](#)  
[11.5.27. RXMCTL](#)

### 4.5.3 Event Capture

The event capture unit can simultaneously monitor up to 4 sources and capture the wallclock time at which the configured event occurs. Each event has its own configuration register. To enable efficient use of SPI bandwidth, all resulting status and timestamps are available in a group of sequentially accessed registers. This allows for use of the autoincrement feature to burst read all of the required registers.

The Event Capture 0 Control Register (EC0CTRL) determines the input source for the event, the desired signal edge and the maximum number of timestamps that can be stored before overflow; these parameters can only be changed while the time stamper is disabled. This register is used to start and stop the time stamper, as can also be used to reset a time stamper without completely stopping it. The other capture units have their own control registers (EC1CTRL, EC2CTRL and EC3CTRL).

The common registers indicate the status of all of the event capture units. A read of the Event Capture Read Status Register (ECRDSTS) will report the number of valid timestamps stored and any overflow conditions; but it will also update all of the event capture registers that follow. These following registers will hold their values until the next time ECRDSTS is read. This enables a consistent view of the timestamps across many SPI clock cycles. All time stampers will continue to capture new time stamps as long as there is storage available even though these interface registers are not updated.

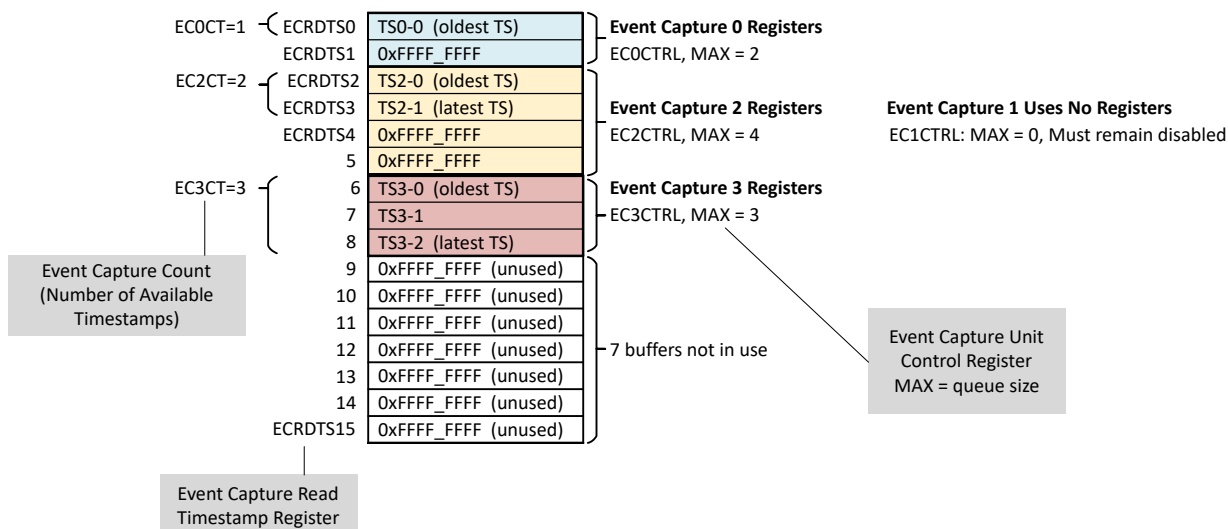
After the ECRDSTS, the next register is Event Capture Total Counts Register (ECTOT). This contains an 8-bit running count of the number of captured timestamps. These values roll over from 255 to 0.

The next three registers, Event Capture Clock Seconds High (ECCLKSH), Event Capture Clock Seconds Low (ECCLKSL), and Event Capture Clock Nanoseconds (ECLKNS), together contain the clock time stored in the MAC Timestamp Unit. In a IEEE 802.1AS, or similar, synchronized system, this clock will be synchronized to the network clock. The value is captured at the time ECRDSTS is read, and is stored with 48 bits for seconds and 30 bits for nanoseconds. This value can be combined with the captured time stamps below to determine the exact network time for any particular time stamp.

There are 16 total timestamp storage registers available; an active event capture unit shall use at least one, and the total configured by use for all four units shall not exceed 16. For event capture unit  $n$ , these are configured using the MAX field of the Event Capture  $n$  Control (EC $n$ CTRL) register. The registers occupied by event capture unit 0, if used, will start with ECRDTS0, then those used by unit 1 and so on. Figure 4-7 illustrates an example where event capture unit 0 is configured to use two registers, while unit 1 will use 10 registers and unit 3 will use three registers. Unit 2 has

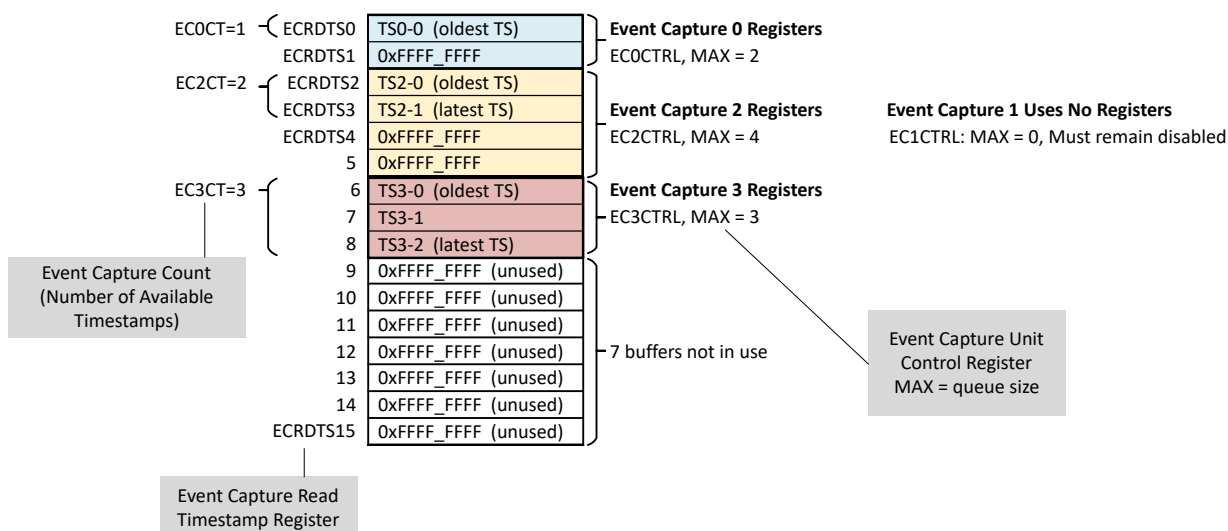
no registers and therefore shall never be enabled. To avoid loss of data in this shared resource, the MAX field of any EC $n$ CTRL register should only be changed if all time stampers are disabled.

**Figure 4-7. Allocation of Event Capture Read Timestamp Registers**



When reading out this memory space, the MAX field of EC $n$ CTRL contains the number of registers used for event capture unit  $n$ , while the EC $n$ CT field of ECRDSTS contains the actual number of valid time stamps currently stored for that unit. If a given event capture unit has more than one read register in use, the oldest timestamp will be at the lowest address. Any registers that do not contain valid timestamps will contain the value 0xFFFF\_FFFF. An example is shown in Figure 4-8, where unit 0 has a maximum of two timestamps, unit 2 has a maximum of four timestamps and unit 3 can have up to three timestamps. When ECRDSTS was read, it indicated a count of 1 timestamp for unit 0, so ECRDTS0 contains a timestamp and ECRDTS1 contains 0xFFFF\_FFFF. There are 2 timestamps from unit 2, so the oldest is in ECRDTS2 and the newer one is in ECRDTS3, with 2 invalid registers following. There are 3 timestamps from unit 3, which use register ECRDTS6-8, with the oldest in ECRDTS6. If one more timestamp is captured before EDRDTS6 is read, there will be an overflow condition and the new timestamp will not be saved.

**Figure 4-8. Reading Timestamps from Timestamp Registers**



When capture unit 0 captures a timestamp and has data available, the Event Capture 0 Data Available (EC0DA) bit in the Synchronization Event Status Register (SEVSTS), will be set. Should unit 0 be unable to save a timestamp due to an overflow, it will set the Event Capture 0 Overflow (EC0OF) bit in SEVSTS. There are Event Capture Data Available and Overflow bits for each of the other capture units also located in the SEVSTS register.

#### Related Links

[11.6.12. EC0CTRL](#)  
[11.6.13. EC1CTRL](#)  
[11.6.14. EC2CTRL](#)  
[11.6.15. EC3CTRL](#)  
[11.6.16. ECRDSTS](#)  
[11.6.17. ECTOT](#)  
[11.6.18. ECCLKSH](#)  
[11.6.19. ECCLKSL](#)  
[11.6.20. ECCLKNS](#)  
[11.6.21. ECRDTSn](#)  
[11.6.52. SEVSTS](#)

### 4.5.4 Synchronized Event Generator

The event generator can produce up to 4 different pulse outputs at once all synchronized to the internal wall clock. In addition, it can generate a separate, synchronized 1 Pulse-per-second (1PPS) signal.

#### 4.5.4.1 Configurable Event Generation

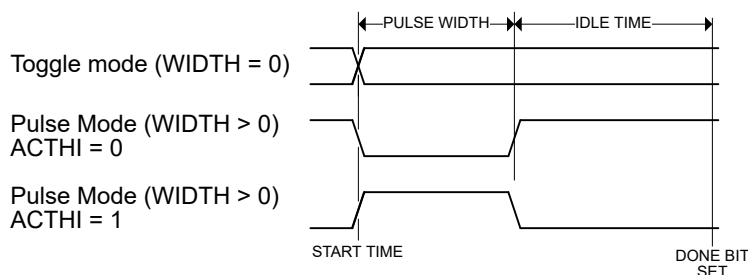
There are 4 configurable event generators, each of which can generate a single pulse or a pulse sequence derived from the same wall clock used for timestamp generation. The generated signals can be routed to the DIO pins to synchronize external devices. In addition, event generator 0 can be used to provide an internal source for ACMA. The routing of the output pulses is configured in the PADCTRL register.

All of the event generators have the same control interface. The following example uses Event Generator 0 (EG0). The names of the control registers for the other event generators begin with EG1, EG2 and EG3.

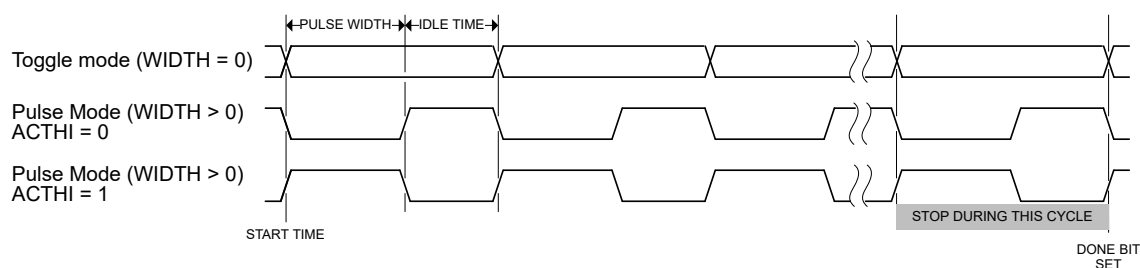
All pulses and pulse sequences begin at a programmed start time. The time is in the same format used in the MAC Time Stamping Unit: 48 bits represent seconds and 30 represent nanoseconds. The most significant 16 bits of the start time in seconds are set in the Event 0 Start Time Seconds High register while the remaining 32 bits of the start time in seconds are in the Event 0 Start Time Seconds Low register and the nanosecond portion is set in the Event 0 Start Time Nanoseconds register. If the event generator is configured for absolute time, the pulse will start when the time stamp clock matches the start time. In relative mode, actual start time is the value of the time stamp clock at the time the start bit is set in the control register plus the value in the start time registers. Relative mode is selected by setting the ISREL bit of the EG0CTL register.

The pulse width in nanoseconds is set in the EG0PW register, and the idle time is set in the EG0IT register. The pulse can be configured as active high or active low using the AH bit in the EG0CTL register.

Single pulse mode is selected by clearing the REP bit in the EG0CTL register. The timing for single pulse mode is shown in [Figure 4-9](#). Once enabled by setting the START bit in EG0CTL, the signal will be deasserted until the start time, then deasserted at the start time plus the pulse width. If the pulse width is 0, the signal will only change value at the start time. In either case, signal generation is complete and the EG0DONE bit is set in the Synchronization Event Status (SEVSTS) register at start time plus pulse width plus idle time. Other event generators will control the EG1DONE, EG2DONE or EG3DONE bits of SEVSTS.

**Figure 4-9.** Single Pulse Timing Parameters

If the REP bit in the EG0CTL register is set, the pulse will repeat, as shown in [Figure 4-10](#). Toggle mode signals will change value after a period equal to idle time. The pulses will continue until they are stopped by writing to the STOP bit of the EG0CTL register. The event will stop at the end of the next idle time. For a repeating signal, the EG0DONE bit in the SEVSTS register is set once, when the event stops.

**Figure 4-10.** Repeating Pulse Timing

**Note:** Event configuration is stored on START. Changes will have no effect on a running signal. The event must indicate DONE, before it can be reconfigured and restarted.

#### Related Links

[11.6.3. PADCTRL](#)  
[11.6.29. EG0CTL](#)  
[11.6.26. EG0STSECH](#)  
[11.6.25. EG0STSECL](#)  
[11.6.24. EG0STNS](#)  
[11.6.27. EG0PW](#)  
[11.6.28. EG0IT](#)  
[11.6.52. SEVSTS](#)

#### 4.5.4.2 One Pulse-per-second Signal Generation

The device can provide a one pulse-per-second (PPS) clock, synchronized to the time stamp clock. This signal can be provided on pin DIOA4 when selected in the register DIOMUX. The One Pulse-per-Second Control Register (PPSCTL) is used to configure the pulse width and enable and disable generation of the signal. The pulse width cannot be changed while enabled; disable signal generation and wait for the signal to stop before changing the pulse width. When the signal has been disabled, the output will continue to be driven low until the end of the second. At this time, the output will stop and the PPSDONE bit in the SEVSTS register will be set.

**Related Links**[11.6.48. PPSCTL](#)[11.6.52. SEVSTS](#)**4.5.5 Phase Adjuster**

When keeping a clock synchronized to an external clock source, it is necessary to regularly adjust the phase of the local clock. For example, in systems using the PTP SYNC message, this is usually sent from the clock source a few times a second, to enable local clocks to maintain alignment. When this message is received, early in clock acquisition, adjustments on the order of seconds may be needed. Very quickly, the systems will become better synchronized, but even then, it is not uncommon to need to make adjustments on the order of tens of nanoseconds. The time stamping clock of the internal MAC can be adjusted by single nanoseconds or single seconds. This requires many writes from the host to obtain and keep synchronization with the external source. The phase adjuster simplifies the programming on the controller, and additionally allows the change to be distributed over many clock cycles, smoothing out clock jitter and minimizing potential for inconsistent local timestamps.

The simplest way to use the phase adjuster is to write to the Phase Adjuster Control Register (PACTRL). This register enables selection of the clock delta, identifies whether it is in units of nanoseconds or of seconds, and if nanoseconds, whether the delta should be added or subtracted. When the phase adjuster is enabled by setting the Phase Adjust Active (ACT) bit, the clock time will be adjusted by one nanosecond (or one second) every clock cycle, for delta cycles. The ACT bit will be cleared at the end of the adjustment and the PADONE bit will be set in the Synchronization Event Status Register (SEVSTS). See the Synchronization Events section for more information on using this register.

If this value is only updated a few times a second, these adjustments could cause significant clock jitter, and large negative deltas could cause unexpected values in timestamps generated elsewhere in the system. To smooth out these changes and minimize jitter, the adjustments can be applied over many clock cycles, instead of at every clock edge. In this case, the Phase Adjuster Cycles Register (PACYC), should be written with the number of clock cycles between updates. This should be done before activating the adjuster via PACTRL.

As an example, suppose the clock needs to be sped up (decremented) by 25 nanoseconds. This could be done in 3 ways:

1. Without using the phase adjuster, write to the MAC 25 times.
  - This will need to be done over SPI, and in a system with network traffic may not be done before the next SYNC packet arrives and a new clock adjustment is calculated.
2. Using the phase adjuster, without using PACYC
  - Write PACTRL: DIF = 25, SEC = 0, DEC = 1 and ACT = 1 to decrement the clock 25ns, one ns per clock cycle (typically 40 ns).
  - This will take 25 timestamp clock cycles (typically 1  $\mu$ s) to complete before the ACT bit is cleared. This entire period will exhibit additional clock jitter.
  - This requires one SPI control write.
3. Use PACYC as well as PACTRL.
  - Write PACYC with the number of clock cycles between adjustments. Suppose this is 100.
  - Write PACTRL: DIF = 25, SEC = 0, DEC = 1 and ACT = 1 to begin to decrement the clock 25ns, one ns per 100 clock cycles.
  - This will take 2500 timestamp clock cycles (typically 100  $\mu$ s) to complete before the ACT bit is cleared. 1% of the cycles will exhibit extra clock jitter.
  - This requires one SPI control write of 2 consecutive addresses.

**Related Links**[11.6.23. PACTRL](#)[11.6.22. PACYC](#)[11.6.52. SEVSTS](#)[4.5.6. Synchronization Events](#)**4.5.6 Synchronization Events**

To determine which event(s) have occurred since the last read, read the Synchronization Event Status Register (SEVSTS). This register is cleared upon read, so software should ensure that all valid sources are checked when processing the data.

The events that are reported in the SEVSTS register can selectively be used to set the SEV bit of the OA\_STATUS1 register, which can be polled or configured as an interrupt. To enable a particular interrupt source to set the SEV bit, write a 1 to its corresponding bit in the Synchronization Event Interrupt Enable Register. To disable an interrupt source, write a 1 to its corresponding bit in the Synchronization Event Interrupt Disable Register. The registers are W1S registers, so a single bit can be changed without affecting other interrupt sources. It is possible to determine whether an individual event will set the SEV bit of the SEVSTS register by reading the Synchronization Event Interrupt Mask Register.

**Related Links**[11.6.52. SEVSTS](#)[11.1.7. OA\\_STATUS1](#)[11.6.49. SEVINTEN](#)[11.6.50. SEVINTDIS](#)[11.6.51. SEVIM](#)**4.6 Safety Features**

The LAN8650/1 implements a number of features for use in ISO 26262 functional safety applications. These safety features are described on the following pages. Additional information on using these features in safety critical systems is available in a Functional Safety Manual. For more information on the LAN8650/1 Functional Safety Manual, please contact Microchip.

**4.6.1 Safety Notifications**

The LAN8650/1 may be configured to perform temperature and voltage monitoring and alert the station controller when operational parameters are at risk of being exceeded. This section describes the monitoring of power supplies and die junction temperature for safe operation within operational limits as well as network related system issues.

**4.6.1.1 Under Voltage Detection**

The LAN8650/1 is able to detect a brown-out condition on each of the 1.8V and 3.3V power supplies. Details for monitoring each of the power supplies is contained in the following sections.

**4.6.1.1.1 Under-Voltage Detection (3.3V Supply)**

The device is able to detect a voltage source brown-out condition. The under-voltage condition is triggered when the VDDA or VDDAU supplies drop below a 3.05V (-7.5% nominal) threshold causing the assertion of the 3.3V supply Under-Voltage (UV33) status bit in the Status 2 (STS2) register. If the interrupt status is not masked via the 3.3V Under-Voltage Interrupt Mask (UV33M) bit in the Interrupt Mask 2 (IMSK2) register, the PHY Interrupt status (PHYINT) bit in the OPEN Alliance Status 0 (OA\_STATUS0) register will assert. The 3.3V Under-Voltage status bit will not be cleared until the supply voltage rises above the minimum threshold.

To prevent false brown-out detection due to power supply noise, the supply voltage must remain below the minimum threshold for greater than 200  $\mu$ s before the under-voltage condition will be triggered. The debounce time may be adjusted by configuring the 3.3V supply Under-Voltage Filter Time (UV33FTM) field of the Analog Control 5 (ANALOG5) register.



**Related Links**[11.5.3. STS2](#)[11.5.6. IMASK2](#)[11.5.55. ANALOG5](#)**4.6.1.1.2 Under Voltage Detection (1.8V Supply)**

The under-voltage condition is triggered when the 1.8V core supply drops below a 1.665V (-7.5% nominal) threshold causing the assertion of the 1.8V supply Under-Voltage (UV18) status bit in the OPEN Alliance Status 1 (OA\_STATUS1) register. In case of the 1.8V supply, both the LAN8650 externally sourced and the LAN8651 internally generated LDO 1.8V supplies are monitored. If the interrupt status is not masked via the 1.8V Under-Voltage Interrupt Mask (UV18M) bit in the OPEN Alliance Mask 1 (OA\_MASK1) register, the IRQ\_N pin will assert. The 1.8V Under-Voltage status bit will not be cleared until the supply voltage rises above the minimum threshold.

To prevent false brown-out detection due to power supply noise, the supply voltage must remain below the minimum threshold for greater than 5.12  $\mu$ s before the under-voltage condition will be triggered. The debounce time may be adjusted by configuring the 1.8V supply Under-Voltage Filter Time (UV18FTM) field of the Miscellaneous (MISC) register.

**Related Links**[11.1.7. OA\\_STATUS1](#)[11.1.10. OA\\_IMASK1](#)[11.6.5. MISC](#)**4.6.1.2 Over-Temperature Detection**

A mechanism is provided within the device to detect when the die junction temperature exceeds a threshold. As shown in [Table 4-2](#), there is a rising and falling die temperature threshold. The over-temperature condition is triggered when the rising temperature threshold is exceeded causing the assertion of the Over-Temperature Error (OT) status bit in the Status 2 (STS2) register. If the interrupt status is not masked via the Over-Temperature Error Interrupt Mask (OTM) bit in the Interrupt Mask 2 (IMASK2) register, the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register will assert. The Over-Temperature Error status bit will not be cleared until the die temperature falls below the falling temperature threshold.

Regardless of the state of the Over-Temperature Error status bit, the device disables this function when in the SLEEP power state and the PHYINT status bit will not be asserted.

**Table 4-2.** Over-Temperature Thresholds

| Description                                                                                                                                                    | Symbol          | Min | Max | Units |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|-------|
| Die Junction Over-Temperature Threshold                                                                                                                        |                 |     |     |       |
| Rising Temperature                                                                                                                                             | T <sub>wh</sub> | 135 | 154 | °C    |
| Falling Temperature                                                                                                                                            | T <sub>wl</sub> | 121 | 139 | °C    |
| <b>Note:</b> This table contains characterization data from a limited number of representative devices. The values are measured values and are not guaranteed. |                 |     |     |       |

**Related Links**[11.5.3. STS2](#)[11.5.6. IMASK2](#)**4.6.1.3 Transmit Jabber**

Network communication may become blocked if a device fails in such a mode as to become stuck in the transmit state continually driving the shared bus, i.e., “jabber”. To help guard against this failure mode the LAN8650/1 is designed with a transmit jabber watchdog. Should the PCS block remain in the transmit state for longer than 2 ms the jabber watchdog will trigger. When the transmit jabber watchdog triggers, the PCS will transmit special ESDERR End-of-Stream Error ESDJAB End-of-Stream



Jabber Delimiter codes to the network followed by disabling the transmitter. Additionally, the Jabber Detection Status (JAB\_DET) bit in the Clause 22 Basic Status (BASIC\_STATUS) register will be set along with the Transmit Jabber Status (TXJAB) status bit in the Status 1 (STS1) register. If the Transmit Jabber Status interrupt status is not masked via the Transmit Jabber Interrupt Mask (TXJABM) bit in the Interrupt Mask 1 (IMSK1) register, the PHY Interrupt status (PHYINT) bit in the OPEN Alliance Status 0 (OA\_STATUS0) register will assert.

Once a transmit jabber condition has been detected, the PCS will wait 16 ms before attempting another transmission. The transmit jabber watchdog is reset between packets transmitted with PLCA burst mode enabled.

Since a device terminates a jabber transmission with a special ESDJAB End-of-Stream Jabber Delimiter code, all receiving devices can detect when a remote device has jabbered. When the LAN8650/1 detects a remote transmit jabber error occurred on a remote device, the Remote Jabber Count (RMTJABCNT) field in the 10BASE-T1S PCS Diagnostic 1 (T1SPCSDIAG1) register will be incremented. In addition, the End-of-Stream Error Delimiter (ESDERR) status bit in the Status 1 (STS1) register will set. If enabled by clearing the End-of-Stream Error Delimiter Mask (ESDERRM) bit in the Interrupt Mask 1 (IMSK1) register, the PHY Interrupt status (PHYINT) bit in the OPEN Alliance Status 0 (OA\_STATUS0) register will assert when a remote jabber condition has been detected..

#### Related Links

[11.1.18. BASIC\\_STATUS](#)

[11.5.2. STS1](#)

[11.5.5. IMSK1](#)

[11.3.3. T1SPCSDIAG1](#)

#### 4.6.1.4 Transmit Collisions

By their very nature, transmitters on pure CSMA/CD networks (without PLCA) will at times collide at a rate dependent on the utilization of the network traffic on the mixing segment collision domain. As a result, many media access controllers (MACs) include collision counters so the station controller can monitor the performance of the network segment. When PLCA is enabled the physical collisions of multiple transmitters are avoided. While PLCA prevents collisions on the physical media, as a part of normal operation the PLCA RS will at times assert a logical, or false, collision to the MAC to align the MAC's transmission with the PHY's transmit opportunity.

These PLCA logical collisions will be counted by a MAC collision counter and lead the station controller to the wrong conclusion about the state of collisions on the network segment. The LAN8650/1 therefore contains a physical collision counter. The station controller can monitor the number of physical collisions the PHY has encountered when transmitting packets onto the network by reading the Corrupted Transmit Count (CORTXCNT) in the 10BASE-T1S PCS Diagnostic 2 (T1SPCSDIAG2) register. Additionally, when the PHY detects a collision while transmitting the Transmit Collision Status (TXCOL) bit in the Status 1 (STS1) register is set. If the Transmit Collision Interrupt Mask (TXCOLM) is enabled in the Interrupt Mask 1 (IMSK1) register then the PHY Interrupt status (PHYINT) bit in the OPEN Alliance Status 0 (OA\_STATUS0) register will assert. In a properly configured and operating PLCA mixing segment, no transmit collisions should be detected and the transmit collision counter should remain zero.

#### Related Links

[11.3.4. T1SPCSDIAG2](#)

[11.5.2. STS1](#)

[11.5.5. IMSK1](#)

#### 4.6.1.5 PLCA Notifications

The LAN8650/1 has the ability to detect the following PLCA error conditions and assert interrupts, if enabled. For details, please refer to the [7.2.4. Physical Layer Collision Avoidance \(PLCA\) Diagnostics](#) section.

**Table 4-3. PLCA Notifications**

| Notification      | Register.Bit    | Description                                                          |
|-------------------|-----------------|----------------------------------------------------------------------|
| PLCA Status       | STS1.PSTC       | PLCA Status Changed                                                  |
| Receive in TO     | STS1.RXINTO     | Packet received in assigned transmit opportunity                     |
| Unexpected Beacon | STS1.UNEXPB     | A Beacon was received from another device on the bus                 |
| Beacon before TO  | STS1.BCNBFTO    | A Beacon was received before the local transmit opportunity occurred |
| Maximum TO        | PRSSTS.MAXID    | Number of transmit opportunities in the last PLCA cycle              |
| TO Counter        | TOCNTH/TOCNTL   | Number of assigned transmit opportunities that have occurred         |
| Beacon Counter    | BCNCNTH/BCNCNTL | Number of received Beacons (PLCA cycles)                             |

**Related Links**

[7.2.4. Physical Layer Collision Avoidance \(PLCA\) Diagnostics](#)

[11.5.2. STS1](#)

[11.5.16. PRSSTS](#)

[11.5.8. TOCNTH](#)

[11.5.9. TOCNTL](#)

[11.5.10. BCNCNTH](#)

[11.5.11. BCNCNTL](#)

**4.6.2 Internal Fault Detection**

The LAN8650/1 includes the ability to detect various internal faults. These faults may be the result of signal noise, electromagnetic interference, high-energy particle radiation, or a latent device defect. When these faults occur the device can perform a safe action and alert the host controller to the fault for additional action in safety critical applications.

Finite state machines related to the transfer of packet data have the ability to detect an invalid transition or a transition into an invalid state. When these faults are detected, the Finite State Machine State Error (FSMSTER) status bit in the OPEN Alliance Status 1 (OA\_STATUS1) register is set. If enabled, the setting of this bit will generate an interrupt to the host controller. When this fault occurs, the host controller must perform a hardware or software reset of the device.

Errors in the internal processing of transmit and receive Ethernet frames through the device are also detectable. When an internal error is detected on the transfer of a transmit frame from the SPI to the integrated MAC, the Transmit Non-recoverable Error (TXNER) status bit in OA\_STATUS1 is set. Similarly, errors detected on the transfer of receive frames from the MAC to the SPI will set the Receive Non-recoverable Error (RXNER) status bit. When these faults occur, the transfer of Ethernet frames through the device is halted. If enabled, the setting of these bits will generate an interrupt to the host controller which must then perform a hardware or software reset of the device.

Additional fault detection features are described in the following sections.

**Related Links**

[11.1.7. OA\\_STATUS1](#)

[11.1.10. OA\\_IMASK1](#)

**4.6.2.1 SRAM Error Correction Code (ECC)**

The LAN8650/1 contains an internal 8 kB SRAM that is used for the internal buffering of transmit/receive Ethernet frames as well as buffer queue management structures. The corruption of a single SRAM bit can result in a corrupt Ethernet packet or undefined behavior when the corrupted bit

occurs in a buffer queue manager memory. Safety critical applications cannot tolerate any memory corruption.

The SRAM controller implements a Single Error Correction, Double Error Detection (SECEDED) error correction and detection circuit. The 8 kB memory is implemented as a 2 k word x 39 bit SRAM. Each word of the SRAM consists of 32 bits of data plus 7 bits of parity. Six of these bits are used as Single Error Correction parity bits, or SEC parity. These 6 parity bits allow for the detection of bit errors in the 32-bit data word. If only a single bit is corrupted, the syndrome calculated from the SEC parity indicates which bit of the 32-bit word was corrupted. The SRAM controller will then flip the corrupted bit, providing the correct data value onto the bus. The seventh parity bit is a Double Error Detection parity bit, or DED parity. When the SEC parity indicates a corrupted data word, the DED parity indicates if only a single bit of the data word was corrupted, and therefore correctable, or if more than 2 bits were corrupted. The corruption of two or more bits can only be detected; they cannot be corrected.

**Note:** If the data word is likely to have more than two bits corrupted, false negatives may occur.

The SRAM ECC is enabled by default. To disable the SRAM ECC, the parity encoder and decoder must be disabled. This is accomplished by setting the ECC Encoder Disable (ENCDIS) and ECC Decoder Disable (DECDIS) bits to a '1' in the Error Correction Code Control (ECCCTL) register. When disabled, no memory corruption will be detected or corrected.

**Note:** Both the ECC Encoder and Decoder Disable bits (ENCDIS, DECDIS) must be written to the same value.

When a single bit error is detected in the data word, the SRAM controller calculates the syndrome and automatically corrects the corrupted bit. The LAN8650/1 continues to operate normally and the Single Bit Error Count (SBERCNT) field is incremented in the Error Correction Code Status (ECCSTS) register if the Bit Error Count Enable (BERCNTEN) bit is set. As single bit errors are detected and corrected, the SBERCNT field will increment up to the limit set by the Single Bit Error Limit (SBERLMT) field in the ECCCTL register. Once the SBERCNT reaches the limit, the ECC Error (ECC) and Internal Bus Error (BUSER) status bits will be set in the OPEN Alliance Status 1 (OA\_STATUS1) register. If enabled, the setting of these bits will also assert the an interrupt to the host alerting it to the excessive number of single-bit errors encountered.

**Note:** When the Single Bit Error Count (SBERCNT) field increments to and reaches the Single Bit Error Limit (SBERLMT), an additional single bit error will cause the SBERCNT to roll over to zero. As single bit errors accumulate, the SBERCNT will continue incrementing again up to the limit.

The detection of double bit errors will immediately set the ECC Error (ECC) status bits will be set in the OA\_STATUS1 register. The transfer of the corrupted SRAM data word on the internal bus will be prevented avoiding any harmful effects and the Internal Bus Error (BUSER) status bit in the OA\_STATUS1 register will also be set. Additionally, if the BERCNTEN bit is set the Double Bit Error Count (DBERCNT) field of the ECCSTS register will be incremented.

**Note:** When the Double Bit Error Count (DBERCNT) increments to 255, an additional double bit error will cause the DBERCNT to roll over to zero.

The type of fault for the last detected SRAM error is available by reading the Error Status (ERRSTS) field of the ECCSTS register. This field will indicate if the fault was due to a single data bit error, a single parity bit error, or an uncorrectable double bit error. Additionally, when single bit errors are corrected, the computed Error Syndrome (ERRSYN) field indicates on which SRAM bit the failure was detected. The address in which the fault was detected is not available. The Error One Shot (ERONESHT) bit determines if the ERRSTS and ERRSYN fields are updated each time an error is detected (ERONESHT='0') or only on the first error detected (ERONESHT='1'). The ECC Error Status fields may be cleared to their default value at any time by writing a '1' to the Error Clear (ERCLR) bit.

### Fault Simulation

The SRAM controller can be forced to inject single and double bit errors to simulate memory corruption. This feature may be useful for the testing of firmware safety mechanisms.

To simulate single bit errors, configure both the FLTINJBIT1 and FLYINJBIT2 fields identically to flip the same SRAM bit. Double bit errors are simulated by setting the FLTINJBIT1 and FLYINJBIT2 fields to flip different bits.

#### Related Links

[11.6.9. ECCCTRL](#)

[11.6.10. ECCSTS](#)

[11.6.11. ECCFLTCTRL](#)

[11.1.7. OA\\_STATUS1](#)

[11.1.10. OA\\_IMASK1](#)

### 4.6.2.2 Bus Parity

The LAN8650/1 internally implements a bus that interconnects its major blocks. As an added measure of safety, a single bit even parity check is added that can detect single bit address and data faults in bus transfers. When enabled, a parity bit will be computed such that there is an equal number of ones on each of the address and data buses. Bus parity error detection is disabled by default and is enabled by setting the Parity Generation and Check Enable (PARGCEN) bit in the Bus Parity Control and Status (BUSPCS) register.

When a bus parity error is detected, the bus transaction is aborted (ignored) and the Bus Error (BUSER) status bit in the OPEN Alliance Status 1 (OA\_STATUS1) register is set. If enabled, an interrupt will be asserted to the host controller which should then perform a hardware or software reset of the device. The block in which the bus parity error was detected may be read from the parity error status bits in the BUSPCS register as described in the table below.

**Table 4-4. Bus Parity Errors**

| Bit Mnemonic | Bit Name                                    | Description                                                            |
|--------------|---------------------------------------------|------------------------------------------------------------------------|
| MBMPPER      | MAC Buffer Manager Parity Error             | Set when the MAC buffer manager detects a bus parity error             |
| SPIPER       | SPI Parity Error                            | Set when the SPI block detects a bus parity error                      |
| CSRBPER      | Control/Status Register Bridge Parity Error | Set when the control/status register bridge detects a bus parity error |
| SRAMPER      | SRAM Controller Parity Error                | Set when the MAC SRAM controller detects a bus parity error            |

#### Fault Simulation

As an aid in the testing of application firmware safety mechanisms, bus data parity errors may be forced. When bus parity checking is enabled setting one of the bits in the BUSPCS register will cause the associated parity error to be triggered. See the following table for the various parity errors that can be injected.

**Table 4-5. Bus Parity Error Injection**

| Bit Mnemonic | Bit Name                                                   | Description                                                             |
|--------------|------------------------------------------------------------|-------------------------------------------------------------------------|
| CSRBDPERI    | Control/Status Register Bridge Data Parity Error Injection | Control/status register bridge injects a read data parity error         |
| SRAMDPERI    | SRAM Controller Data Parity Error Injection                | SRAM controller injects a read data parity error                        |
| MBMDPERI     | MAC Buffer Manager Data Parity Error Injection             | MAC buffer manager injects a data parity error on write access          |
| MBMAPERI     | MAC Buffer Manager Address Parity Error Injection          | MAC buffer manager injects an address parity error on read/write access |

#### Related Links

[11.6.7. BUSPCS](#)

[11.1.7. OA\\_STATUS1](#)

[11.1.10. OA\\_IMASK1](#)

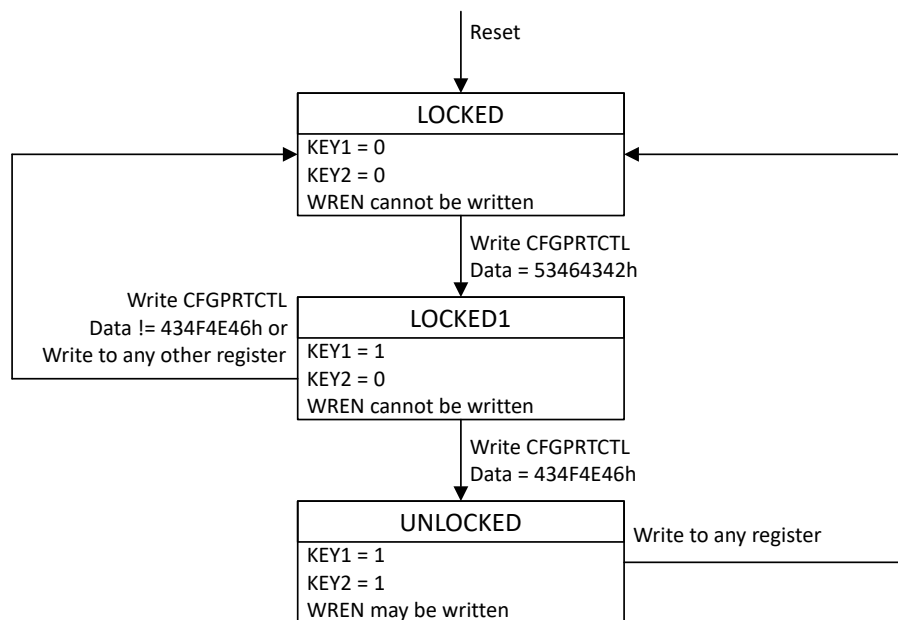
### 4.6.3 Configuration Protection

Once the device has been configured, writes to register bit fields by the host controller are typically no longer necessary. However, should the host controller encounter a fault, it is possible that incorrect firmware execution may result in errant writes to critical registers resulting in misconfiguration that could interfere with system-wide communication among other nodes on the bus. For this reason, the LAN8650/1 includes a feature to prevent writes to critical registers once configuration by the host controller is complete.

The Write Enable (WREN) bit in the Configuration Protection Control (CFGPRCTL) register enables and disables (blocks) writes to all integrated PHY registers in MMS2 (PHY PCS Registers), MMS3 (PHY PMA/PMD Registers), and MMS4 (PHY Vendor Specific Registers) as well as non-PHY registers identified in [Table 4-6](#). Following reset, the Write Enable bit is set indicating that configuration protection is inactive and writing to all register bit fields is enabled. Once the host controller has configured the device, it may write a '0' to the Write Enable bit to activate configuration protection and disable writing to all PHY configuration register bit fields preventing changes to the configuration. When register configuration protection is active, All integrated PHY and non-PHY registers not listed in the table below may be written.

By default, the Configuration Protection Control register is locked and the Write Enable bit cannot be modified. Changing the Write Enable bit requires the Configuration Protection Control register to be unlocked. Unlocking the Configuration Protection Control register requires writing two unique key values in sequence to the Configuration Protection Control register. The host controller must first write a value of 53464352h to the Configuration Protection Control register. Once written, the Key #1 Accepted (KEY1) status bit will be set. The host controller must then write a value of 434F4E46h to the Configuration Protection Control register resulting in the Key #2 Accepted (KEY2) status bit being set. If any value other than 434F4E46h is written after the first key value has been accepted, the LOCKED state is re-entered, the Key #1 Accepted status bit will be cleared and the unlocking process must be restarted. Additionally, writing to any register other than the Configuration Protection Control will also result in the register being locked again with the Key #1 Accepted status bit cleared. When both key values have been written in the correct sequence and accepted as indicated by both the KEY1 Accepted and KEY2 Accepted status bits being set, the Configuration Protection Control register is unlocked and the host controller may then write and modify the Write Enable bit, enabling or disabling writes to all register bit fields. When the Configuration Protection Control register is unlocked, a write to *any* other register will cause the Configuration Protection Control register to immediately become locked again. See [Figure 4-11](#).

**Figure 4-11.** Configuration Protection Control Register Lock/Unlock State Diagram



**Table 4-6.** Protectable non-PHY registers

| MMS   | Address | Mnemonic   | Name                             |
|-------|---------|------------|----------------------------------|
| MMS 0 |         |            | OPEN Alliance Standard Registers |
|       | 0x0003  | OA_RESET   | OPEN Alliance Configuration 0    |
|       | 0x0004  | OA_CONFIG0 | OPEN Alliance Configuration 0    |
|       | 0x0008  | OA_STATUS0 | OPEN Alliance Status 0           |
|       | 0x0009  | OA_STATUS1 | OPEN Alliance Status 1           |
|       | 0x000C  | OA_IMASK0  | OPEN Alliance Interrupt Mask 0   |
|       | 0x000D  | OA_IMASK1  | OPEN Alliance Interrupt Mask 1   |

.....continued

| MMS   | Address       | Mnemonic  | Name                            |
|-------|---------------|-----------|---------------------------------|
| MMS 1 | MAC Registers |           |                                 |
|       | 0x0000        | MAC_NCR   | Network Control Register        |
|       | 0x0001        | MAC_NCFGR | Network Configuration Register  |
|       | 0x0020        | MAC_HRB   | Hash Register Bottom            |
|       | 0x0021        | MAC_HRT   | Hash Register Top               |
|       | 0x0022        | MAC_SAB1  | Specific Address 1 Bottom       |
|       | 0x0023        | MAC_SAT1  | Specific Address 1 Top          |
|       | 0x0024        | MAC_SAB2  | Specific Address 2 Bottom       |
|       | 0x0025        | MAC_SAT2  | Specific Address 2 Top          |
|       | 0x0026        | MAC_SAB3  | Specific Address 3 Bottom       |
|       | 0x0027        | MAC_SAT3  | Specific Address 3 Top          |
|       | 0x0028        | MAC_SAB4  | Specific Address 4 Bottom       |
|       | 0x0029        | MAC_SAT4  | Specific Address 4 Top          |
|       | 0x002A        | MAC_TIDM1 | MAC Type ID Match 1             |
|       | 0x002B        | MAC_TIDM2 | MAC Type ID Match 2             |
|       | 0x002C        | MAC_TIDM3 | MAC Type ID Match 3             |
|       | 0x002D        | MAC_TIDM4 | MAC Type ID Match 4             |
|       | 0x0032        | SAMB1     | Specific Address Match 1 Bottom |
|       | 0x0033        | SAMT1     | Specific Address Match 1 Top    |
|       | 0x006F        | TIUSBN    | Timer Increment Sub-Nanoseconds |
|       | 0x0070        | TSH       | Timestamp Seconds High          |
|       | 0x0074        | TSL       | Timestamp Seconds Low           |
|       | 0x0075        | TN        | Timestamp Nanoseconds           |
|       | 0x0076        | TA        | TSU Timer Adjust                |
|       | 0x0077        | TI        | TSU Timer Increment             |
|       | 0x0200        | BMGR_CTL  | Buffer Manager Control          |

.....continued

| MMS    | Address                 | Mnemonic   | Name                                               |
|--------|-------------------------|------------|----------------------------------------------------|
| MMS 10 | Miscellaneous Registers |            |                                                    |
|        | 0x0081                  | QTXCFG     | Queue Transmit Configuration                       |
|        | 0x0082                  | QRXCFG     | Queue Receive Configuration                        |
|        | 0x0088                  | PADCTRL    | Pad Control                                        |
|        | 0x0089                  | CLKOCTL    | Clock Output Control                               |
|        | 0x0096                  | BUSPCS     | Bus Parity Control/Status                          |
|        | 0x008C                  | MISC       | Miscellaneous                                      |
|        | 0x0100                  | ECCCTRL    | SRAM Error Correction Code Control                 |
|        | 0x0101                  | ECCSTS     | SRAM Error Correction Code Status                  |
|        | 0x0102                  | ECCFLTCTRL | SRAM Error Correction Code Fault Injection Control |
|        | 0x0200                  | EC0CTRL    | Event Capture 0 Control                            |
|        | 0x0201                  | EC1CTRL    | Event Capture 1 Control                            |
|        | 0x0202                  | EC2CTRL    | Event Capture 2 Control                            |
|        | 0x0203                  | EC3CTRL    | Event Capture 3 Control                            |
|        | 0x0220                  | PACTL      | Phase Adjuster Control                             |
|        | 0x0221                  | EG0STNS    | Event 0 Start Time Nanoseconds                     |
|        | 0x0222                  | EG0STSECL  | Event 0 Start Time Seconds Low                     |
|        | 0x0223                  | EG0STSECH  | Event 0 Start Time Seconds High                    |
|        | 0x0224                  | EG0PW      | Event 0 Pulse Width                                |
|        | 0x0225                  | EG0IT      | Event 0 Idle Time                                  |
|        | 0x0226                  | EG0CTL     | Event 0 Control                                    |
|        | 0x0227                  | EG1STNS    | Event 1 Start Time Nanoseconds                     |
|        | 0x0228                  | EG1STSECL  | Event 1 Start Time Seconds Low                     |
|        | 0x0229                  | EG1STSECH  | Event 1 Start Time Seconds High                    |
|        | 0x022A                  | EG1PW      | Event 1 Pulse Width                                |
|        | 0x022B                  | EG1IT      | Event 1 Idle Time                                  |
|        | 0x022C                  | EG1CTL     | Event 1 Control                                    |
|        | 0x022D                  | EG2STNS    | Event 2 Start Time Nanoseconds                     |
|        | 0x022E                  | EG2STSECL  | Event 2 Start Time Seconds Low                     |
|        | 0x022F                  | EG2STSECH  | Event 2 Start Time Seconds High                    |
|        | 0x0230                  | EG2PW      | Event 2 Pulse Width                                |
|        | 0x0231                  | EG2IT      | Event 2 Idle Time                                  |
|        | 0x0232                  | EG2CTL     | Event 2 Control                                    |
|        | 0x0233                  | EG3STNS    | Event 3 Start Time Nanoseconds                     |
|        | 0x0234                  | EG3STSECL  | Event 3 Start Time Seconds Low                     |
|        | 0x0235                  | EG3STSECH  | Event 3 Start Time Seconds High                    |
|        | 0x0236                  | EG3PW      | Event 3 Pulse Width                                |
|        | 0x0237                  | EG3IT      | Event 3 Idle Time                                  |
|        | 0x0238                  | EG3CTL     | Event 3 Control                                    |
|        | 0x0239                  | PPSCTL     | One Pulse-per- Second Control                      |
|        | 0x023A                  | SEVINTEN   | Synchronization Event Interrupt Enable             |
|        | 0x023B                  | SEVINTDIS  | Synchronization Event Interrupt Disable            |
|        | 0x023D                  | SEVSTS     | Synchronization Event Status                       |



**Related Links**[11.6.8. CFGPRTCTL](#)

## 5. Serial Peripheral Interface (SPI)

The LAN8650/1 is designed to conform to the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification, Version 1.1. The IEEE Clause 4 MAC integration provides the low pin count standard SPI interface to any microcontroller therefore providing Ethernet functionality without requiring MAC integration within the microcontroller.

The LAN8650/1 operates as an SPI client supporting SCLK clock rates up to a maximum of 25 MHz. This SPI interface supports the transfer of both data (Ethernet frames) and control (register access).

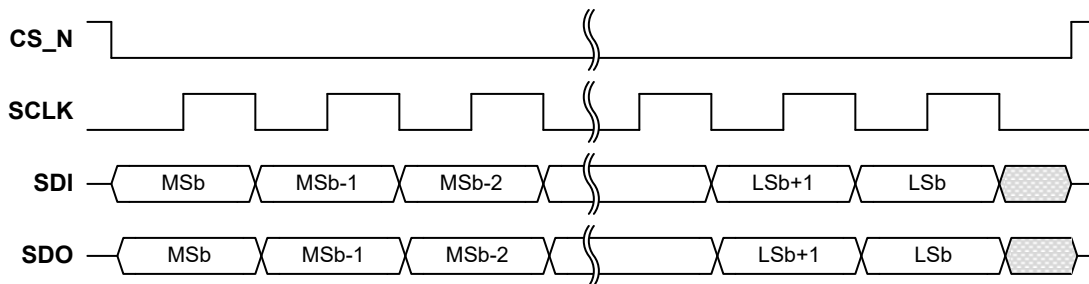
**Table 5-1.** SPI Pins

| Pin Name | Description                    | Direction |
|----------|--------------------------------|-----------|
| SDI      | Serial Data In                 | Input     |
| SDO      | Serial Data Out                | Output    |
| CS_N     | Chip Select (active low)       | Input     |
| SCLK     | Serial Clock                   | Input     |
| IRQ_N    | Interrupt Request (active low) | Output    |

### 5.1 SPI Format

The LAN8650/1 receives the SPI serial bit clock, SCLK, from the SPI host microcontroller. On the rising edge of SCLK the data is captured, while on the falling edge of SCLK the data will change. The data on SDI and SDO is always transferred most significant bit/byte first.

**Figure 5-1.** SPI Clock Polarity/Phase Mode



There are two types of SPI transactions, each with a different transaction protocol:

- Ethernet MAC Frame data transactions
- Control transactions (access to status and control registers)

The CS\_N pin must be asserted (driven low) by the SPI host to begin a transaction on SDI and SDO. The CS\_N pin is de-asserted (released) by the SPI host when the transaction completes. CS\_N must also be de-asserted between different types of transactions (Ethernet data vs Control). Multiple Ethernet data frames may be transmitted under a single CS\_N assertion, but CS\_N must be toggled and re-asserted again for every Control transaction.

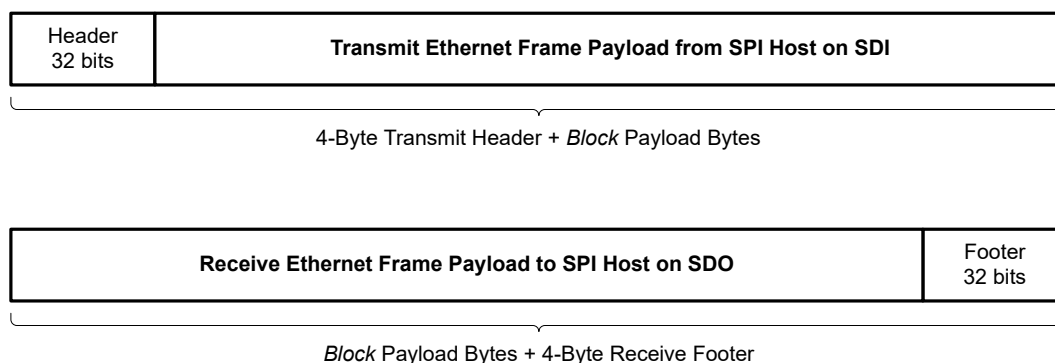
### 5.2 MAC Frame Data Transactions

All Ethernet MAC frame data transactions consist of a series of *blocks*. Ethernet MAC frames are transferred over SPI between the MAC-PHY and host by breaking the frames into segments. Each block consists of one or more segments of an Ethernet frame within a data payload plus a 32-bit header/footer. See [Figure 5-2](#). Each SPI transaction will consist of an equal number of transmit and receive data blocks. Not all data within each data block payload is required to all be valid. A transmit data block will be preceded with a 32-bit header indicating which bytes of the following data payload contains valid Ethernet transmit frame data. A receive data block is concluded with a 32-bit footer indicating which bytes of the following data payload contains valid Ethernet receive frame data.

**Note:** The OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification refers to these data transaction blocks as *chunks*.

By default, the block payload data is 64 bytes in size. A smaller block payload data size of 32 bytes is also supported and may be configured in the Block Payload Size (BPS) field of the Configuration 0 (OA\_CONFIG0) register. When changing the block payload size, the Buffer Size (BUFSZ) field of the Queue Transmit Configuration (QTXCFG) and Queue Receive Configuration (QRXCFG) registers must also be changed. Changing the block payload size must be performed prior to setting the Configuration Synchronization (SYNC) bit in the OA\_CONFIG0 register enabling Ethernet frame transfer.

**Figure 5-2.** Transmit and Receive Data Block Formats



Typically, transmit Ethernet frames are received by the MAC-PHY from the host without any padding or frame check sequence (FCS). The integrated MAC appends any padding and calculated FCS to the frame before transmitting the packet over the network.

When receiving, the MAC-PHY receives the packets from the network and the integrated MAC validates the received frames with the received FCS. When the MAC validates that a frame was received correctly, it will relay the frame to the host over SPI. If the Remove FCS (RFCS) bit of the MAC Network Configuration Register (MAC\_NCFGR) is set, the MAC will strip the FCS from the frames prior to forwarding them to the host. Should the received FCS for a frame fail to validate, the MAC will increment the Frame Check Sequence Error (FCSE) counter in the MAC Statistics 2 (STATS2) register and the frame will be dropped.

#### Related Links

[11.1.5. OA\\_CONFIG0](#)

[11.6.1. QTXCFG](#)

[11.6.2. QRXCFG](#)

## 5.2.1 MAC Frame Transmit Data Block Header

The following table depicts the breakdown of the 32-bit transmit data block header.

**Table 5-2.** Transmit Data Block Header Format

|     |       |     |      |    |     |    |    |    |
|-----|-------|-----|------|----|-----|----|----|----|
| Bit | 31    | 30  | 29   | 28 | 27  | 26 | 25 | 24 |
|     | DNC=1 | SEQ | NORX | 0  | 0   | 0  | 0  | 0  |
| Bit | 23    | 22  | 21   | 20 | 19  | 18 | 17 | 16 |
|     | VS    |     | DV   | SV | SWO |    |    |    |
| Bit | 15    | 14  | 13   | 12 | 11  | 10 | 9  | 8  |
|     | 0     | EV  | EBO  |    |     |    |    |    |
| Bit | 7     | 6   | 5    | 4  | 3   | 2  | 1  | 0  |
|     | TSC   |     | 0    | 0  | 0   | 0  | 0  | P  |

**Bit 31 - DNC** **Data, Not Control** - Flag indicating the type of transaction, data or control.

0 Control (register read/write)  
1 Data (Ethernet frame)

**Note:** The DNC bit is always set to indicate an Ethernet data transaction.

**Bit 30 - SEQ** **Data Block Sequence** - Indication of data block (chunk) sequence (even or odd). This bit is ignored by the LAN8650/1.

**Bit 29 - NORX** **No Receive** - The host MCU will set this bit to indicate to the LAN8650/1 that it will ignore any receive Ethernet frame data sent on SDO during this data block.

**Bits 23:22 - VS** **Vendor Specific** - This field is reserved for future use. The host MCU shall set these bits to zero.

**Bit 21 - DV** **Data Valid** - The host MCU sets this bit to indicate to the LAN8650/1 that valid Ethernet frame data is being transferred within the data block payload.

**Bit 20 - SV** **Start Valid** - This bit is set by the host MCU to indicate that the beginning of an Ethernet frame is contained within the data block payload. The beginning of the frame is located by the Start Word Offset (SWO) field. The SV bit is ignored if the Data Valid bit is '0'.

**Bits 19:16 - SWO** **Start Word Offset** - This field indicates which 32-bit word of the data block payload contains the first word of a new Ethernet frame. This field is ignored when Data Valid or Start Valid bits are '0'.

**Bit 14 - EV** **End Valid** - This bit is set by the host MCU to indicate that the end of an Ethernet frame is contained within the data block payload. The end of the frame is located by the End Byte Offset (EBO) field. The EV bit is ignored if the Data Valid bit is '0'.

**Bits 13:8 - EBO** **End Byte Offset** - This field indicates which byte of the data block payload contains the last byte of the end of an Ethernet frame. This field is ignored when Data Valid or End Valid bits are '0'.

**Bits 7:6 - TSC** **Time Stamp Capture** - The SPI host may use this field to indicate to the LAN8650/1 to capture the egress timestamp of an Ethernet frame into the specified timestamp capture register.

**Note:** This field is ignored when frame timestamping is disabled in the Frame Timestamp Enable (FTSE) bit of the Configuration 0 (OA\_CONFIG0) register. This field is ignored in all other conditions except when the Data Valid (DV) and Start Valid (SV) bits are both set to '1' to indicate the beginning of a new Ethernet frame transfer.

00 Do not capture frame egress timestamp  
01 Capture frame egress timestamp into Transmit Timestamp Capture Register A (TTSCA)  
10 Capture frame egress timestamp into Transmit Timestamp Capture Register B (TTSCB)  
11 Capture frame egress timestamp into Transmit Timestamp Capture Register C (TTSCC)

**Bit 0 - P** **Parity** - Parity bit over bits 31:1 of the transmit data header field. This field is set such that there is an odd total number of bits set within the header.

### Related Links

[11.1.5. OA\\_CONFIG0](#)

## 5.2.2 MAC Frame Receive Data Block Footer

The following table depicts the breakdown of the 32-bit receive data block footer.

**Table 5-3.** Receive Data Block Footer Format

|     |      |      |      |     |     |    |    |    |
|-----|------|------|------|-----|-----|----|----|----|
| Bit | 31   | 30   | 29   | 28  | 27  | 26 | 25 | 24 |
|     | EXST | HDRB | SYNC | RBA |     |    |    |    |
| Bit | 23   | 22   | 21   | 20  | 19  | 18 | 17 | 16 |
|     | VS   |      | DV   | SV  | SWO |    |    |    |
| Bit | 15   | 14   | 13   | 12  | 11  | 10 | 9  | 8  |
|     | FD   | EV   | EBO  |     |     |    |    |    |
| Bit | 7    | 6    | 5    | 4   | 3   | 2  | 1  | 0  |
|     | RTSA | RTSP | TXC  |     |     |    |    | P  |

- Bit 31 - EXST** **Extended Status** - The LAN8650/1 sets this bit any time a status bit is set pending (and unmasked) within the Status 0 (OA\_STATUS0) or Status 1 (OA\_STATUS1) registers.
- Bit 30 - HDRB** **Header Bad** - Indication that the LAN8650/1 received a transaction header with an invalid parity.
- Bit 29 - SYNC** **Configuration Synchronized** - This bit reflects the state of the Configuration Synchronization (SYNC) bit in the Configuration 0 (OA\_CONFIG0) register. A zero indicates that the LAN8650/1 configuration may be unsynchronized with the SPI host. Following configuration, the SPI host shall set the SYNC bit within the OA\_CONFIG0 register to enable the transfer of Ethernet frame data.
- Bits 28:24 - RBA** **Receive Blocks Available** - This field reflects the minimum number of blocks of buffered frame data received from the network that is available for the MCU host to read from the LAN8650/1.
- Bits 23:22 - VS** **Vendor Specific** - This field is reserved for future use. The LAN8650/1 will always set these bits to zero.
- Bit 21 - DV** **Data Valid** - The LAN8650/1 sets this bit to indicate to the SPI host that valid Ethernet frame data is being transferred within the data block payload.
- Bit 20 - SV** **Start Valid** - This bit is set by the LAN8650/1 to indicate that the beginning of an Ethernet frame is contained within the data block payload. The beginning of the frame is located by the Start Word Offset (SWO) field. The SV bit is ignored if the Data Valid bit is '0'.
- Bits 19:16 - SWO** **Start Word Offset** - This field indicates which 32-bit word of the data block payload contains the first word of a new Ethernet frame.
- Bit 15 - FD** **Frame Drop** - This bit is set when the LAN8650/1 has detected an error in the received Ethernet frame indicating to the host MCU that the current frame received from SPI should be dropped. This bit is only valid when End Valid (EV) is set indicating the end of an Ethernet frame.
- Bit 14 - EV** **End Valid** - This bit is set by the LAN8650/1 to indicate that the end of an Ethernet frame is contained within the data block payload. The end of the frame is located by the End Byte Offset (EBO) field. The EV bit is ignored if the Data Valid bit is '0'.
- Bits 13:8 - EBO** **End Byte Offset** - This field indicates which byte of the data block payload contains the last byte of the end of an Ethernet frame. This field is ignored when Data Valid or End Valid bits are '0'.
- Bit 7 - RTSA** **Receive Timestamp Added** - When set, this bit indicates that the LAN8650/1 has captured a frame ingress timestamp and added it to the beginning of the frame in the data block payload.
- Bit 6 - RTSP** **Receive Timestamp Parity** - When an ingress frame timestamp has been captured and added to the beginning of a new frame in the data block payload as indicated by the Receive Timestamp Added (RTSA) bit being set, this bit contains the odd parity bit calculated over the timestamp.
- Bits 5:1 - TXC** **Transmit Credits** - This field is used to indicate to the SPI host the number of transmit data blocks which may be sent to the LAN8650/1 without causing a buffer overflow.
- Bit 0 - P** **Parity** - Parity bit over bits 31:1 of the receive data footer field. This field is set such that there is an odd total number of bits set within the footer.

### Related Links

[11.1.5. OA\\_CONFIG0](#)

[11.1.6. OA\\_STATUS0](#)

[11.1.7. OA\\_STATUS1](#)

### 5.2.3 MAC Frame Data Integrity

While the MAC and Frame Check Sequence (FCS) safeguards Ethernet packets against bit errors over the network, it assumes an error free SPI connection between the MAC-PHY and host. However, there always exists a very small probability that the Ethernet frames between the MAC-PHY may incur bit errors over SPI. This is especially true for applications in high electromagnetic environments that could couple noise into the application. Normally these SPI bit errors cannot be detected at the Ethernet frame level and data integrity is therefore guaranteed by higher protocol layers.

For high safety or electromagnetic sensitive applications, the MAC-PHY may be configured to guarantee error-free communication over SPI at cost of increased processing by the host. The MAC-PHY is configured to protect SPI communication by setting the following bits:

- Write a '1' to the Transmit Frame Check Sequence Validation (TXFCSVE) bit of the OPEN Alliance Configuration 0 (OA\_CONFIG0) register. Setting this bit causes the MAC-PHY to validate transmit frames with the FCS computed and appended by the host.
- Write a '1' to the MAC Frame Check Sequence Disable (MACFCSDIS) bit of the Queue Transmit Configuration (QTXCFG) register. Setting this bit disables the calculation and appending of FCS for frames from the host.
- Write a '0' to the Remove FCS (RFCS) bit of the MAC Network Configuration Register (MAC\_NCFGR). note: This bit is 0 by default, preventing the MAC from stripping the FCS from frames received from the network when relaying them to the host via SPI.

For transmit frames, the host must pad the frame by appending dummy bytes to the frame payload such that the frame will be at least 60 bytes (64 bytes in length once the frame check sequence is appended). The host must then compute the 32-bit FCS for the frame and append it to the frame. The host may then transmit the frame to the MAC-PHY over SPI. When the MAC-PHY receives the frame from the host, it will validate the FCS of the frame computed and appended by the host. If the FCS fails to validate, the MAC-PHY will drop the packet and set the Transmit Frame Check Sequence Error (TXFCSSE) bit in the OPEN Alliance Status 0 (OA\_STATUS0) register.

The integrated MAC still validates frames received from the network for a valid FCS and drops the frame when an error is detected. If the frame passes the FCS validation, the MAC-PHY will relay the frame to the host via SPI without stripping the FCS. The host may then perform its own validation of the FCS to guarantee no bit errors were introduced by the SPI.

#### Related Links

[11.1.5. OA\\_CONFIG0](#)

[11.1.6. OA\\_STATUS0](#)

[11.2.2. MAC\\_NCFGR](#)

[11.2.28. STATS2](#)

[11.6.1. QTXCFG](#)

### 5.2.4 Store-and-Forward versus Cut-Through

The MAC-PHY can transfer Ethernet frames using two methods. By default, the MAC-PHY operates in a store-and-forward method. In this method the MAC-PHY receives the full Ethernet frame, from either the network or the host controller via SPI, and only thereafter forwards it to the destination, the host controller via SPI or the network. Store-and-forward is the most robust transfer method, however it incurs the most latency, especially with large frames, as the frame must be fully received by the MAC-PHY before it can be forwarded.

The second method of transfer is cut-through mode. In cut-through mode, the MAC-PHY does not need to receive the full packet before forwarding it on. Once a threshold of data has been received by the MAC-PHY, either from the network or the host controller via SPI, the MAC-PHY may begin to immediately forward the packet on to the host controller or the network much earlier than in store-and-forward mode.

Cut-through mode can significantly reduce latency in some situations. For packets received from the network, the latency can almost always be reduced when forwarding them to the host controller over SPI. However, in the transmit direction, packets received by the MAC-PHY from the host controller over SPI may need to wait for other devices to finish transmitting and will often need to wait for the local PLCA transmit opportunity to occur before the MAC-PHY can begin to forward the packet onto the network.

#### 5.2.4.1 Receive Cut-Through

By default, the MAC-PHY will receive packets and send them to the host controller in store-and-forward mode. Receive cut-through operation is enabled by setting the Receive Cut-Through Enable (RXCTE) bit in the OPEN Alliance Configuration 0 (OA\_CONFIG0) register.

When receive cut-through is enabled, the MAC-PHY will begin to send receive packet data to the host controller once it has received enough data from the network to fill a data block. The SPI host cannot read packet data from the MAC-PHY fast enough to overrun the MAC-PHY receive packet buffer. If the MAC-PHY does not have a full block of data to send to the host over SPI (and the end of the frame has not been received), the MAC-PHY will simply respond with a receive data block containing no data. Data Valid will be '0' in the block's receive data footer.

In store-and-forward operation, packets received from the network are checked for validity before being forwarded to the host controller. For example, packets with an incorrect frame check are normally not forwarded to the host controller. When operating in cut-through mode, the packet is already partially received by the host controller before the MAC can identify receive errors. As it would be a burden on the host controller to verify the receive packet integrity, when the MAC detects an invalid receive packet it will signal to the host controller that the packet should be ignored. Packets that should be ignored by the host are identified by the Frame Drop bit being set in the receive data footer in the final block of the packet when End Valid is also set.

Receive cut-through operation must be configured and enabled prior to the setting of the Configuration Synchronization (SYNC) bit in the OA\_CONFIG0 register.

#### Related Links

[11.1.5. OA\\_CONFIG0](#)

#### 5.2.4.2 Transmit Cut-Through

The MAC-PHY accepts packets from the host controller and transmits them to the network in store-and-forward mode by default. To enable transmit cut-through operation, set the Transmit Cut-Through Enable (TXCTE) bit in the OPEN Alliance Configuration 0 (OA\_CONFIG0) register.

When transmit cut-through is enabled, special care must be taken not to allow the MAC-PHY transmit buffer to underflow. Once the host controller begins to send an Ethernet frame, the MAC-PHY may begin transmitting the frame onto the network as soon as a threshold of data has arrived. At this point the host controller must continue to send the remainder of the Ethernet frame over SPI faster than the MAC-PHY is transmitting the frame to the network. If the host controller fails to keep up with the rate at which the frame is transmitted to the network a MAC-PHY transmit buffer underflow condition occurs. When this condition occurs, the MAC-PHY will terminate transmitting the frame and set the Transmit Buffer Underflow Error (TXBUE) bit in the OPEN Alliance Status 0 (OA\_STATUS0) register. The remainder of the Ethernet packet from the host controller will be ignored by the MAC-PHY and the packet will be dropped. The Ethernet frame will not be delivered to its destination and must be retransmitted by the host controller.

The risk of under-running the MAC-PHY transmit buffer and dropping frames may be reduced by increasing the threshold of Ethernet data the MAC-PHY must receive from the host controller before it begins to transmit. By default, the threshold of Ethernet packet data the MAC-PHY must receive from the SPI host before it begins transmitting is two blocks. This threshold may be increased by writing to the Cut-Through Threshold (CTTHR) field of the Queue Transmit Configuration (QTXCFG) register prior to enabling cut-through operation.

**Note:** Increasing the transmit Cut-Through Threshold will also increase transmit latency.

The cut-through latency improvement over store-and-forward is limited as the MAC-PHY may still need to wait for other devices on the network to complete transmitting on the shared media.

Transmit cut-through operation must be configured and enabled prior to the setting of the Configuration Synchronization (SYNC) bit in the OA\_CONFIG0 register.

### Related Links

[11.1.5. OA\\_CONFIG0](#)

[11.1.6. OA\\_STATUS0](#)

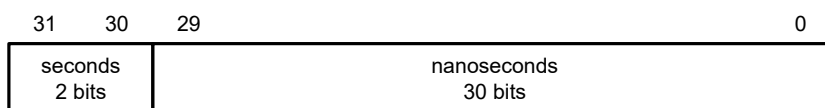
[11.6.1. QTXCFG](#)

## 5.2.5 Ethernet Frame Timestamping

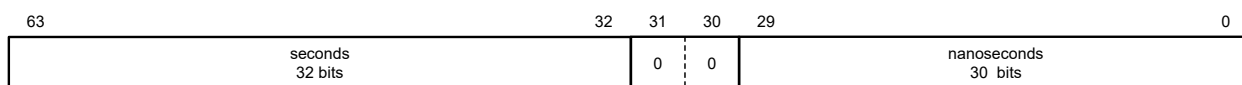
The LAN8650/1 supports timestamping on egress (transmit) or ingress (receive) of Ethernet frames via the MDI. The Frame Timestamp Capability (FTSC) bit in the Standard Capabilities (OA\_STDCAP) register indicates that the LAN8650/1 supports frame timestamping. Frame timestamping is enabled by setting the Frame Timestamp Enable (FTSE) bit within the Configuration 0 (OA\_CONFIG0) register.

Both 32-bit and 64-bit timestamp formats are supported, as shown in [Figure 5-3](#) and [Figure 5-4](#). Each timestamp format contains a 30-bit nanoseconds field which rolls over each second to zero at 0x3B9ACA00. The seconds field is incremented by one each time the nanoseconds field rolls over. The 32-bit timestamp contains a 2-bit seconds field allowing for a range of 4 seconds. The 64-bit timestamp includes a larger 32-bit seconds field.

**Figure 5-3. 32-bit Timestamp Format**



**Figure 5-4. 64-bit Timestamp Format**



The time stamp is captured by the MAC Time Stamp Unit; time stamps will be captured at the end of the Start-of-Frame delimiter for both inbound and outbound frames.

### Related Links

[4.5.1. Wall Clock](#)

[11.1.3. OA\\_STDCAP](#)

[11.1.5. OA\\_CONFIG0](#)

## 5.2.5.1 Timestamping - Frame Egress

Transmit timestamping is enabled by setting the Frame Timestamp Enable (FTSE) bit in the Configuration 0 (OA\_CONFIG0) register. The SPI host will indicate to the LAN8650/1 that a transmit (egress) timestamp should be captured for a specific frame by writing the Timestamp Capture (TSC) field of the transmit data header. The TSC field is only valid in the corresponding data header of the transmit data block payload containing the beginning of a new frame, i.e., Start Valid (SV) is set to '1'. A non-zero TSC field indicates which of three Transmit Timestamp Capture High/Low registers (TTSCAH/L, TTSCBH/L, TTSCCH/L) the captured egress timestamp value for the frame will be placed. When the frame is transmitted, the LAN8650/1 will capture the current timestamp, place the timestamp into the desired Transmit Timestamp Capture register pair, and set the appropriate Transmit Timestamp Capture Available (TTSCAA, TTSCAB, TTSCAC) status bit in the Status 0 (OA\_STATUS0) register. If enabled, the IRQ\_N pin will also be asserted.



When the TSC header field is zero (or frame timestamping is disabled), no frame egress timestamp will be captured.

**Related Links**[11.1.5. OA\\_CONFIG0](#)[11.1.6. OA\\_STATUS0](#)[11.1.11. TTSCAH](#)[11.1.12. TTSCAL](#)[11.1.13. TTSCBH](#)[11.1.14. TTSCBL](#)[11.1.15. TTSCCH](#)[11.1.16. TTSCCL](#)[5.2.1. MAC Frame Transmit Data Block Header](#)**5.2.5.2 Timestamping - Frame Ingress**

If the Frame Timestamp Enable (FTSE) bit in the Configuration 0 (OA\_CONFIG0) is set, then the LAN8650/1 will capture the current timestamp for each ingress frame received from the network. When the SPI host reads the received frame from the LAN8650/1, the LAN8650/1 will add the captured timestamp to the beginning of the frame within the data block payload. The SPI receive footer for the corresponding data block containing the added timestamp will have the footer Receive Timestamp Added (RTSA) bit set along with the Start Valid (SV) bit. The Start Word Offset (SWO) field of the footer will contain the word offset within the receive data block payload containing the first word of the added timestamp. The beginning of the received frame will immediately follow the added timestamp in the receive data block payload. The size of the timestamp will be either one or two 32-bit words as configured by the Frame Timestamp Select (FTSS) bit in the Configuration 0 (OA\_CONFIG0) register. Depending on the location of the timestamp within the receive data block payload, the beginning of the new frame may begin in the following receive data block. Likewise, the lower 32-bit word of a 64-bit timestamp may appear in the following receive data block.

When the RTSA bit is set, the Receive Timestamp Parity (RTSP) will contain the odd parity check calculated over the added timestamp.

When frame timestamping is disabled (FTSE is '0') or the footer does not indicate the beginning of a new frame (SV is '0'), then the footer RTSA and RTSP bits will always be '0'.

**Related Links**[11.1.5. OA\\_CONFIG0](#)[5.2.2. MAC Frame Receive Data Block Footer](#)

## 5.3 Control Transactions

### 5.3.1 Control Command Header

All control and status register data reads/writes are performed with Control Transactions. All Control transactions, regardless of read or write, are preceded by a 32-bit Control Command Header as shown in the following table:

**Table 5-4.** Control Command Header Format

|     |            |      |     |     |     |    |    |    |
|-----|------------|------|-----|-----|-----|----|----|----|
| Bit | 31         | 30   | 29  | 28  | 27  | 26 | 25 | 24 |
|     | DNC=0      | HDRB | WNR | AID | MMS |    |    |    |
| Bit | 23         | 22   | 21  | 20  | 19  | 18 | 17 | 16 |
|     | ADDR[15:8] |      |     |     |     |    |    |    |
| Bit | 15         | 14   | 13  | 12  | 11  | 10 | 9  | 8  |
|     | ADDR[7:0]  |      |     |     |     |    |    |    |
| Bit | 7          | 6    | 5   | 4   | 3   | 2  | 1  | 0  |
|     | LEN        |      |     |     |     |    |    | P  |

**Bit 31 - DNC** **Data, Not Control** - Flag indicating the type of transaction, data or control.

0 Control (register read/write)

1 Data (Ethernet frame)

**Note:** The DNC bit is always zero to indicate a control command and distinguish it from a frame data block header.

**Bit 30 - HDRB** **Header Bad** - Indication from the LAN8650/1 to the SPI host that the MAC-PHY received a transaction header with an invalid parity. When sent to the LAN8650/1 by the SPI host, the value of this bit is ignored by the LAN8650/1.

**Bit 29 - WNR** **Write, Not Read** - This bit indicates the type of control access to perform.

0 Control/Status register read

1 Control/Status register write

**Bit 28 - AID** **Address Increment Disable** - Normally, when this bit is 0, the address is post-incremented by one following each read/write register access within the same control command. When this bit is 1, subsequent reads or writes within the same control command will result in the same register address being accessed. This feature is useful for reading and writing register FIFOs located at a single address.

0 Register address will automatically be post-incremented following each read/write within the same control command.

1 Register address will not be post-incremented following each read/write within the same control command, allowing successive access to the same register address.

**Bits 27:24 - MMS** **Memory Map Selector** - This bit field selects the LAN8650/1 memory map to be accessed

**Bits 23:8 - ADDR** **Address** - This field specifies the address of the first register to access within the selected memory map.

**Bits 7:1 - LEN** **Length** - This field specifies the number of successive registers to read/write within the control command. The length is the number of registers to access minus one. Up to 128 consecutive registers may be read or written by a single control command. When accessing only a single register, this field is zero.

**Bit 0 - P** **Parity** - Parity bit over bits 31:1 of the control command header field. This field is set such that there is an odd total number of bits set within the header.

**Note:** The parity bit will be updated by the LAN8650/1 if it is echoed back to the SPI host with the Header Bad (HDRB) bit set.

### 5.3.2 Control Read/Write Format

Before performing a Control Read or Control Write, the SPI host will assert the CS\_N low before initiating the Control Command transaction to the LAN8650/1. The Control Read/Write Command is used to perform both individual consecutive register reads/writes. For both read and write, the Control Header sent to the LAN8650/1 over SDI is always echoed back to the SPI host over SDO. When performing control writes, the register data sent over SDI is also echoed back over SDO.

All register data is transmitted as 32-bit words, most significant byte and bit first. Any register data that is less than 32-bits will be right aligned within the word and preceded with zeros.

Register reads or writes can be unprotected (default) or protected when the Protection Enable (PROTE) bit is set in the OA\_CONFIG0 register. A protected read or write is the original word of data immediately followed with a duplicate word containing the ones' complement of the original data. The receiver of the data then performs an exclusive-OR (XOR) of the data and the ones' complement to determine if any ones are detected indicating a transmission error. If an error was detected, the LAN8650/1 will not write the incorrect data; additionally, the LAN8650/1 will not attempt to correct any write data over SDO when echoing the data.

The following figures illustrate Control Reads, Control Writes, and register data format in both protected and unprotected modes.

**Figure 5-5. Control Register Write**

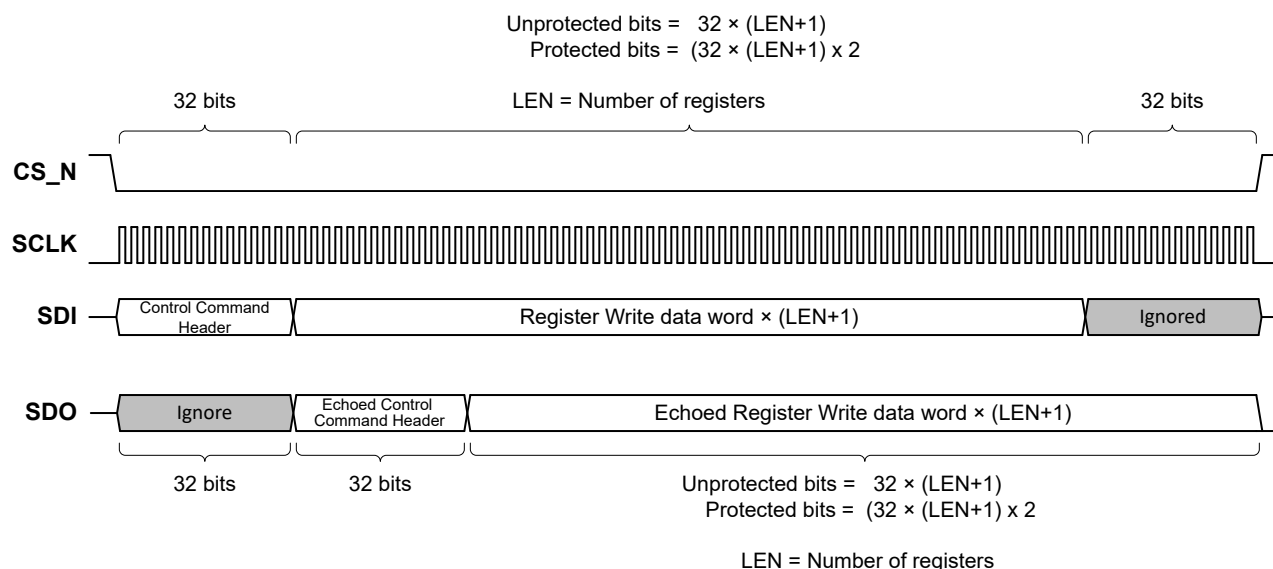


Figure 5-6. Control Register Read

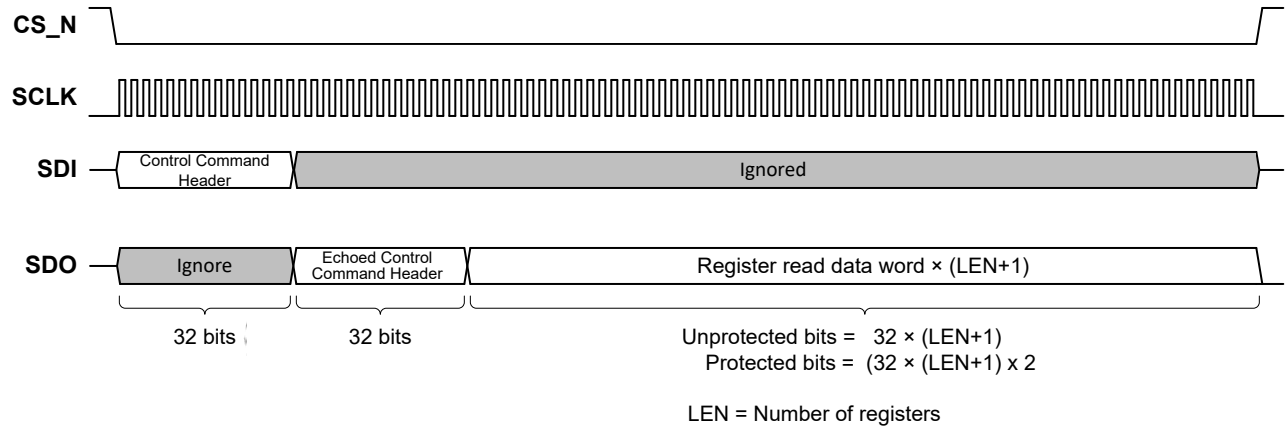
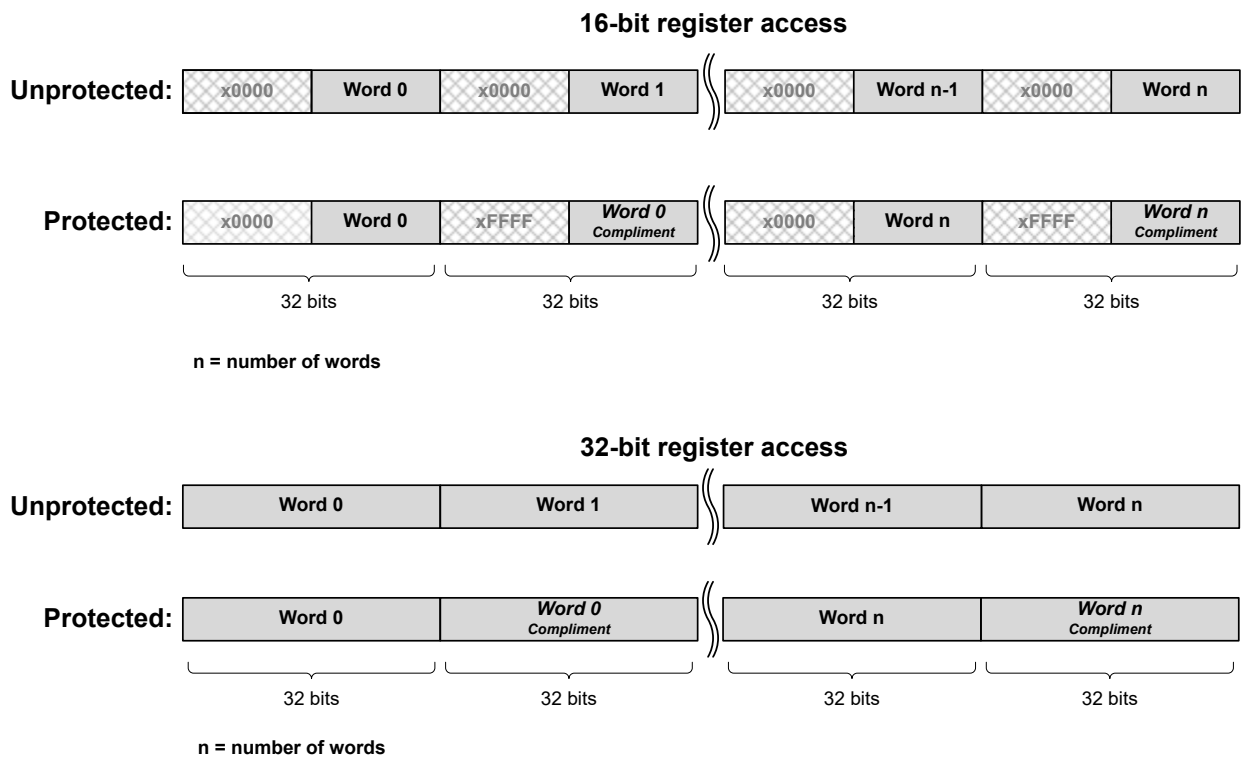


Figure 5-7. Control Register Data Formats - Protected and Unprotected



## 6. Ethernet MAC

### 6.1 Description

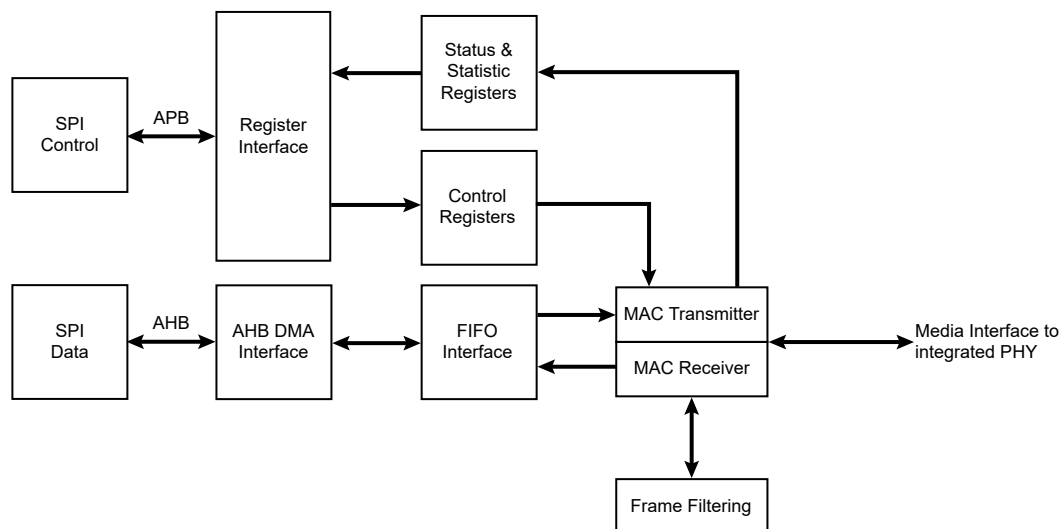
The Ethernet Media Access Controller (MAC) module implements a 10 Mbps half duplex Ethernet MAC, compatible with the IEEE 802.3 standard.

### 6.2 Embedded Characteristics

- Compatible with IEEE Standard 802.3
- 10 Mbps half duplex operation
- Statistics Counter Registers
- Internal MII interface to the integrated physical layer
- Interrupt generation to signal errors or other events
- Automatic pad and cyclic redundancy check (CRC) generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic for four specific 48-bit addresses, four type IDs, promiscuous mode, hash matching of unicast and multicast destination addresses
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Time stamp unit (TSU)

### 6.3 Block Diagram

Figure 6-1. Block Diagram



### 6.4 Functional Description

#### 6.4.1 Media Access Controller

The Transmit Block of the Media Access Controller (MAC) takes data from FIFO, adds preamble, checks and adds padding and frame check sequence (FCS). Only 10Mbps half duplex Ethernet mode of operation is supported.

Operating in half duplex mode, the MAC Transmit Block generates data according to the Carrier Sense Multiple Access with Collision Detect (CSMA/CD) protocol. The start of transmission is deferred if Carrier Sense (CRS) is active. If Collision (COL) is detected during transmission, a jam sequence is asserted and the transmission is retried after a random back off.

The Receive Block of the MAC checks for valid preamble, Frame Check Sequence (FCS), alignment/length, and presents received frames to the MAC address checking block and FIFO. It can optionally strip FCS bytes from the received frame before transferring it to FIFO.

The Address Checker recognizes four specific 48-bit addresses, can recognize four different types of ID values, and contains a 64-bit Hash register for matching multicast and unicast addresses as required. It can recognize the broadcast address *all-'1'* (0xFFFFFFFFFFFF) and copy all frames (promiscuous mode). The MAC can also reject all frames that are not VLAN tagged.

#### 6.4.2 MAC Transmit Block

The MAC transmitter operates in half duplex mode and transmits frames in accordance with the Ethernet IEEE 802.3 standard. In half duplex mode, the CSMA/CD protocol of the IEEE 802.3 specification is followed.

A small input buffer receives data through the FIFO interface which will extract data in 32-bit form. All subsequent processing prior to the final output is performed in bytes.

Transmit data is output to the integrated 10BASE-T1S PHY using the internal MII interface.

Frame assembly starts by adding the preamble and the start frame delimiter. Data is taken from the transmit FIFO interface a word at a time.

If necessary, padding is added to take the frame length to 60 bytes. A 32-bit CRC is calculated, inverted, and appended to the end of the frame taking the frame length to a minimum of 64 bytes.

In half duplex mode, the transmitter checks carrier sense. If asserted, the transmitter waits for the signal to become inactive and then begins transmission after the interframe gap of 96 bit times. If the collision signal is asserted during transmission, the transmitter will transmit a jam sequence of 32 bits taken from the data register and then retry transmission after the back off time has elapsed. If the collision occurs during either the preamble or Start Frame Delimiter (SFD), then these fields will be completed prior to generation of the jam sequence.

The back off time is based on a pseudo random binary sequence (PRBS) generator seeded from the least significant 32 bits of the MAC address as configured in the Specific Address Bottom 1 (MAC\_SAB1) register. The number of bits of the PRBS output used depends on the number of collisions seen. After the first collision 1 bit is used, then the second 2 bits and so on up to the maximum of 10 bits. All 10 bits are used above ten collisions. An error will be indicated and no further attempts will be made if 16 consecutive attempts cause collision. This operation is compliant with the description in Clause 4.2.3.2.5 of the IEEE 802.3 standard which refers to the truncated binary exponential back off algorithm. Collision back off and retry will be performed up to 16 times.

**Note:** The Specific Address Bottom 1 register should be uniquely configured for proper CSMA/CD operation. When operating in CSMA/CD mode with PLCA disabled, two nodes may collide and retry at the exact same time if the Specific Address Bottom 1 register is not configured or configured identically. This may result in frames being dropped due to excessive collisions.

#### 6.4.3 MAC Receive Block

All processing within the MAC receive block is implemented using a 16-bit data path. The MAC receive block checks for valid preamble, FCS, alignment and length, presents received frames to the FIFO interface and stores the frame destination address for use by the address checking block.

If, during the frame reception, the frame is found to be too long, a bad frame indication is sent to the FIFO interface. The receiver logic ceases to send data to memory as soon as this condition occurs.

At end of frame reception the receive block indicates to the DMA block whether the frame is good or bad. The DMA block will recover the current receive buffer if the frame was bad and the frame will not be forwarded to the SPI.

Ethernet frames are normally stored in DMA memory complete with the FCS. Setting the Remove FCS (RFCS) bit in the Network Configuration register causes frames to be stored without their corresponding FCS bytes. The reported frame length field is reduced by four bytes to reflect this operation.

The receive block signals to the statistics register block to increment the alignment, Frame Check Sequence Errors (FCSE), Undersize Frames Received (UFRX), Oversize Frames Received (OFRX), or Receive Symbol Errors (RXSE) when any of these exception conditions occur. A count of jabber errors received may be found within the integrated PHY status registers.

If the Ignore RX FCS (IRXFCS) bit is set in the Network Configuration register, CRC errors will be ignored and CRC errored frames will not be discarded, though the Frame Check Sequence Errors statistic register will still be incremented. This is useful for applications where individual frames with FCS errors must be identified.

Received frames can be checked for length field errors by setting the Length Field Error Frame Discard (LFERD) bit of the Network Configuration register. When this bit is set, the receiver compares a frame's measured length with the length field (bytes 13 and 14) extracted from the frame. The frame is discarded if the measured length is shorter. This checking procedure is for received frames between 64 bytes and 1518 bytes in length.

Each discarded frame is counted in the 8-bit Length Field Error (LFER) field of the statistics register. Frames where the length field is greater than or equal to 1536 will not be checked.

#### Related Links

[11.2.2. MAC\\_NCFGR](#)

### 6.4.4 MAC Filtering Block

The filter block determines which frames should be written to the FIFO interface and on to the SPI.

Whether a frame is passed to the SPI depends on what is enabled in the Network Configuration register, the contents of the specific address, type and Hash registers, and the frame's destination address and type field.

If the EFRHD bit of the Network Configuration register is not set, a frame will not be copied to memory if the MAC is transmitting in half duplex mode at the time a destination address is received.

Ethernet frames are transmitted a byte at a time, least significant bit first. The first six bytes (48 bits) of an Ethernet frame make up the destination address. The first bit of the destination address, which is the LSB of the first byte of the frame, is the group or individual bit. This is one for multicast addresses and zero for unicast. The *all-1*' (0xFFFFFFFF) address is the broadcast address and a special case of multicast.

The MAC supports recognition of four specific addresses. Each specific address requires two registers, Specific Address Bottom (MAC\_SABn) and Specific Address Top (MAC\_SATn). The Specific Address Bottom register stores the first four bytes of the destination address and Specific Address Top contains the last two bytes. The addresses stored can be specific, group, local, or universal.

The destination address of received frames is compared against the data stored in the Specific Address registers once they have been activated. The addresses are deactivated at reset or when their corresponding Specific Address register Bottom is written. They are activated when Specific Address register Top is written. If a receive frame address matches an active address, the frame is written to the FIFO interface and on to the SPI.

Frames may be filtered using the type ID field for matching. Four type ID registers (MAC\_TIDMn) exist in the register address space and each can be enabled for matching by writing a one to the MSB (bit 31) of the respective register. When a frame is received, the matching is implemented as an OR function of the various types of match.

The contents of each type ID register (when enabled) are compared against the length/type ID of the frame being received (e.g., bytes 13 and 14 in non-VLAN and non-SNAP encapsulated frames) and copied to memory if a match is found.

The reset state of the type ID registers is zero, hence each is initially disabled.

The following example illustrates the use of the address and type ID match registers for a MAC destination address of 21:43:65:87:A9:CB:

**Table 6-1.** Example Ethernet Frame Beginning

|                                                               |                       |
|---------------------------------------------------------------|-----------------------|
| Preamble                                                      | 55                    |
| SFD                                                           | D5                    |
| DA (Octet 0 - LSB)                                            | 21                    |
| DA (Octet 1)                                                  | 43                    |
| DA (Octet 2)                                                  | 65                    |
| DA (Octet 3)                                                  | 87                    |
| DA (Octet 4)                                                  | A9                    |
| DA (Octet 5 - MSB)                                            | CB                    |
| SA (LSB)                                                      | 00 (see <b>Note</b> ) |
| SA                                                            | 00 (see <b>Note</b> ) |
| SA                                                            | 00 (see <b>Note</b> ) |
| SA                                                            | 00 (see <b>Note</b> ) |
| SA                                                            | 00 (see <b>Note</b> ) |
| SA (MSB)                                                      | 00 (see <b>Note</b> ) |
| Type ID (MSB)                                                 | 43                    |
| Type ID (LSB)                                                 | 21                    |
| <b>Note:</b> Contains the address of the transmitting device. |                       |

The sequence in [Table 6-1](#) shows the beginning of an Ethernet frame. Byte order of transmission is from top to bottom, as shown. For a successful match to specific address 1, the following address matching registers must be set up:

Specific Address 1 Bottom register (MAC\_SAB1) = 0x87654321

Specific Address 1 Top register (MAC\_SAT1) = 0x0000CBA9

For a successful match to the type ID, the following Type ID Match 1 register must be set up:

Type ID Match 1 register (MAC\_TIDM1) = 0x80004321

#### Related Links

[11.2.2. MAC\\_NCFGR](#)

[11.2.5. MAC\\_SAB1](#)

[11.2.6. MAC\\_SAT1](#)

[11.2.13. MAC\\_TIDM1](#)

### 6.4.5 Broadcast Address

Frames with the broadcast address of 0xFFFFFFFF are received only if the No Broadcast (NBC) bit in the Network Configuration register is set to zero.

#### Related Links

[11.2.2. MAC\\_NCFGR](#)



### 6.4.6 Hash Addressing

The hash address register is 64 bits long and takes up two locations in the memory map. The least significant bits are stored in Hash Register Bottom (MAC\_HRB) and the most significant bits in Hash Register Top (MAC\_HRT).

The Unicast Hash Enable (UNIHEN) and the Multicast Hash Enable (MTIHEN) bits in the Network Configuration register enable the reception of hash matched frames. The destination address is reduced to a 6-bit index into the 64-bit Hash register using the following hash function: The hash function is an exclusive OR (XOR) of every sixth bit of the destination address.

```
hash_index[05] = da[05] ^ da[11] ^ da[17] ^ da[23] ^ da[29] ^ da[35] ^ da[41] ^ da[47]
hash_index[04] = da[04] ^ da[10] ^ da[16] ^ da[22] ^ da[28] ^ da[34] ^ da[40] ^ da[46]
hash_index[03] = da[03] ^ da[09] ^ da[15] ^ da[21] ^ da[27] ^ da[33] ^ da[39] ^ da[45]
hash_index[02] = da[02] ^ da[08] ^ da[14] ^ da[20] ^ da[26] ^ da[32] ^ da[38] ^ da[44]
hash_index[01] = da[01] ^ da[07] ^ da[13] ^ da[19] ^ da[25] ^ da[31] ^ da[37] ^ da[43]
hash_index[00] = da[00] ^ da[06] ^ da[12] ^ da[18] ^ da[24] ^ da[30] ^ da[36] ^ da[42]
```

da[0] represents the least significant bit of the first byte received, that is, the multicast/unicast indicator, and da[47] represents the most significant bit of the last byte received.

If the hash index points to a bit that is set in the Hash register then the frame will be matched according to whether the frame is multicast or unicast.

A multicast match will be signaled if the multicast hash enable bit is set, da[0] is logic 1 and the hash index points to a bit set in the Hash register.

A unicast match will be signaled if the unicast hash enable bit is set, da[0] is logic 0 and the hash index points to a bit set in the Hash register.

To receive all multicast frames, the Hash register should be set with all ones and the Multicast Hash Enable bit should be set in the Network Configuration register.

#### Related Links

[11.2.3. MAC\\_HRB](#)  
[11.2.4. MAC\\_HRT](#)  
[11.2.2. MAC\\_NCFGR](#)

### 6.4.7 Copy all Frames (Promiscuous Mode)

If the Copy All Frames (CAF) bit is set in the Network Configuration register then all frames (except those that are too long, too short, have FCS errors, or have RXER asserted by the PHY during reception) will be copied to memory. Frames with FCS errors will be copied if the Ignore RX FCS (IRXFCS) bit is set in the Network Configuration register.

#### Related Links

[11.2.2. MAC\\_NCFGR](#)

### 6.4.8 VLAN Support

The following table describes an Ethernet encoded 802.1Q VLAN tag.

**Table 6-2.** 802.1Q VLAN Tag

|                                        |                                                       |
|----------------------------------------|-------------------------------------------------------|
| TPID (Tag Protocol Identifier) 16 bits | TCI (Tag Control Information) 16 bits                 |
| 0x8100                                 | First 3 bits priority, then CFI bit, last 12 bits VID |

The VLAN tag is inserted at the 13th byte of the frame adding an extra four bytes to the frame. To support these extra four bytes, the MAC can accept frame lengths up to 1536 bytes by setting the 1536 Maximum Frame Size (MAXFS) bit in the Network Configuration register.

The MAC can be configured to reject all frames except VLAN tagged frames by setting the discard Non-VLAN Frames (DNVLAN) bit in the Network Configuration register.

**Related Links**[11.2.2. MAC\\_NCFGR](#)**6.4.9 Wall Clock**

The wall clock is used for timestamps for inbound and outbound packets in the MAC and in the event capture unit, as well as for the time references used in the event generator. It is implemented as part of the MAC, so it can be configured and adjusted via accesses in MMS1.

The wall clock is implemented as a timer which increments each tick of the reference clock. The timer contains 94 bits where:

- The 48 upper bits [93:46] represent seconds
- The 30 lower bits [45:16] represent nanoseconds. This field resets to 0 at the end of each second.
- The lowest 16 bits [15:0] of the timer count sub-nanoseconds. This field resets to 0 at the end of each nanosecond.

Event capture and event generation use all 48 seconds bits and all 30 nanoseconds bits. Packet time stamps accessed using the built-in features of the SPI protocol will use the least significant seconds bits, as shown in the Ethernet Frame Timestamping Section.

To set the wallclock,

- Set the upper 16 bits of the wall clock seconds in the TSU Timer Seconds High (MAC\_TSH) register
- Set the lower 32 bits of the wall clock seconds in the TSU Timer Seconds Low (MAC\_TSL) register.
- Set the wall clock nanoseconds in the TSU Timer Nanoseconds (MAC\_TN) register.
- The wall clock sub-nanosecond portion is not set or read directly.

In addition to setting the clock time, it is also necessary to set the amount of time the clock increments on each tick of the reference clock. The nanosecond portion of the increment is set in the TSU Timer Increment (MAC\_TI) register, while the sub-nanosecond portion is set using the TSU Timer Increment Sub-Nanoseconds (MAC\_TISUBN) register. The LAN8650/1 uses a 25.0 MHz timer clock source and requires that the timer increment by 40.0 ns for each clock period. This is programmed by writing the value 0x00000028 to the TSU Timer Increment (MAC\_TI) register. The sub-nanosecond register is not needed on initial configuration, but can be used when synchronizing the wall clock to an external clock source.

**Related Links**[5.2.5. Ethernet Frame Timestamping](#)[11.2.20. MAC\\_TSH](#)[11.2.21. MAC\\_TSL](#)[11.2.22. MAC\\_TN](#)[11.2.24. MAC\\_TI](#)[11.2.19. MAC\\_TISUBN](#)**6.4.10 PHY Interface**

The Ethernet MAC incorporates an internal MII to the integrated 10BASE-T1S PHY.

**6.5 Programming Interface****6.5.1 Initialization****6.5.1.1 Configuration**

Initialization of the MAC configuration (e.g., loop back mode) must be done while the transmit and receive circuits are disabled. See the description of the Network Control register and Network Configuration register earlier in this document.

To change loop back mode, the following sequence of operations must be followed:

1. Write to Network Control register to disable transmit and receive circuits.
2. Write to Network Control register to change loop back mode.
3. Write to Network Control register to re-enable transmit or receive circuits.

Note: These writes to the Network Control register cannot be combined in any way.

#### 6.5.1.2 Address Matching

The MAC Hash register pair and the four Specific Address register pairs must be written with the required values. Each register pair comprises of a bottom register and top register, with the bottom register being written first. The address matching is disabled for a particular register pair after the bottom register has been written and re-enabled when the top register is written. Each register pair may be written at any time, regardless of whether the receive circuits are enabled or disabled.

As an example, to set Specific Address register 1 to recognize destination address 21:43:65:87:A9:CB, the following values are written to Specific Address register 1 bottom and Specific Address register 1 top:

- Specific Address register 1 bottom bits 31:0 (MMS1, address 0x0022): 0x8765\_4321.
- Specific Address register 1 top bits 31:0 (MMS1, address 0x0023): 0x0000\_CBA9.

#### 6.5.1.3 PHY Maintenance

The internal PHY control and status registers are accessed directly using SPI command reads and writes to various Memory Map Selectors (MMS).

##### Related Links

[5.3. Control Transactions](#)

[11. Register Descriptions](#)

#### 6.5.1.4 Transmitting Frames

Frames may be written by the SPI host and transmitted if the Configuration Synchronization (SYNC) bit in the OA\_CONFIG0 register is set and the MAC transmit circuits are enabled.

1. Enable transmit in the Network Control register.
2. Set the Configuration Synchronization (SYNC) bit in the OA\_CONFIG0 register.
3. The SPI host transfers the transmit frame from the host to the MAC via the SPI.
4. The MAC transmits the frame to the internal PHY as specified by the CSMA/CD algorithm.

#### 6.5.1.5 Receiving Frames

Network frames are ignored when the Configuration Synchronization (SYNC) bit in the OA\_CONFIG0 register is '0'.

- Enable receive in the Network Control register.
- Set the Configuration Synchronization (SYNC) bit in the OA\_CONFIG0 register.

When a frame is received, the SYNC bit is set, and the MAC receive circuits are enabled, the MAC checks the address and, in the following cases, the frame is written to internal memory buffers:

- If it matches one of the four Specific Address registers.
- If it matches one of the four type ID registers.
- If it matches the hash address function.
- If it is a broadcast address (0xFFFFFFFF) and broadcasts are allowed.
- If the MAC is configured to "copy all frames" (i.e., promiscuous mode).

Once the frame has been completely and successfully received and written to internal memory, the MAC then updates the receive blocks available entry and the SPI is notified that receive data is available for reading. The host is then responsible for reading the data from the SPI.

If the MAC is unable to write the receive data into internal memory, then a receive overrun interrupt is set. If the frame is not successfully received, a statistics register is incremented and the frame is discarded without informing software.

## 6.5.2 Statistics Registers

The statistics register block is located within Memory Map Selector 1 (MMS1) beginning with the [Statistics 0 Register](#) at 0x288 and runs through to the [Statistics 11 Register](#) at 0x293. The statistic registers consist of the statistic counters listed in [Table 6-3](#) below.

**Table 6-3.** Available MAC Statistics

|                                        |                                      |
|----------------------------------------|--------------------------------------|
| Receive Symbol Errors                  | Multicast Hash Match Frames Received |
| Length Field Errors                    | Broadcast Frames Received            |
| Oversize Frames Received               | VLAN Tagged Frames Received          |
| Undersize Frames Received              | Total Frames Received                |
| Receive Resource Errors                | Frames Received Without Error        |
| Receive Buffer Overrun Errors          | Transmit Abort Internal Errors       |
| Receive FIFO Overrun Errors            | Transmit Abort External Errors       |
| Multiple Start-of-Packet Errors        | Transmit FIFO Underrun Errors        |
| Frame Check Sequence Errors            | Transmit Buffer Underrun Errors      |
| Type ID Match Frames Received          | Excessive Collisions                 |
| Specific Address Match Frames Received | Total Frames Transmitted             |
| Unicast Hash Match Frames Received     | Frames Transmitted Without Error     |

These registers reset to zero on a read and stick at all ones when they count to their maximum value. They should be read frequently enough to prevent loss of statistics data.

The receive statistics registers are only incremented when the receive enable bit (RXEN) is set in the Network Control (MAC\_NCR) register.

Once a statistics register has been read, it is automatically cleared.

### Related Links

[11.2.26. STATSO](#)

## 7. Integrated PHY

This section describes features of the 10BASE-T1S physical layer transceiver integrated into the LAN8650/1. The PHY and MAC are connected via an internal Media Independent Interface (MII).

### 7.1 Interrupt Management

The LAN8650/1 integrated PHY supports multiple interrupt capabilities which are not part of the IEEE 802.3 specification. When selected PHY status events are detected as configured by the PHY Interrupt Mask Registers, the PHY Interrupt (PHYINT) status bit in the OPEN Alliance Status 0 (OA\_STATUS0) register is set. If further enabled by PHY Interrupt Mask (PHYINTM) bit in the OPEN Alliance Interrupt Mask 0 (OA\_IMASK0) register, the IRQ\_N pin will be asserted low.

To assert the PHY Interrupt status for a given event in the Status 1 (STS1) and Status 2 (STS2) registers, the corresponding mask bit in the Interrupt Mask 1 (IMASK1) and Interrupt Mask 2 (IMASK2) registers must be written to '0' to enable the interrupt. When the associated event occurs setting the status bit, the PHY Interrupt status bit will also be asserted. When the event to negate the status bit is true, or the corresponding bit in the Interrupt Mask Register is set disabling the interrupt, the PHY Interrupt status bit will be deasserted.

All PHY interrupts are disabled (masked) following a reset.

#### Related Links

[11.1.6. OA\\_STATUS0](#)

[11.1.9. OA\\_IMASK0](#)

[11.5.2. STS1](#)

[11.5.3. STS2](#)

[11.5.5. IMASK1](#)

[11.5.6. IMASK2](#)

### 7.2 Physical Layer Collision Avoidance (PLCA)

PLCA operates in conjunction with a CSMA/CD MAC to actively avoid collisions among half-duplex stations (known as PLCA *nodes*) allowing for greater network utilization. Each node on the network segment (i.e., collision domain) is assigned a unique *Local ID*. *Transmit opportunities* are then granted to each node in sequence based on their Local ID. The node configured as Local ID = 0 is known as the *PLCA coordinator*. The role of the PLCA coordinator is to transmit a periodic synchronizing BEACON onto the physical media. All other nodes are referred to as a *PLCA follower* as they follow the synchronization of the coordinator. Once the BEACON has been received on the segment, all nodes begin counting transmit opportunities beginning with zero. Nodes detect their assigned transmit opportunity by counting the number of opportunities that have passed since the transmission of the BEACON by the PLCA coordinator. Each node may transmit when the number of transmit opportunities counted since the BEACON matches the Local ID assigned to the node. Within each transmit opportunity, the node assigned the current opportunity may either transmit a packet or yield. Once the node has transmitted a packet (or yielded), each node increments the transmit opportunity counter and the transmit opportunity goes to the next node. The first transmit opportunity of zero allows node with Local ID = 0 to transmit. Once a fixed number of transmit opportunities has been provided, the PLCA coordinator will transmit another BEACON starting the cycle over again. A BEACON followed by a fixed number of transmit opportunities is known as a *PLCA bus cycle*.

On multidrop topologies with multiple nodes connected to a shared media mixing segment, PLCA enables a fairness in opportunity to transmit such that one node cannot transmit more than one frame without each of the other nodes also being granted an opportunity to transmit. There are 2 exceptions that can be useful on multidrop segments where one or more nodes transmit more often than other nodes. PLCA allows individual nodes to be configured to transmit a burst of frames within

a single transmit opportunity. The LAN8650/1 can also assign individual nodes multiple transmit opportunities within the bus cycle.

PLCA is enabled by setting the PLCA Enable bit in the PLCA Control 0 (PLCA\_CTRL0) register. The node Local ID is configured within the PLCA Local ID (ID) field of the PLCA Control 1 (PLCA\_CTRL1) register and must be unique within the PLCA network segment to successfully avoid collisions. Additionally, the Local ID must be less than the number of transmit opportunities in each bus cycle in order to be granted a transmit opportunity (see the Node Count field of the PLCA Control 1 register). When the node is configured as the PLCA coordinator, then the number of transmit opportunities within each PLCA bus cycle (period between successive BEACON transmissions) is configured in the Node Count (NCNT) field of the PLCA Control 1 register.

The time for each transmit opportunity is configured within the PLCA Transmit Opportunity Timer (PLCA\_TOTMR) register. The transmit opportunity timer must be set equal among all nodes in the PLCA collision domain to maintain synchronization among the nodes. The default transmit opportunity timer value, 3.2  $\mu$ s, is appropriate for segments specified in IEEE 802.3 Clause 147 and should only be changed in special circumstances.



**Important:** The Transmit Opportunity timer must be configured identically across all nodes on the multidrop mixing segment.



Improper configuration of Transmit Opportunity timer may result in reduced network performance or collisions. Determination of the optimal Transmit Opportunity time requires knowledge of various delays of each of the vendor PHYs on the mixing segment and various physical layer propagation delay. It is recommended to leave this field at its default value unless a full evaluation of delays has been performed.



**Tip:** As collisions should not occur on a properly configured PLCA mixing segment, disabling collision detection is recommended when PLCA is enabled and active as it improves bus noise tolerance. See the PLCA Collision Detection section for more details.

When PLCA has been enabled on a node, the PLCA Status bit in the PLCA Status (PLCA\_STS) register will indicate if the node is actively receiving a periodic PLCA BEACON. When the PLCA Status bit changes, the PLCA Status Changed (PSC) bit in the Status 0 (STS0) register will be set and, optionally, may assert the IRQ\_N pin. This may be useful for diagnosing a misbehaving PLCA network segment.

#### Related Links

[7.2.1. PLCA Burst Mode](#)

[7.2.2. Multiple PLCA Transmit Opportunities](#)

[8.5. PLCA Collision Detection](#)

[11.5.57. PLCA\\_CTRL0](#)

[11.5.58. PLCA\\_CTRL1](#)

[11.5.60. PLCA\\_TOTMR](#)

[11.5.59. PLCA\\_STS](#)

### 7.2.1 PLCA Burst Mode

Some applications, such as sensors or audio, may require the transmission of frequent small frames with a limited latency. As PLCA specifies only one transmit opportunity for each node in each bus cycle, these applications may experience significant latency when they are connected onto a multidrop mixing segment with applications that transmit large packets. For example, an audio application may require the transmission of eight stereo 16-bit audio samples as 64 byte packets

every 167  $\mu$ s with minimal latency. When another node on the segment transmits a 1500 byte packet it will occupy the channel for 1.2 ms. The audio application will therefore buffer seven audio packets during the time that the channel is occupied. With standard PLCA, the audio application will only be able to transmit one of its audio packets during the next PLCA bus cycle. The result is that each successive audio packet the audio application needs to transmit is delayed with increasing latency.

One solution to this problem is to allow specific nodes to transmit more than one packet during its transmit opportunity. This ability to transmit a burst of multiple packets allows the audio application in the above example to empty its buffers and transmit all audio packets that it has queued, preventing the latency of the audio packets to grow beyond a tolerable limit.

The ability to transmit packets in a burst is configurable individually for each node on the segment. The Maximum Burst Count (MAXBC) field in the PLCA Burst Mode (PLCA\_BURST) register configures the maximum number of additional packets allowed to transmit in each of the node's transmit opportunities. This is in addition to the initial packet that may be transmitted by the node in its transmit opportunity. Additionally, the Burst Timer (BTMR) field configures the amount of time the node may transmit (COMMIT) to maintain a hold on its current transmit opportunity after transmitting a packet to allow the MAC to transmit an additional packet. Once this timer expires, the node will then yield the transmit opportunity to the next node.



**Restriction:** To prevent undesirable traffic shaping behavior, PLCA burst mode should not be used in conjunction with credit based traffic shaping.

#### Related Links

[11.5.61. PLCA\\_BURST](#)

## 7.2.2 Multiple PLCA Transmit Opportunities

The PLCA burst mode allows a node to transmit multiple packets within its single transmit opportunity in each PLCA bus cycle. While transmitting a burst of packets in a single transmit opportunity bounds the maximum latency to the period of a PLCA bus cycle, the latency may be further reduced by allowing a node multiple transmit opportunities in each PLCA bus cycle. This allows the same node to transmit multiple frames evenly spread in time throughout the PLCA bus cycle. This is accomplished by assigning multiple Local IDs to the node thereby allowing it multiple transmit opportunities. When the transmit opportunity counter matches any one of the multiple Local IDs assigned to the node, the node may then transmit a packet or yield the transmit opportunity.

The LAN8650/1 supports the assignment of up to eight additional transmit opportunities per PLCA bus cycle. The additional transmit opportunity Local IDs are configured in the ID1-ID8 fields of the PLCA Multiple ID 0-3 (MULTID0-MULTID3) registers.

The Clause 4 compliant MAC requires an inter-packet gap (IPG) of at least 9.6  $\mu$ s (96 bits) following the transmission of one packet before it will transmit another packet. Should consecutive transmit opportunities be assigned to the same node, transmit opportunities following a packet transmission will not be used until after the inter-packet gap has expired. For best performance when assigning multiple transmit opportunities to the same node it is therefore recommended that they should be interleaved with transmit opportunities assigned to other nodes.

#### Related Links

[11.5.12. MULTID0](#)

[11.5.13. MULTID1](#)

[11.5.14. MULTID2](#)

[11.5.15. MULTID3](#)



### 7.2.3 PLCA Transmit Opportunity Skipping

PLCA transmit opportunity skipping is useful to limit the amount of data low-priority nodes may transmit onto the network. When transmit opportunity skipping is enabled, the PHY is configured to skip a number of PLCA transmit opportunities once a packet has been transmitted. The PHY will yield the skipped transmit opportunities and prevent the internal MAC from transmitting by asserting the internal MII CRS signal. Once the specified number of transmit opportunities have been skipped, the PHY will re-enable normal PLCA operation of CRS and permit the MAC to transmit packets when its transmit opportunities occur.

PLCA transmit opportunity skipping is enabled by setting the PLCA Transmit Opportunity Skip Enable (TOSKPEN) bit in the PLCA Skip Control (PLCASKPCTL) register. The number of transmit opportunities to skip after transmitting a packet is configured in the PLCA Transmit Opportunity Skip (PLCATOSKP) register.



**Restriction:** To prevent undesirable traffic shaping behavior, PLCA transmit opportunity skipping should not be used in conjunction with credit based traffic shaping.

#### Related Links

[11.5.46. PLCASKPCTL](#)

[11.5.47. PLCATOSKP](#)

### 7.2.4 Physical Layer Collision Avoidance (PLCA) Diagnostics

The LAN8650/1 integrated PHY implements a number of features useful to the detection of PLCA misconfiguration on the network segment. These features include error status indications and event counters.

The PLCA error status indicators are located in the PHY Status 1 (STS1) register. Each indication also has an associated interrupt mask bit in the Interrupt Mask 1 (IMSK1) register to enable an assertion of the PHY interrupt (PHYINT) status bit of the OPEN Alliance Status 0 (OA\_STATUS0) register when the event is detected. When enabled, an assertion of the PHY interrupt (PHYINT) status bit will also assert the IRQ\_N pin to the station controller.

Each node of a PLCA segment must be assigned a unique Local ID to properly avoid collisions. The device has the ability to detect that another node is assigned the same Local ID by detecting the reception of a packet from the network during its assigned transmit opportunity. When this condition occurs, the Receive in Transmit Opportunity (RXINTO) status bit is set. Additionally, should a collision be detected while the device is transmitting in its assigned transmit opportunity, the Transmit Collision (TXCOL) status bit will be set.

Multiple nodes configured and acting as PLCA Coordinators also cause problems. Multiple Coordinators on the mixing segment will each transmit a BEACON according to its own PLCA bus cycle and timing. The result is that each Coordinator will receive BEACONS that it did not transmit. When configured as a PLCA Coordinator, it will set the Unexpected BEACON Received (UNEXPB) status bit to indicate the presence of another Coordinator on the network segment.

The PLCA Coordinator must be configured with the correct number of nodes on the segment to permit the proper number of transmit opportunities per bus cycle. If the Coordinator is configured to allow for too few transmit opportunities between BEACONS, Follower nodes may not have access to their assigned transmit opportunity. When the device is operating as a PLCA Follower, if it detects a BEACON before its assigned transmit opportunity occurs then the BEACON Received Before Transmit Opportunity (BCNBFTO) status bit is set to indicate that the configured PLCA bus cycle is too small to allow the Follower to transmit.

When configured as a PLCA Follower, the PLCA Status (PST) bit in the PLCA Status (PLCA\_STS) register will be set as long as BEACONS are regularly being received from a Coordinator. If BEACONS are not received by the device it will continue incrementing its transmit opportunity counter. When the



transmit opportunity counter reaches the maximum count of 255, it will then stop incrementing and a 13 ms timer is started. If no BEACON is received after the timer expires, the PLCA Status bit will be cleared. When the PLCA Status bit is zero, the device will revert to CSMA/CD operation with PLCA deactivated. Once a BEACON is received the device will set the PLCA Status bit and return to normal PLCA operation. Refer to Clause 148 of the IEEE 802.3cg specification for additional details. When the PLCA Status bit changes, the PLCA Status Changed (PSTC) bit in the Status 1 register is set and will assert the PHY interrupt (PHYINT) status bit, if enabled in the Interrupt Mask 1 register.

The number of transmit opportunities in the PLCA bus cycle may be determined by reading the Maximum ID (MAXID) field of the PLCA Reconciliation Sublayer Status (PRSSTS) register. The MAXID field is updated at the end of each bus cycle. When read it will contain the number of transmit opportunities the PLCA coordinator allowed in the previous bus cycle.

Two event counters are implemented to aid the station controller in monitoring PLCA on the segment. These counters include a transmit opportunity counter and a BEACON counter. Each counter is enabled by setting the corresponding enable bit in the Counter Control (CTRCTRL) register. Writing a '1' to the Transmit Opportunity Counter Enable (TOCTRE) bit enables the transmit opportunity counter. The BEACON Counter Enable (BCNCTRE) bit enables the BEACON counter when set.

When enabled, the Transmit Opportunity Count High/Low (TOCNTH/TOCNTL) registers will contain the number of transmit opportunities the local PHY could have used to transmit since the last read. By polling the counter, the station controller can monitor that PLCA is active and that the PHY can transmit packets when needed.

Similarly, the BEACON Count High/Low (BCNCNTH/BCNCNTL) register contains the number of received BEACONS since the last read. The station controller can poll this counter to monitor the health of the PLCA Coordinator.

#### Related Links

[11.1.6. OA\\_STATUS0](#)

[11.1.9. OA\\_IMASK0](#)

[11.5.2. STS1](#)

[11.5.5. IMASK1](#)

[11.5.59. PLCA\\_STS](#)

[11.5.16. PRSSTS](#)

[11.5.7. CTRCTRL](#)

[11.5.8. TOCNTH](#)

[11.5.9. TOCNTL](#)

[11.5.10. BCNCNTH](#)

[11.5.11. BCNCNTL](#)

## 7.3 Application Controlled Media Access (ACMA)

Physical Layer Collision Avoidance (PLCA) improves upon traditional CSMA/CD network utilization by eliminating collisions while also providing determinism for packet transmission. A customized media access method may be appropriate in systems requiring more control over latency or bandwidth allocation. The LAN8650/1 provides Application Controlled Media Access (ACMA) as an alternative to PLCA or CSMA/CD which allows implementation of custom scheduled access to the medium for applications requiring a fixed, deterministic latency. This could be used to implement a time-division multiple access (TDMA) method that allocates a specific transmit time slot for each station on the shared medium. Such a system avoids collisions, while reserving fixed bandwidth for each station and guarantees access latency to provide deterministic network behavior. A system using ACMA can even allow synchronization of the time slots across a network using the IEEE Std 802.1AS generalized Precision Time Protocol (gPTP).

The ACMA mode is enabled by setting the ACMA Enable (ACMAEN) bit in the ACMA Control (ACMACTL) register. The ACMA signal source is selected using the ACMA Input Select bit field (ACMASEL) in Pad Control Register (PADCTL) and can be either DIO2 or the output of Event Generator 0. This signal is always active high.

When enabled, the ACMA signal is used to control transmit access to the medium. If the ACMA input is not asserted, transmission from the MAC is held off. Only when the ACMA signal is asserted is the MAC allowed to transmit. If the MAC has a frame to send, it asserts TXEN and begins transmitting. The MAC can send multiple packets if the ACMA assertion time is long enough to permit it. Once transmission of a packet has started, the full packet will be transmitted regardless of the status of ACMA.

The timing of the ACMA signals depends on the bandwidth requirements and numbers of transmitters on the mixing segment. To work with the greatest variety of MACs, the minimum recommended ACMA enable pulse width is 10  $\mu$ s. This ensures that the device will have more than the inter-packet gap of 9.6  $\mu$ s to enable TXEN after release of CRS. The minimum period between consecutive time slots on the mixing segment must not be less than the time to transmit the largest Ethernet packet or sequence of packets plus 9.6  $\mu$ s.

**Note:** Other stations on the network must not assert ACMA until the previous time slot has expired. Failure to meet this constraint may result in collisions on the network or the loss of ability to transmit within the assigned time slot.

Collisions will not occur on properly engineered and synchronized ACMA. However, to aid in development and debug, when ACMA is enabled the device will set the Unexpected CRS (UNCRS) status bit in the Status 1 (STS1) register if receive carrier is sensed from the network when the ACMA pin is asserted. If needed, IRQ\_N can be asserted when this status bit is asserted; this is configured by writing a 0 into the UNCRSM bit of the IMSK1 register.

#### Related Links

[11.5.48. ACMACTL](#)

[11.6.3. PADCTRL](#)

[11.5.2. STS1](#)

[11.5.5. IMSK1](#)

## 7.4 Credit Based Traffic Shaping

The LAN8650/1 implements a hardware credit based traffic shaper (CBS) to control the station's transmit bandwidth. A hardware credit counter is used to enable and disable the ability to transmit packets onto the medium. The PHY decrements the credit counter during transmit and increments the counter when the PHY is receiving data or the medium is idle. When the credit counter is below the stop threshold, the PHY does not have enough credits to transmit. The PHY will then hold the MAC off from transmitting by asserting the internal MII CRS signal. When the PHY is not transmitting, it will accumulate credits. Once the credit counter exceeds the start threshold, CRS will operate normally. Once the PHY allows the internal MAC to begin transmitting a packet, the entire packet will be transmitted even if the credit counter decrements below the stop threshold while it is transmitting.

The credit based traffic shaper is enabled by setting the CBS Enable (CBSEN) bit in the Credit Based Shaper Control (CBSCTRL) register. The credit based traffic shaper may be used with or without PLCA.

The transmit stop threshold is configurable in the Stop Threshold (STOPTHR) bit field in the Credit Based Shaper Stop Threshold High/Low (CBSSPTHH/CBSSPTHL) registers. The Start Threshold (STARTTHR) field in the Credit Based Shaper Start Threshold High/Low (CBSSTTHH/CBSSTTHL) registers is used to configure the transmit start threshold.

The Falling Slope (FALLSLP) field of the Credit Based Shaper Slope Control (CBSSLPCTL) register configures the rate at which the credit counter loses credits when transmitting. Similarly, the Rising

Slope (RISESLP) field configures the rate at which the credit counter will accumulate credits when the medium is idle or the PHY is receiving data. When PLCA is enabled, credits may additionally be accumulated at an accelerated rate when no transmission is detected within each PLCA bus cycle. The rate at which credits are accumulated for each empty PLCA bus cycle is configured by the Empty Cycle Credits (ECCRDS) field of the Credit Based Shaper Control register.

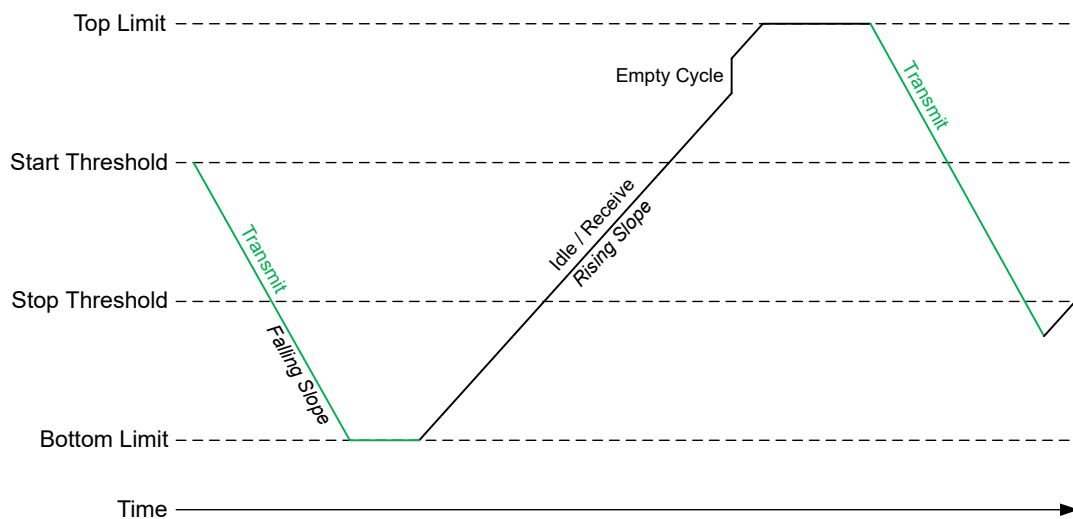
The credit counter will saturate and stop accumulating credits when the limit set by the Top Limit (TOPLIMIT) field in the Credit Based Shaper Top Limit High/Low (CBSTPLMTH/CBSTPLMTL) registers is reached. Likewise, the credit counter will saturate and stop losing credits at the limit set by the Bottom Limit (BOTLIMIT) field in the Credit Based Shaper Bottom Limit High/Low (CBSBTLMTH/CBSBTLMTL) registers. This prevents the credit counter from incrementing or decrementing into an overflow condition. The saturation of the credit counter also prevents the PHY from delaying transmission of a packet too long or transmitting a burst of packets. For example, the PHY may lose a significant number of credits by transmitting a maximal size packet. If the credit counter were not limited by a lower bound, it may take a significant amount of time for the PHY to accumulate enough credits to transmit another packet. Similarly, if the PHY has not transmitted in a long time, it may accumulate too many credits allowing it to transmit multiple frames if the credit counter were not limited by an upper bound. By controlling the top and bottom limits of the credit counter, the credit based shaper may be configured to transmit at the desired rate.

For debug or monitoring purposes, the current value of the credit counter may be obtained by reading the Credit Counter (CREDITCTR) field of the Credit Based Shaper Counter High/Low (CBSCRCTR/CBSCRCTRL) registers.



**Restriction:** To prevent undesirable traffic shaping behavior, the credit based shaper should not be used in conjunction with PLCA transmit opportunity skipping, or with PLCA burst mode.

**Figure 7-1.** Credit Based Shaping Example



**Related Links**

[11.5.45. CBSCTRL](#)  
[11.5.36. CBSSTTHH](#)  
[11.5.37. CBSSTTHL](#)  
[11.5.34. CBSSPTHH](#)  
[11.5.35. CBSSPTHL](#)  
[11.5.38. CBSSLPCTL](#)  
[11.5.39. CBSTPLMTH](#)  
[11.5.40. CBSTPLMTL](#)  
[11.5.41. CBSBTLMTH](#)  
[11.5.42. CBSBTLMTL](#)  
[11.5.43. CBSCRCTRH](#)  
[11.5.44. CBSCRCTRL](#)

## 7.5 Signal Quality Indicator (SQI)

The channel Signal Quality Indication (SQI) provides an indication of channel quality between nodes on the network segment. In the LAN8650/1, the SQI implementation is designed to be compatible with the OPEN Alliance specification for advanced diagnostic features for automotive Ethernet PHYs.

The SQI is determined by accumulating statistics on received data. When PLCA is used, a single node is selected by using the Transmit Opportunity ID (TOID) bit field of the SQI Configuration 0 (SQICFG0); the SQI is then computed from the data received only during that transmit opportunity. When PLCA is not enabled, this field should be set to request that the SQI will be computed over all received data. Statistics are calculated on the selected data and the resulting quality index is stored in the SQI Value (SQIVAL) field of the SQI Status 0 (SQISTS0) register in eight levels (between '000' = worst value and '111' = best value).

During the accumulation of statistics, it is possible that an error could occur. Such an error is indicated by setting bits in two different registers: the SQI Error (SQIERR) bit in the SQI Status 0 (SQISTS0) register and the SQI status bit in the Status 1 (STS1) register. In addition, an SQI error can be selected to assert the IRQ\_N pin by clearing the SQI Interrupt Mask (SQIM) bit in the Interrupt Mask 1 (IMSK1) register.



**Important:** When an SQI measurement error has been detected, receive statistic accumulation is halted and the SQI Enable bit must be written to '0' before starting another SQI measurement.

The SQI feature operates in one of two modes. Polling mode is used for taking a single measurement or when comparing performance between multiple channels. Threshold alert mode is used to monitor one TOID continuously and provide an interrupt should SQI drop below a limit. These modes are described in the following sections.

### Programming Model - Polling

In polling mode, the station controller polls the device to identify when a new SQI estimation is available. Polling mode is selected by setting the SQI Interrupt Threshold (SQIINTTHR) field of the SQI Configuration 2 (SQICFG2) to 11111b, which disables interrupts.



When writing to the configuration registers below, use read-modify-write operations to avoid accidental updates to reserved fields.

1. Configure the PLCA transmit opportunity of the node of interest into the Transmit Opportunity ID (TOID) bit field of the SQI Configuration 0 (SQICFG0) register. If not using PLCA, the value 0xFF should be used so that the SQI is computed from received packets from all nodes.
2. Ensure that the SQI Interrupt Threshold (SQIINTTHR) field of the SQI Configuration 2 (SQICFG2) register is at the default value of 11111b.
3. Set the SQI Enable (SQIEN) bit to '1' in the SQI Control (SQICTL) register to start SQI measurement.
4. The SQI statistical accumulation process has completed and an SQI computed once the SQI Valid (SQIVLD) bit is set. Periodically poll both the SQIVLD and SQIERR bit until one is set.
  - If the SQIVLD bit = '1', the measured SQI is returned in the SQI Value (SQIVAL) field.
  - Else if the SQIERR bit = '1', restart the measurement:
    - i. Write a '0' to the SQI Enable bit to clear the error.
    - ii. Write a '1' to the SQI Enable to restart.



**Tip:** The time required for the SQI statistical accumulation process to complete depends on the amount of data received from the node of interest and may therefore vary significantly. A polling rate of approximately once per second is recommended.

5. The SQI Valid status bit will be cleared when read and automatically set again once a new SQI value has been determined. The application may continue to monitor the SQI for the selected transmit opportunity by returning to step #3 above and polling for the SQI Valid bit to become set again.
6. To stop SQI measurements, write a '0' to clear the SQI Enable bit.

### Programming Model - Threshold Alert Mode

In threshold alert mode, the device is configured to continually estimate the SQI and alert the station controller via an interrupt when the measured SQI falls below a specified threshold. When the SQI Interrupt Threshold is set to a value from 1 to 7, the device will assert the SQI status bit in the Status 1 (STS1) register any time the measured SQI is equal to or below the configured threshold. If the SQI Interrupt Mask (SQIM) bit is '0' in the Interrupt Mask 1 (IMSK1) register, the assertion of the SQI status bit will additionally generate an assertion on the IRQ\_N pin.



**CAUTION** When writing to the configuration registers below, use read-modify-write operations to avoid accidental updates to reserved fields.

1. Configure the PLCA transmit opportunity of the node of interest into the Transmit Opportunity ID (TOID) bit field of the SQI Configuration 0 (SQICFG0) register. If not using PLCA, the value 0xFF should be used so that the SQI is computed from received packets from all nodes.
2. Configure the SQI Interrupt Threshold (SQIINTTHR) field of the SQI Configuration 2 (SQICFG2) register for the SQI threshold at which the SQI status bit will be asserted. For example, configuring SQIINTTHR to 00101b will result in the SQI status bit being asserted when an SQI of 4 or below is measured.
3. Write a '0' to the SQI Interrupt Mask (SQIM) bit of the Interrupt Mask 1 (IMSK1) register to enable the assertion of the IRQ\_N pin when the SQI status bit is set.
4. Set the SQI Enable (SQIEN) bit to '1' in the SQI Control (SQICTL) register to enable SQI measurement.
5. When the IRQ\_N pin is asserted, read the Status 1 (STS1) register.

- If the SQIVLD bit = '1', the device measured an SQI of less than or equal to the configured threshold..
  - Else if the SQIERR bit = '1', restart the measurement:
    - i. Write a '0' to the SQI Enable bit to clear the error.
    - ii. Write a '1' to the SQI Enable to restart.
6. To stop SQI measurements, write a '0' to clear the SQI Enable bit.

**Related Links**[11.5.52. SQICTL](#)[11.5.53. SQISTS0](#)[11.5.54. SQICFG0](#)[11.5.2. STS1](#)[11.5.5. IMASK1](#)

## 7.6 Cable Fault Diagnostics

The LAN8650/1 contains hardware support for cable fault diagnostics, which can be used to support, for example, OPEN Alliance harness defect detection requirements for automotive Ethernet PHYs. Using these features, it is possible for a station controller to determine various cable failures in a multidrop network. These failures include

- Both conductors open
- Both conductors shorted together
- Both conductors shorted to power or ground

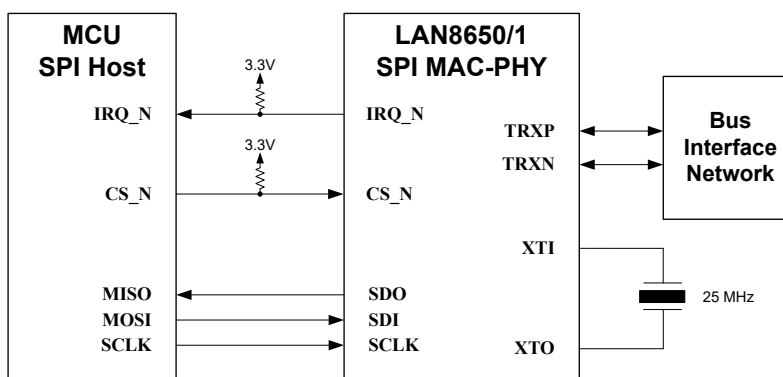
Additional information, including the software algorithm recommended for the station controller, is available under NDA.

## 8. Application Information

### 8.1 SPI Connectivity

Figure 8-1 illustrates device connectivity to the host MCU.

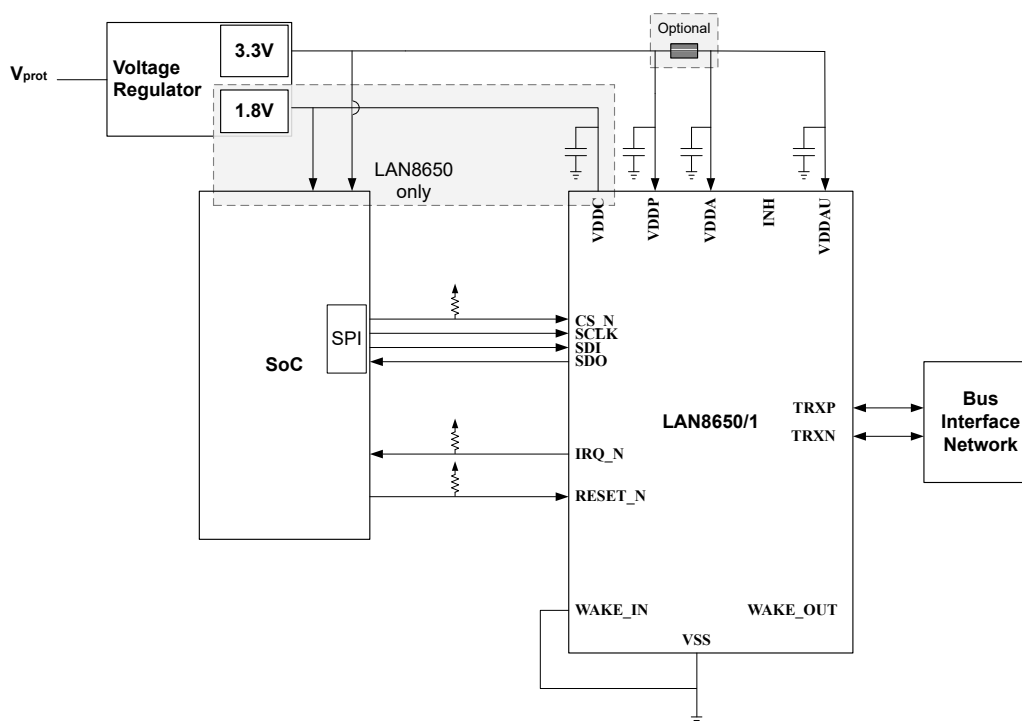
Figure 8-1. SPI Connectivity



### 8.2 System Configuration without Sleep Mode

Device connectivity without sleep mode is illustrated in the following figure. A configuration with sleep mode can be found in the Sleep Mode and System Power Management section.

Figure 8-2. Example System without Sleep Mode



#### Related Links

[4.4.1. Sleep Mode and System Power Management](#)



### 8.3 Power Connectivity

This section describes typical power configuration for the LAN8650/1 devices with the power supply architecture and recommended decoupling.

The VDDA pins supply power to the internal 3.3V analog circuits while the VDDP pins supply power to the 3.3V digital I/O pins. The internal digital logic of the LAN8650/1 operates at 1.8V. For the LAN8650, this 1.8V is supplied through the VDDC core power pins. The LAN8651 incorporates an internal 1.8V low drop-out regulator that powers the 1.8V core from the 3.3V VDDA analog power.

For applications requiring a low power sleep state and wake-up, an uninterrupted, continuous 3.3V power supply (3.3Vcont) must be connected to VDDAU to power the internal wake-up circuitry and the INH pin. The INH pin will then drive enable pins for the separate switched local power supplies for VDDA, VDDP and, for the LAN8650, VDDC.

In a design where sleep mode is not used, a continuous 3.3V power supply is not necessary and VDDAU is therefore connected to the same 3.3V power supply as VDDA. When VDDAU and VDDA are not connected to the same supply, the VDDA supply pin must never exceed the VDDAU supply pin by more than 0.5V. One approach to satisfying this power sequencing requirement is to connect a Schottky diode between the power supplies to prevent VDDA from exceeding VDDAU by more than a forward-biased voltage drop. The Schottky diode must be sized appropriately if used; the forward voltage drop must be less than 0.5V when the diode conducts current when VDDA exceeds VDDAU.

The LAN8650 has an additional restriction: the VDDC supply pin must never exceed the VDDP supply pin by more than 0.5V. A Schottky diode can also be used, as above, to ensure this requirement is met.

Proper decoupling of the LAN8650/1 power distribution network is a prerequisite for stable operation and best EMC performance. Low ESR 0.1  $\mu$ F and 0.01  $\mu$ F capacitors are placed at each of the VDDA, VDDP, and, in the case of the LAN8650, the VDDC pins. These decoupling capacitors should be located right at the pin as close as possible to minimize parasitic inductance and maximize their effectiveness. This is typically done by placing the decoupling capacitors on the opposite side of the board from the device directly under the pin and connecting them to the exposed pad ground. Priority is always given to the placement of the smaller 0.01  $\mu$ F decoupling capacitor during layout to achieve optimal effectiveness due to its lower capacitance. Each decoupling capacitor is ideally connected to the power plane through two vias to minimize interconnection inductance; decoupling capacitors should not share vias.

In addition to the decoupling capacitors at each pin, a bulk capacitance, typically 10  $\mu$ F, is placed near the LAN8650/1 in the direction of the power supply that will be supplying current. The bulk capacitors serve to provide low frequency energy that is outside the supply's response time.

For the LAN8651, a 4.7  $\mu$ F low ESR (metal film) capacitor is required on the CCOMP pin to provide external capacitive compensation to the internal 1.8V regulator. The addition of 0.1  $\mu$ F and 0.01  $\mu$ F decoupling capacitors to the CCOMP pin may be found useful, but are not required.

EMI sensitive applications requiring increased noise performance, may optionally add ferrite beads such as the Würth 742792640 to create localized power islands around the device for the VDDA, VDDAU, and VDDP supplies as illustrated in [Figure 8-4](#) and [Figure 8-5](#). When a ferrite bead is used, it should have a resistance of around 300 $\Omega$  at 100 MHz. Additionally, the ferrite bead must have a DC current rating at least twice the maximum current to be supplied to the power pins to avoid core saturation and degradation in performance. During the prototype phase, it is recommended to include the option for the ferrite beads should the need arise to populate it to improve noise immunity.

Depending on the properties of the ferrite bead, its combination with the small decoupling capacitors may cause resonant peaking at certain frequencies leading to an undesired amplification of certain frequencies of noise in the system resulting in increased electromagnetic radiation and noise coupling in form of amplitude noise and jitter. Since the ferrite bead selection is highly dependent on the noise in the system, which varies from design to design, the large bulk capacitor,



typically 10  $\mu$ F, is recommended to be placed on the device side of the ferrite bead. When ferrite beads are used, a 10  $\mu$ F bulk capacitor on the supply side of the ferrite bead is not necessary. See [Figure 8-4](#) and [Figure 8-5](#).

Ideally, the board stackup will contain a large power plane layer adjacent to a ground plane layer. The capacitance between the power and ground planes serve to provide high frequency, low inductance decoupling. When local power islands are used, the islands should be smaller planes underneath the LAN8651, again adjacent to a ground plane to provide high-frequency capacitive decoupling. The use of power tracks are discouraged but, if used, should be as short and wide as possible to minimize sheet resistance and current dependent voltage ripple at the power distribution to the pins.



**Important:** The exposed ground pad (ePAD) of the package serves as the primary ground connection of the device and must be adequately connected to the board ground plane through an array of vias as specified in the Packaging Information section.

The analog pins (WAKE\_IN, TRXP, TRXN, XTI, and XTO) must never be driven to more than the VDDAU supply. Furthermore, all other digital pins must never be driven to more than the VDDP supply. These requirements are applicable to power-up and power-down as well as normal operating conditions.

The following figures illustrate typical power configurations for the LAN8650/1.

Figure 8-3. LAN8650/1 Minimal Power Connectivity

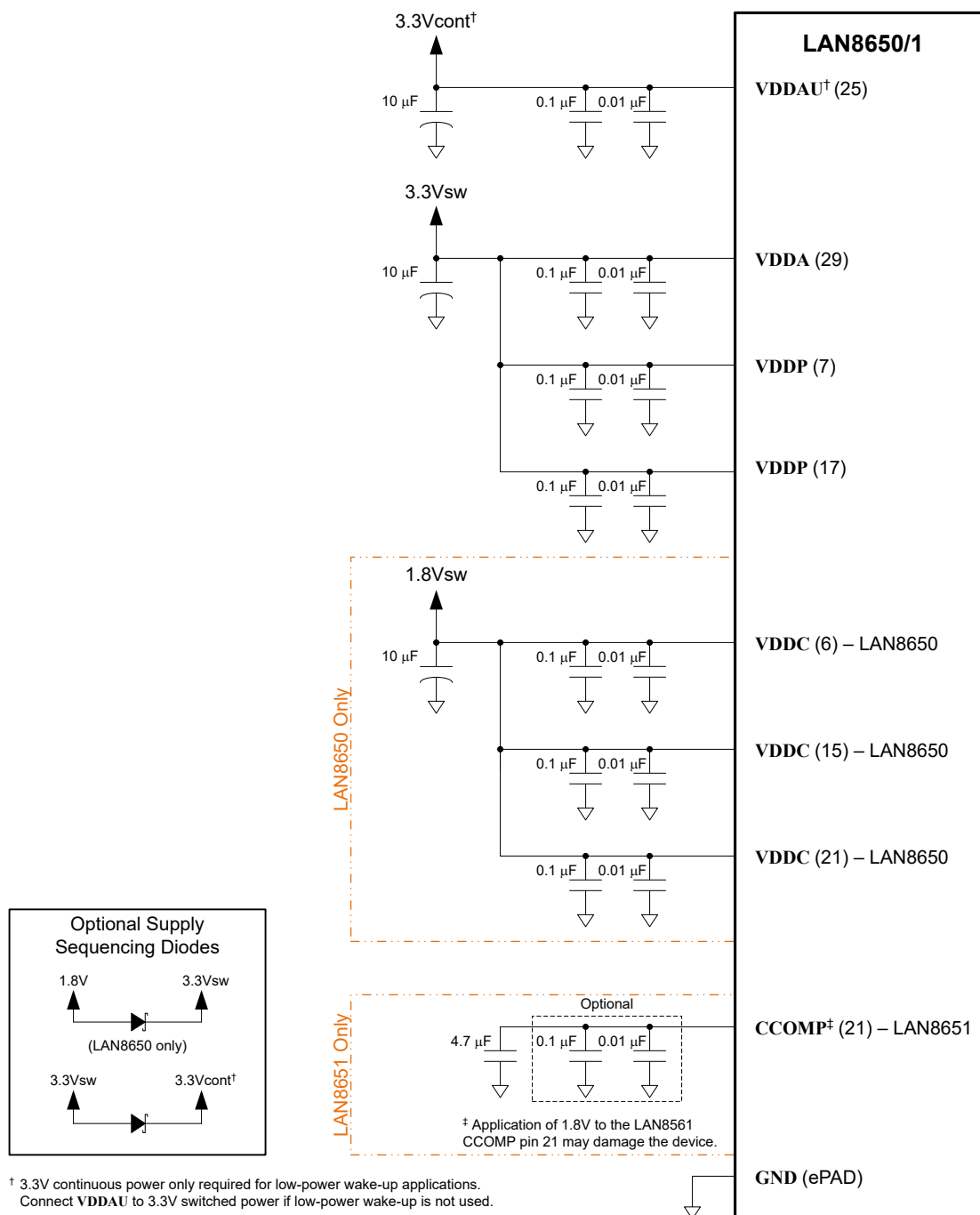


Figure 8-4. LAN8650/1 Localized Power Island Connectivity without Sleep

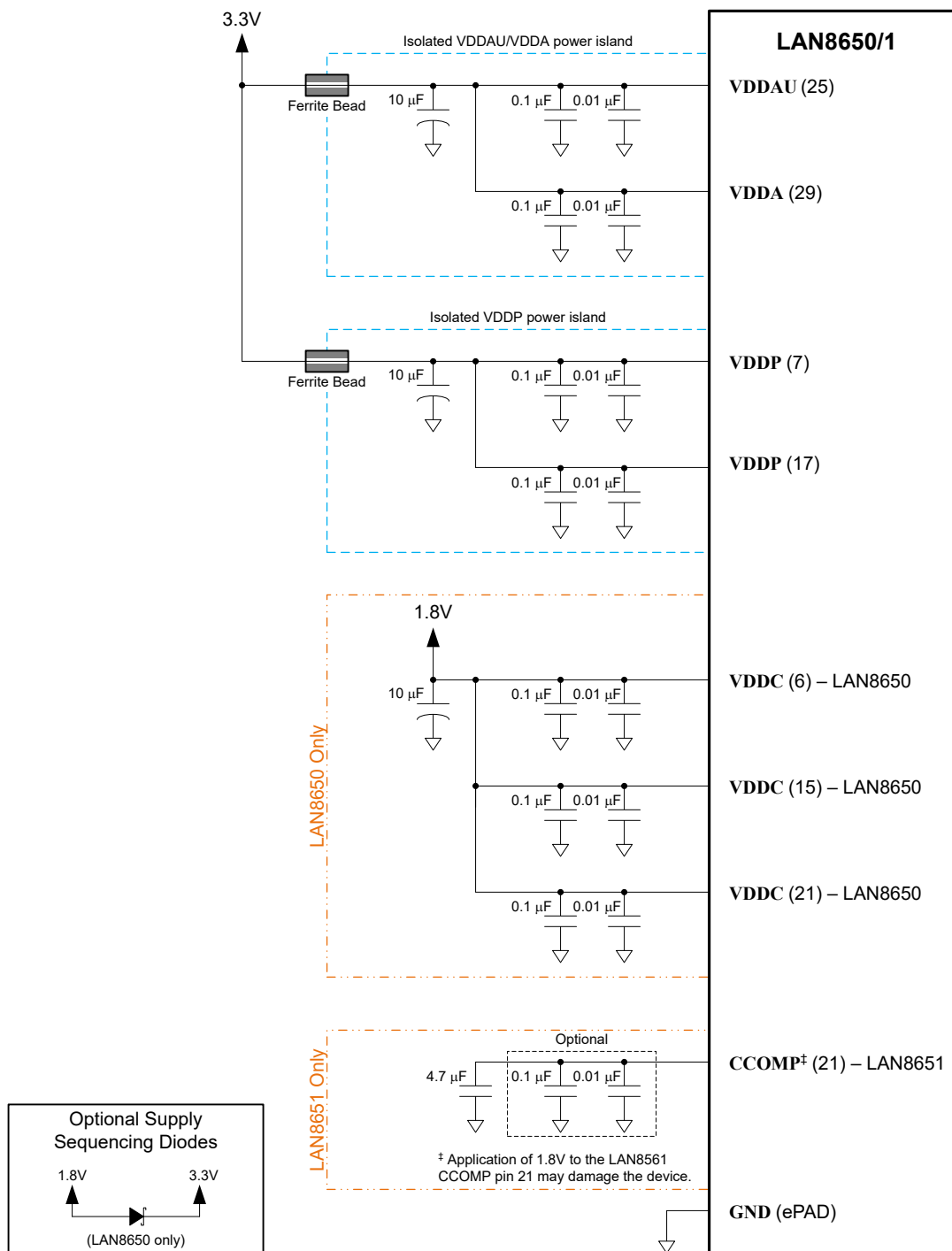
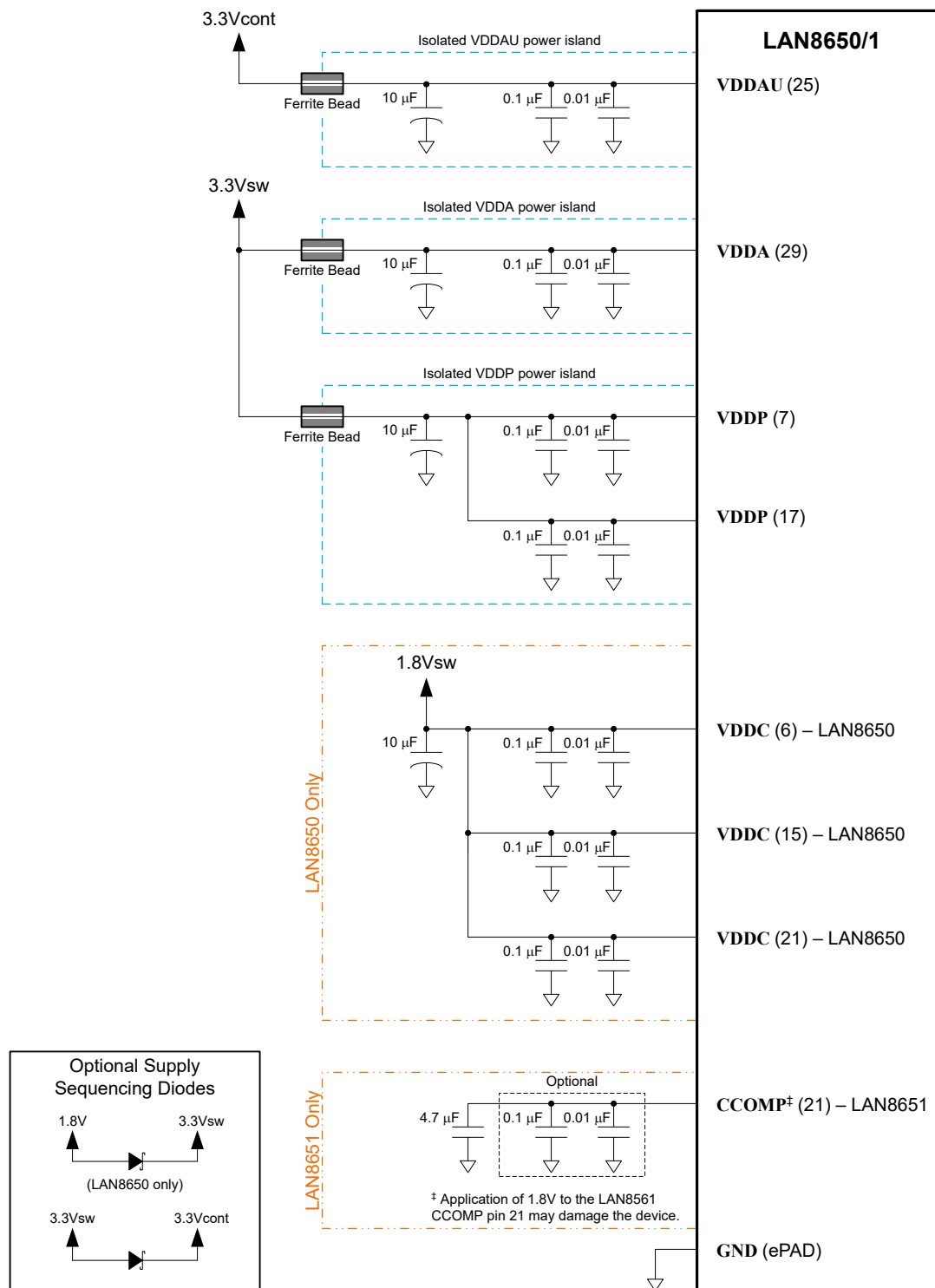


Figure 8-5. LAN8650/1 Localized Power Island Connectivity with Sleep



## 8.4 Electromagnetic Compatibility (EMC) Considerations

The latest recommendations for schematic design and PCB layout to achieve optimal EMC performance for the LAN8650/1 can be found in the *LAN86xx Bus Interface Network (BIN) Reference Design Application Note AN1718*.

### 8.4.1 Output Drive Strength Control

The LAN8650/1 digital outputs are configurable to one of four drive strengths. By changing the digital output impedance in combination with the output load, the rise and fall time of driven output signals may be adjusted to meet timing requirements while reducing the sharp transitions and ringing that can be a source of unwanted radiated emissions. The pin output drive strength is configurable in groups based on their application as defined in the table below. The output drive level for each pin group is configured within the Pad Control (PADCTRL) register. The output drive currents are specified in the DC Specifications section.

**Table 8-1.** Digital Output Drive Pin Groups

| Pin Name           | Pin Number |
|--------------------|------------|
| <b>Pin Group 1</b> |            |
| SDO                | 10         |
| <b>Pin Group 2</b> |            |
| IRQ_N              | 9          |
| DIOB0              | 16         |
| DIOB1              | 14         |
| <b>Pin Group 3</b> |            |
| DIOA0              | 18         |
| DIOA1              | 19         |
| DIOA2              | 20         |
| DIOA3              | 22         |
| DIOA4              | 23         |
| WAKE_OUT           | 24         |

#### Related Links

[11.6.3. PADCTRL](#)

[9.5. DC Specifications \(other than 10BASE-T1S PMA\)](#)

## 8.5 PLCA Collision Detection

When nodes in a mixing segment are properly configured for PLCA operation there will be no physical collisions. However, under certain conditions, including mixing segments with significant inherent noise due to reflections, and systems under high electromagnetic stress, false collisions may be detected. The false detection of late collisions will result in the transmitting node dropping the packet. As packets are typically received correctly in these conditions, it is recommended to disable collision detection at any time that PLCA is enabled and active. Collision detection is disabled by writing a zero to the Collision Detect Enable (CDEN) bit in the Collision Detector Control 0 (CDCTL0) register.

**Note:** Collision detection must be enabled when the node is operating purely CSMA/CD when PLCA is disabled or inactive.

#### Related Links

[11.5.51. CDCTL0](#)

## 8.6 Crystal Oscillator Selection

Oscillator margin is a measure of the stability of an oscillator circuit, and is defined in [Equation 8-1](#) as the ratio of the oscillator's negative resistance ( $R_{\text{NEG}}$ ) to the crystal's ESR ( $R_{\text{ESR}}$ ).

**Equation 8-1.** Crystal Oscillator Margin Measurement

$$\text{Margin} = \frac{|R_{\text{NEG}}|}{R_{\text{ESR}}} = \frac{|R_{\text{VAR}}| + R_{\text{ESR}}}{R_{\text{ESR}}}$$

The negative resistance can be measured by placing a variable resistor ( $R_{\text{VAR}}$ ) in series with the crystal and finding the largest resistor value where the crystal still starts up properly. This point would be just below where the oscillator does not start-up or where the start-up time is excessively long. Ideally, oscillator margin should be greater than 10, and should be at least 5. Smaller oscillator margin can affect the ability of the oscillator to start up.

The load capacitance,  $C_L$ , which is specified when ordering the crystal, is calculated from the capacitance on each leg of the crystal,  $C_x$ , combined with the stray capacitance,  $C_{\text{stray}}$ , which is contributed by PCB traces and chip pins.  $C_{\text{stray}}$  is usually in the range of 2pF to 5pF. The clock circuit requires that both crystal pins have matching  $C_x$ .  $C_L$  can then be calculated from

**Equation 8-2.** Crystal Load Capacitance

$$C_L = \frac{1}{2}C_x + C_{\text{stray}}$$

Larger capacitors also have a negative effect on oscillator margin. It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XTI/XTO). The transconductance gain ( $g_m$ ) of the internal inverting amplifier is nominally 18.2 mS.

The crystal cut and tolerance value listed in the Crystal Specifications section are typical values and may be changed to suit differing system requirements. Higher ESR values (than those listed in Crystal Specifications) run the risk of having start-up problems and should be thoroughly tested before being used. Contact the crystal manufacturer for more information.

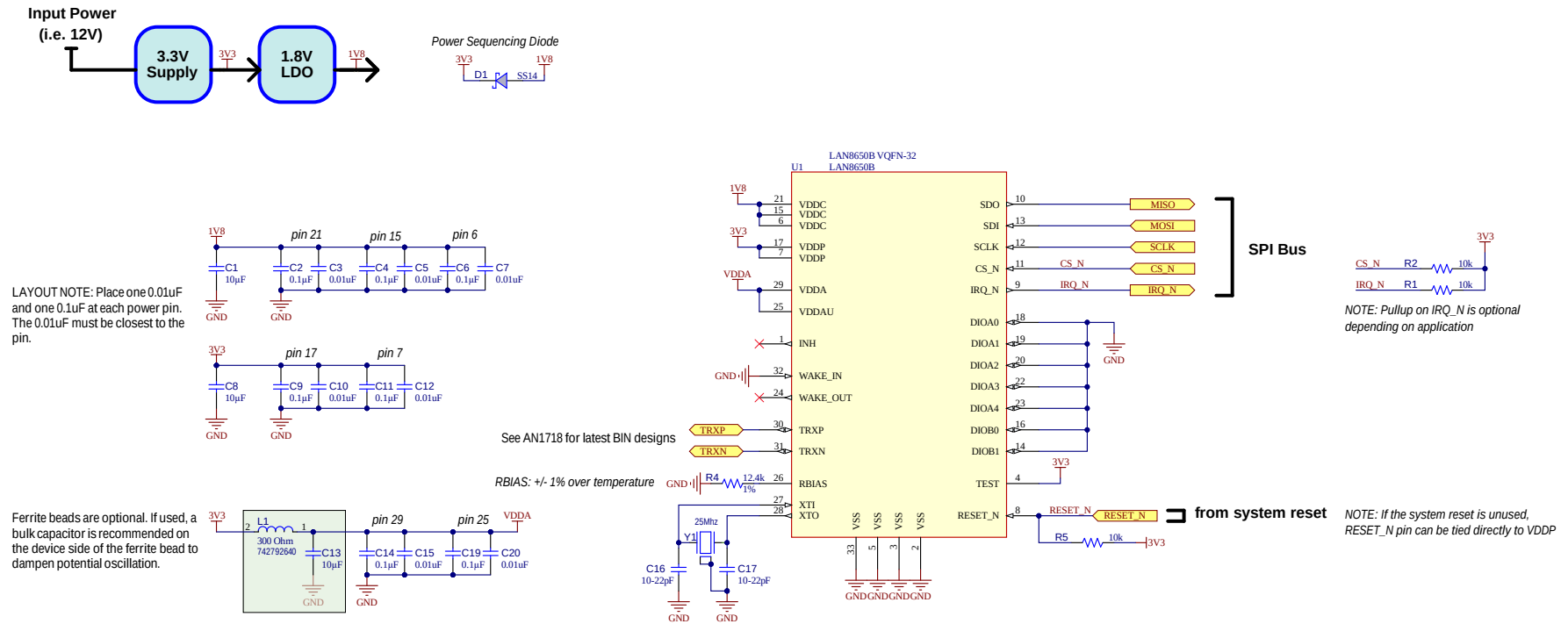
### Related Links

[9.7. Crystal Specifications](#)

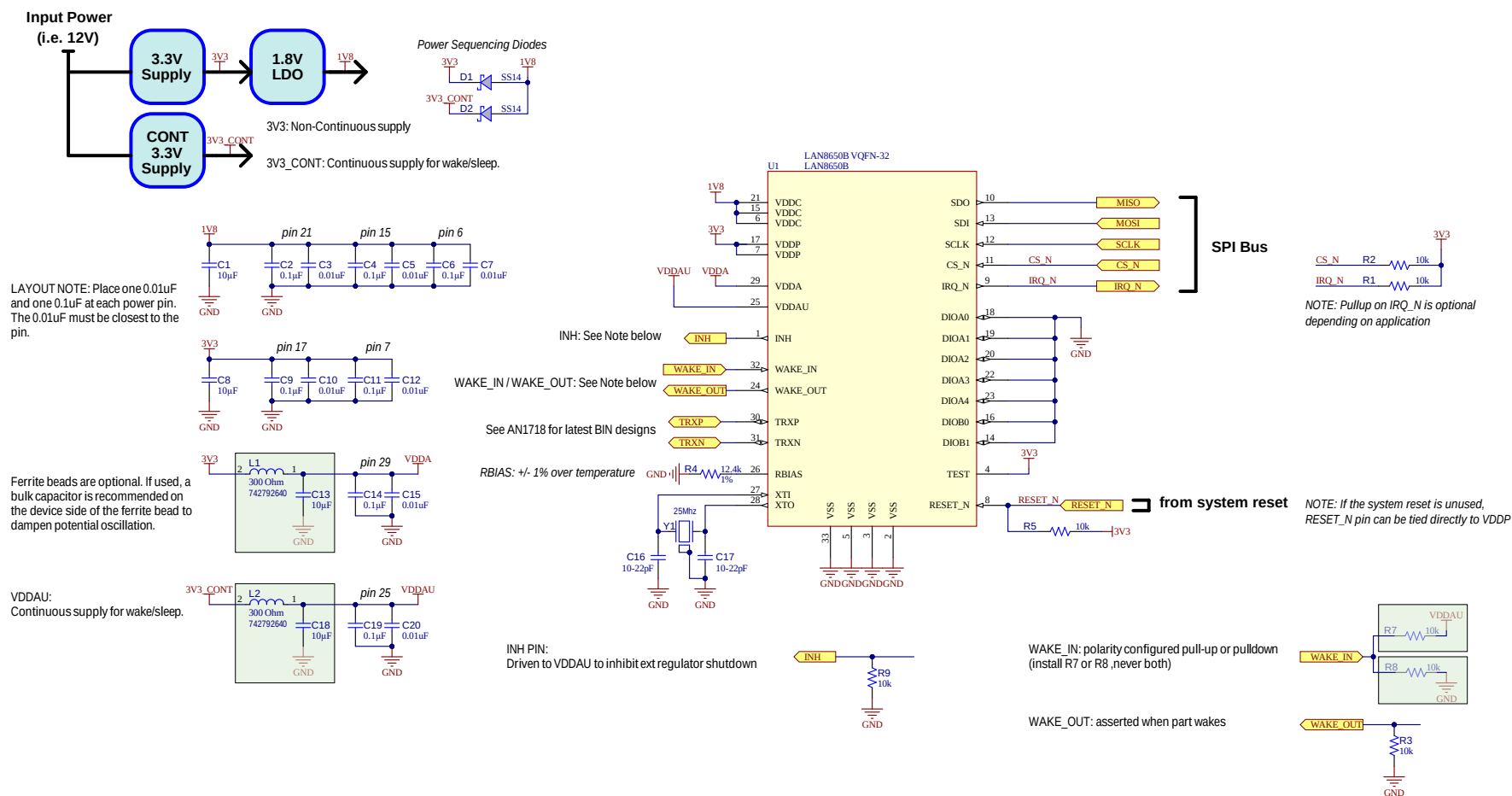
## 8.7 Reference Schematics

The schematics on the following pages contain example reference implementations of the LAN8650/1. Engineers may wish to include series termination resistors near digital output pins to aid in matching the driver and PCB trace impedance. At a minimum, a series 100 nF coupling capacitor (not shown) is needed on each of the TRXP and TRXN pins. Additional bus interface network (BIN) details are contained in a separate *LAN86xx Bus Interface Network (BIN) Reference Design Application Note AN1718*.

**Figure 8-6. LAN8650 Reference Schematic (No Sleep/Wake)**

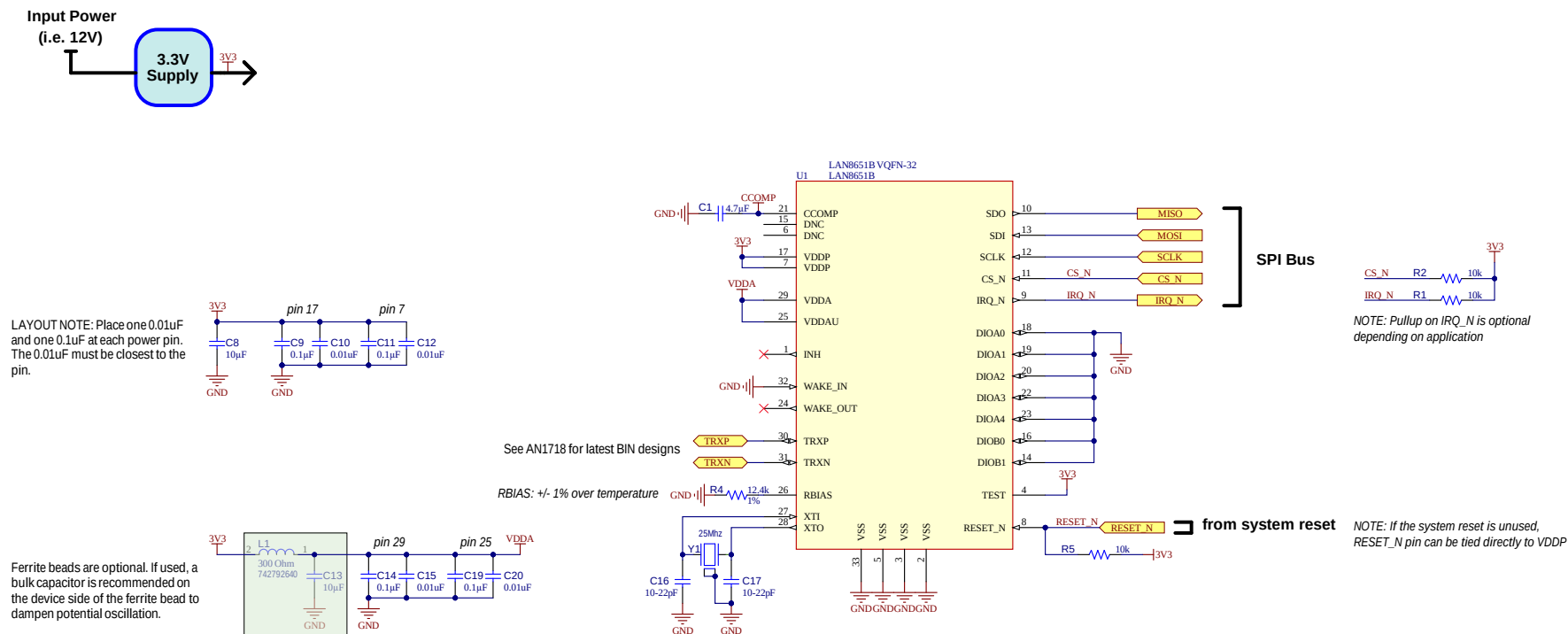


**Figure 8-7. LAN8650 Reference Schematic (With Sleep/Wake Support)**

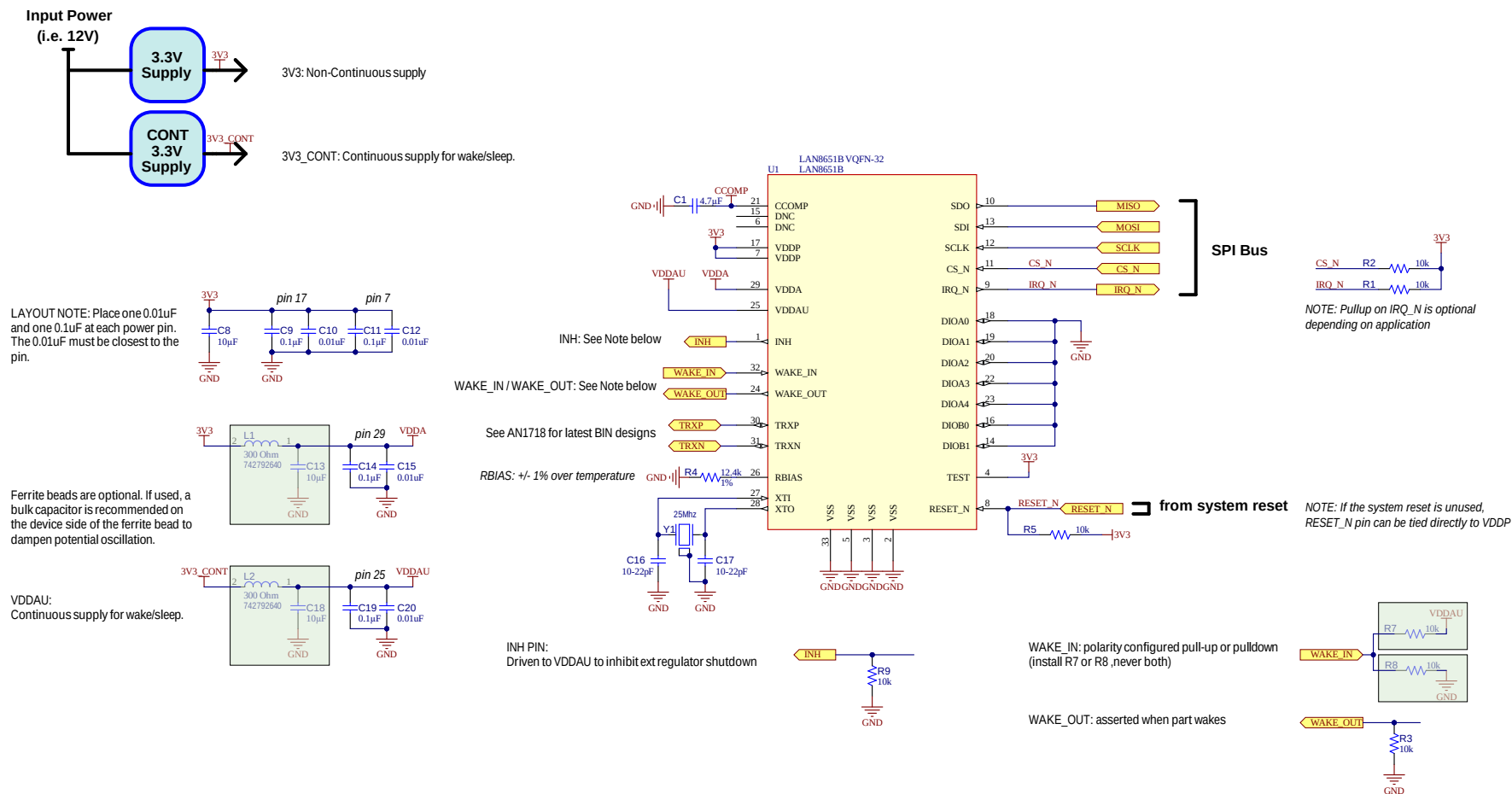




**Figure 8-8. LAN8651 Reference Schematic (No Sleep/Wake)**



**Figure 8-9. LAN8651 Reference Schematic (With Sleep/Wake Support)**



## 9. Operational Characteristics

### 9.1 Absolute Maximum Ratings

Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Operating Conditions, DC Specifications, or any other applicable section of this specification is not implied.



**Attention:** Exposure at or above these limits may damage the device.

**Table 9-1.** Absolute Maximum Ratings

| Parameter                       | Symbol                         | Min  | Max         | Units | Notes        |
|---------------------------------|--------------------------------|------|-------------|-------|--------------|
| Power Supply Voltage:           |                                |      |             |       | Note 1       |
| Core (VDDC)                     |                                | -0.5 | 2.5         | V     | LAN8650 only |
| Digital I/O (VDDP)              |                                | -0.5 | 3.9         | V     |              |
| Analog (VDDA)                   |                                | -0.5 | 3.9         | V     |              |
| Continuous (VDDAU)              |                                | -0.5 | 3.9         | V     |              |
| Voltage applied to pins:        |                                |      |             |       |              |
| TRXP, TRXN                      | $V_{TRXP/N}$                   | -27  | 42          | V     | Note 2       |
| TRXP/TRXN (differential)        | $V_{DIFF}$                     | -25  | 25          | V     |              |
| XTI/REFCLKIN, RBIAS             |                                | -0.5 | VDDA + 0.5  | V     |              |
| WAKE_IN                         |                                | -0.5 | VDDAU + 0.5 | V     |              |
| All other pins                  |                                | -0.5 | VDDP + 0.5  | V     |              |
| Junction Temperature Under Bias | $T_j$                          | -40  | 150         | °C    |              |
| Storage Temperature             | $T_{stg}$                      | -55  | 150         | °C    |              |
| Lead Temperature Range          | Refer to JEDEC Spec. J-STD-020 |      |             |       |              |
| ESD according to IBEE CAN EMC   |                                |      |             |       | Note 3       |
| TRXP, TRXN (to VSS)             |                                | -8   | +8          | kV    | Note 4       |
| ESD Human Body Model            |                                |      |             |       |              |
| TRXP, TRXN (to VSS)             |                                | -8   | +8          | kV    |              |
| All other pins                  |                                | -2   | +2          | kV    |              |
| ESD Charge Device Model         |                                | -1   | +1          | kV    | AEC-Q100-011 |

**Notes:**

1. When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.
2. Voltage applied to pins must remain below 3.9V.
3. IBEE CAN EMC test specification following IEC 62228, IEC 61000-4-2: (330  $\Omega$ /150 pF)
4. Test specification following JESD22-A114/AEC-Q100-002: (1.5 k $\Omega$ /100 pF)

## 9.2 Operating Conditions

Proper operation of the device is guaranteed only within the ranges specified in this section.

**Table 9-2.** Operating Conditions

| Description                                                                                                              | Symbol         | Min   | Max         | Units | Notes  |
|--------------------------------------------------------------------------------------------------------------------------|----------------|-------|-------------|-------|--------|
| Power Supply Voltage:                                                                                                    |                |       |             |       |        |
| Core I/O (VDDC)                                                                                                          |                | 1.71  | 1.89        | V     | Note 1 |
| Digital I/O (VDDP)                                                                                                       |                | 3.135 | 3.465       | V     |        |
| Continuous (VDDAU)                                                                                                       |                | 3.135 | 3.465       | V     |        |
| Analog (VDDA)                                                                                                            |                | 3.135 | 3.465       | V     | Note 2 |
| Maximum Input Voltage:                                                                                                   |                |       |             |       |        |
| XTI, RBIAS                                                                                                               |                | -0.3  | VDDA + 0.3  | V     |        |
| WAKE_IN                                                                                                                  |                | -0.3  | VDDAU + 0.3 | V     |        |
| All other pins                                                                                                           |                | -0.3  | VDDP + 0.3  | V     |        |
| Power Supply Ramp Rate                                                                                                   |                | 300   |             | μs/V  |        |
| Ambient Operating Temperature (Still Air)                                                                                | T <sub>A</sub> | -40   | +125        | °C    |        |
| <b>Notes:</b>                                                                                                            |                |       |             |       |        |
| 1. LAN8650 only: The VDDC pin must not exceed the VDDP pin by more than 0.5V, including during power-up and power-down.. |                |       |             |       |        |
| 2. The VDDA pin must never exceed the VDDAU pin by more than 0.5 V, including during power-up and power-down.            |                |       |             |       |        |

## 9.3 Power Consumption

All parameters tested unless otherwise noted

**Table 9-3.** LAN8650 Current Consumption and Power Dissipation

| Supply                                                                                                   | Current |         |       | Power   |         |       | Notes                                       |
|----------------------------------------------------------------------------------------------------------|---------|---------|-------|---------|---------|-------|---------------------------------------------|
|                                                                                                          | Typical | Maximum | Units | Typical | Maximum | Units |                                             |
| Sleep                                                                                                    |         |         |       |         |         |       |                                             |
| VDDAU                                                                                                    | 40      | 56      | μA    | 132     | 194     | uW    | Notes <a href="#">1</a> , <a href="#">2</a> |
| Normal operation                                                                                         |         |         |       |         |         |       |                                             |
| VDDAU                                                                                                    | 570     |         | μA    |         |         |       | Note <a href="#">3</a>                      |
| VDDA                                                                                                     | 26      | 35      | mA    |         |         |       | Note <a href="#">3</a>                      |
| VDDP                                                                                                     | 5       |         | mA    |         |         |       | Note <a href="#">4</a>                      |
| VDDC                                                                                                     |         | 25      |       |         |         |       |                                             |
| Power                                                                                                    |         |         |       | 137     | 167     | mW    | Note <a href="#">5</a>                      |
| Notes:                                                                                                   |         |         |       |         |         |       |                                             |
| 1. Current for sleep mode is only for VDDAU. All other power pins are assumed to be unpowered.           |         |         |       |         |         |       |                                             |
| 2. Maximum sleep power calculated for VDDAU = 3.465V                                                     |         |         |       |         |         |       |                                             |
| 3. Continuous transmission.                                                                              |         |         |       |         |         |       |                                             |
| 4. Typical VDDP current when receiving data. Current is lower in other modes.                            |         |         |       |         |         |       |                                             |
| 5. Maximum power occurs during continuous transmission with VDDC = 1.89V and all power supplies = 3.465V |         |         |       |         |         |       |                                             |

**Table 9-4.** LAN8651 Maximum Current Consumption and Power Dissipation

| Supply                                                                                         | Current |         |       | Power   |         |       | Notes                                       |
|------------------------------------------------------------------------------------------------|---------|---------|-------|---------|---------|-------|---------------------------------------------|
|                                                                                                | Typical | Maximum | Units | Typical | Maximum | Units |                                             |
| Sleep                                                                                          |         |         |       |         |         |       |                                             |
| VDDAU                                                                                          | 40      | 56      | μA    | 132     | 194     | uW    | Notes <a href="#">1</a> , <a href="#">2</a> |
| Normal operation                                                                               |         |         |       |         |         |       |                                             |
| VDDAU                                                                                          | 570     |         | μA    |         |         |       | Note <a href="#">3</a>                      |
| VDDA                                                                                           | 41      | 55      | mA    |         |         |       | Note <a href="#">3</a>                      |
| VDDP                                                                                           | 5       |         | mA    |         |         |       | Note <a href="#">4</a>                      |
| Power                                                                                          |         |         |       | 164     | 200     | mW    | Note <a href="#">5</a>                      |
| Notes:                                                                                         |         |         |       |         |         |       |                                             |
| 1. Current for sleep mode is only for VDDAU. All other power pins are assumed to be unpowered. |         |         |       |         |         |       |                                             |
| 2. Maximum sleep power calculated for VDDAU = 3.465V                                           |         |         |       |         |         |       |                                             |
| 3. Continuous transmission.                                                                    |         |         |       |         |         |       |                                             |
| 4. Typical VDDP current when receiving data. Current is lower in other modes.                  |         |         |       |         |         |       |                                             |
| 5. Maximum power occurs during continuous transmission with all supplies at 3.465              |         |         |       |         |         |       |                                             |

### Related Links

[4.4. Sleep Mode](#)

## 9.4 Package Thermal Specifications

**Note:** Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JE5D51.

**Table 9-5.** LAN8650/1 Package Thermal Parameters (32-VQFN)

| Parameter                  | Symbol        | Value | Units | Notes     |
|----------------------------|---------------|-------|-------|-----------|
| Junction-to-Ambient        | $\Theta_{JA}$ | 43    | °C/W  | Still air |
| Junction-to-Top-of-Package | $\Psi_{JT}$   | 0.6   | °C/W  | Still air |
| Junction-to-Case           | $\Theta_{JC}$ | 7.6   | °C/W  |           |

## 9.5 DC Specifications (other than 10BASE-T1S PMA)

All parameters tested unless otherwise noted.

**Table 9-6.** DC Electrical Characteristics (other than 10BASE-T1S PMA)

| Parameter                           | Symbol           | Min        | Typ | Max | Units | Notes                     |
|-------------------------------------|------------------|------------|-----|-----|-------|---------------------------|
| <b>VIS-VDDP Type Input Buffers</b>  |                  |            |     |     |       |                           |
| Low-Level Input Voltage             | $V_{IL}$         |            |     | 0.8 | V     |                           |
| High-Level Input Voltage            | $V_{IH}$         | 2.0        |     |     | V     |                           |
| Input Hysteresis                    | $\Delta V_{hys}$ | 25         |     | 230 | mV    | Note 1                    |
| Input Leakage                       | $I_L$            | -10        |     | 10  | μA    | $V_{IN} = VSS$ or $VDDP$  |
| Input Capacitance                   | $C_{IN}$         |            |     | 3   | pF    | Note 2                    |
| <b>VI-VDDAU Type Input Buffers</b>  |                  |            |     |     |       |                           |
| Low-Level Input Voltage             | $V_{IL}$         |            |     | 0.8 | V     |                           |
| High-Level Input Voltage            | $V_{IH}$         | 2.0        |     |     | V     |                           |
| Input Leakage                       | $I_L$            | -10        |     | 10  | μA    | $V_{IN} = VSS$ or $VDDAU$ |
| Input Capacitance                   | $C_{IN}$         |            |     | 3   | pF    |                           |
| <b>VO-VDDP Type Output Buffers</b>  |                  |            |     |     |       |                           |
| Low-Level Output                    | $V_{OL}$         |            |     | 0.4 | V     | Note 3                    |
|                                     | $I_{OL-L}$       | -0.6       |     |     | mA    | Low drive                 |
|                                     | $I_{OL-ML}$      | -1.7       |     |     | mA    | Medium-low drive          |
|                                     | $I_{OL-MH}$      | -2.6       |     |     | mA    | Medium-high drive         |
|                                     | $I_{OL-H}$       | -3.5       |     |     | mA    | High drive                |
| High-Level Output                   | $V_{OH}$         | $VDDP-0.4$ |     |     | V     | Note 4                    |
|                                     | $I_{OH-L}$       | 0.45       |     |     | mA    | Low drive                 |
|                                     | $I_{OH-ML}$      | 1.2        |     |     | mA    | Medium-low drive          |
|                                     | $I_{OH-MH}$      | 2.0        |     |     | mA    | Medium-high drive         |
|                                     | $I_{OH-H}$       | 2.9        |     |     | mA    | High drive                |
| <b>VOD-VDDP Type Output Buffers</b> |                  |            |     |     |       |                           |
| Low-Level Output                    | $V_{OL}$         |            |     | 0.4 | V     | Note 3                    |
|                                     | $I_{OL-L}$       | -0.57      |     |     | mA    | Low drive                 |
|                                     | $I_{OL-ML}$      | -1.7       |     |     | mA    | Medium-low drive          |
|                                     | $I_{OL-MH}$      | -2.8       |     |     | mA    | Medium-high drive         |
|                                     | $I_{OL-H}$       | -3.6       |     |     | mA    | High drive                |
| <b>VOH-VDDP Type Output Buffers</b> |                  |            |     |     |       |                           |
| Low-Level Output                    | $V_{OL}$         |            |     | 0.4 | V     | Note 3                    |
|                                     | $I_{OL-L}$       | -1.3       |     |     | mA    | Low drive                 |
|                                     | $I_{OL-ML}$      | -2.7       |     |     | mA    | Medium-low drive          |
|                                     | $I_{OL-MH}$      | -4.0       |     |     | mA    | Medium-high drive         |

.....continued

| Parameter                            | Symbol      | Min       | Typ | Max | Units | Notes             |
|--------------------------------------|-------------|-----------|-----|-----|-------|-------------------|
| High-Level Output                    | $I_{OL-H}$  | -5.3      |     |     | mA    | High drive        |
|                                      | $V_{OH}$    | VDDP-0.4  |     |     | V     | Note 4            |
|                                      | $I_{OH-L}$  | 1.0       |     |     | mA    | Low drive         |
|                                      | $I_{OH-ML}$ | 2.0       |     |     | mA    | Medium-low drive  |
|                                      | $I_{OH-MH}$ | 2.8       |     |     | mA    | Medium-high drive |
|                                      | $I_{OH-H}$  | 3.5       |     |     | mA    | High drive        |
| <b>VOD-VDDAU Type Output Buffers</b> |             |           |     |     |       |                   |
| High-Level Output                    | $V_{OH}$    | VDDAU-0.4 |     |     | V     |                   |
|                                      | $I_{OH}$    | 1.7       |     |     | mA    |                   |

**Notes:**

1. Characterized on samples.
2. Design parameter, not tested.
3.  $I_{OL}$  is configurable to four levels of sink current.
4.  $I_{OH}$  is configurable to four levels of source current.

## 9.6 AC Specifications

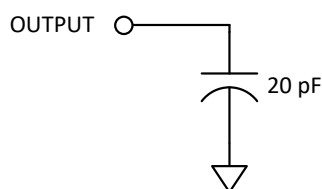
This section details the various AC timing specifications of the device. All parameters are tested unless otherwise noted.

**Note:** The Ethernet TRXP/TRXN pin timing adheres to IEEE Std 802.3cg. Refer to the IEEE Std 802.3cg specification for detailed Ethernet timing information.

### 9.6.1 Equivalent Test Load

Output timing specifications assume a 20 pF equivalent test load, unless otherwise noted, as illustrated below.

**Figure 9-1.** Output Equivalent Test Load



## 9.6.2 General Signals and Clocks

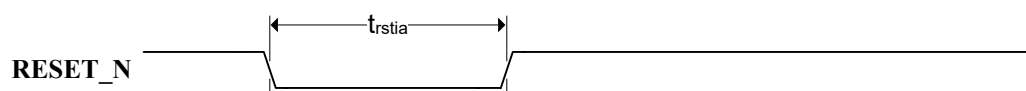
**Table 9-7. AC Electrical Characteristics (other than Ethernet PMA)**

| Parameter                        | Symbol         | Min | Typ | Max | Units | Additional Information |
|----------------------------------|----------------|-----|-----|-----|-------|------------------------|
| VO-VDDP Type Output Buffers      |                |     |     |     |       |                        |
| Output Rise Time<br>(10% to 90%) | t <sub>r</sub> |     | 23  |     | ns    | Low drive              |
|                                  |                |     | 8   |     | ns    | Medium-low drive       |
|                                  |                |     | 5   |     | ns    | Medium-high drive      |
|                                  |                |     | 3   |     | ns    | High drive             |
| Output Fall Time<br>(90% to 10%) | t <sub>f</sub> |     | 23  |     | ns    | Low drive              |
|                                  |                |     | 8   |     | ns    | Medium-low drive       |
|                                  |                |     | 5   |     | ns    | Medium-high drive      |
|                                  |                |     | 3   |     | ns    | High drive             |
| VODL-VDDP Type Output Buffers    |                |     |     |     |       |                        |
| Output Fall Time<br>(90% to 10%) | t <sub>f</sub> |     | 23  |     | ns    | Low drive              |
|                                  |                |     | 7   |     | ns    | Medium-low drive       |
|                                  |                |     | 5   |     | ns    | Medium-high drive      |
|                                  |                |     | 3   |     | ns    | High drive             |
| VOH-VDDP Type Output Buffers     |                |     |     |     |       |                        |
| Output Rise Time<br>(10% to 90%) | t <sub>r</sub> |     | 10  |     | ns    | Low drive              |
|                                  |                |     | 5   |     | ns    | Medium-low drive       |
|                                  |                |     | 4   |     | ns    | Medium-high drive      |
|                                  |                |     | 3   |     | ns    | High drive             |
| Output Fall Time<br>(90% to 10%) | t <sub>f</sub> |     | 10  |     | ns    | Low drive              |
|                                  |                |     | 5   |     | ns    | Medium-low drive       |
|                                  |                |     | 4   |     | ns    | Medium-high drive      |
|                                  |                |     | 3   |     | ns    | High drive             |
| VODH-VDDAU Type Output Buffers   |                |     |     |     |       |                        |
| Output Rise Time<br>(10% to 90%) | t <sub>r</sub> |     | 27  |     | ns    |                        |

## 9.6.3 RESET\_N Timing

The following diagram illustrates the RESET\_N timing requirements. Assertion of RESET\_N is not a requirement. However, if used, it must be asserted for the minimum period specified.

**Figure 9-2. RESET\_N Timing**



**Table 9-8. RESET\_N Timing**

| Description                  | Symbol      | Min | Typ | Max | Units   |
|------------------------------|-------------|-----|-----|-----|---------|
| RESET_N input assertion time | $t_{rstia}$ | 5   |     |     | $\mu$ s |



## 9.6.4 SPI Port

Figure 9-3. SPI Timing

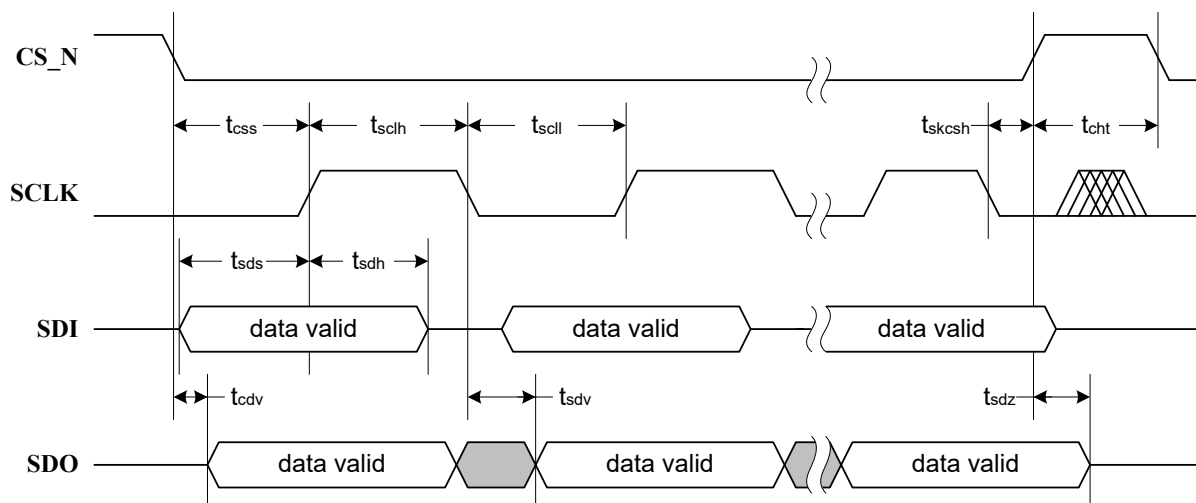


Table 9-9. SPI Port AC Operational Characteristics

| Description               | Symbol      | Min  | Max | Units |
|---------------------------|-------------|------|-----|-------|
| Maximum SCLK frequency    | $f_{sck}$   |      | 25  | MHz   |
| SCLK low time             | $t_{scll}$  | 15   |     | ns    |
| SCLK high time            | $t_{sclh}$  | 15   |     | ns    |
| SCLK low to CS_N high     | $t_{skcsh}$ | 13.5 |     | ns    |
| CS_N low to SCLK rising   | $t_{css}$   | 8    |     | ns    |
| CS_N low to SDO valid     | $t_{cdv}$   |      | 20  | ns    |
| CS_N high time            | $t_{cht}$   | 200  |     | ns    |
| SDI valid to SCLK rising  | $t_{sds}$   | 4.3  |     | ns    |
| SDI hold from SCLK rising | $t_{sdh}$   | 4    |     | ns    |
| SCLK falling to SDO valid | $t_{sdv}$   |      | 21  | ns    |
| CS_N high to SDO Hi-Z     | $t_{sdz}$   |      | 8   | ns    |

## 9.6.5 10BASE-T1S PMA Electrical Characteristics

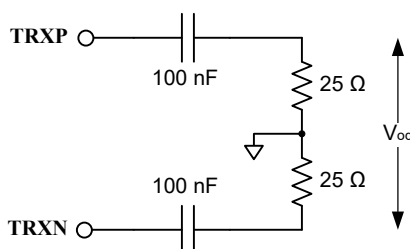
This section contains electrical characteristics of the TRXP/TRXN pins to enable the design of IEEE Std 802.3cg compliant devices.

### 9.6.5.1 10BASE-T1S PMA Transmitter Characteristics

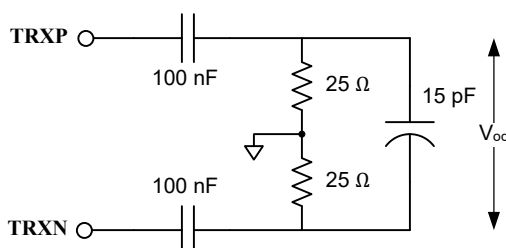
**Table 9-10.** 10BASE-T1S PMA Transmitter Electrical Characteristics

| Parameter                                       | Symbol             | Min | Typ  | Max   | Units | Additional Information               |
|-------------------------------------------------|--------------------|-----|------|-------|-------|--------------------------------------|
| Differential driver output                      | $V_{od}$           | 0.8 | 1.0  | 1.2   | V     | <a href="#">Figure 9-4</a>           |
| Cycle-to-cycle jitter                           | $t_{j(c-c)}$       |     | 0.65 | 1.2   | ns    | Note 1<br><a href="#">Figure 9-4</a> |
| Rise time, Fall time (20%-80%)                  | $t_{rtx}, t_{ftx}$ | 7.9 |      | 14.75 | ns    | Note 1<br><a href="#">Figure 9-5</a> |
| Droop                                           |                    | 0   |      | 13    | %     | Note 1<br><a href="#">Figure 9-4</a> |
| <b>Note:</b><br>1. C = Characterized on samples |                    |     |      |       |       |                                      |

**Figure 9-4.** Differential Output Test Fixture

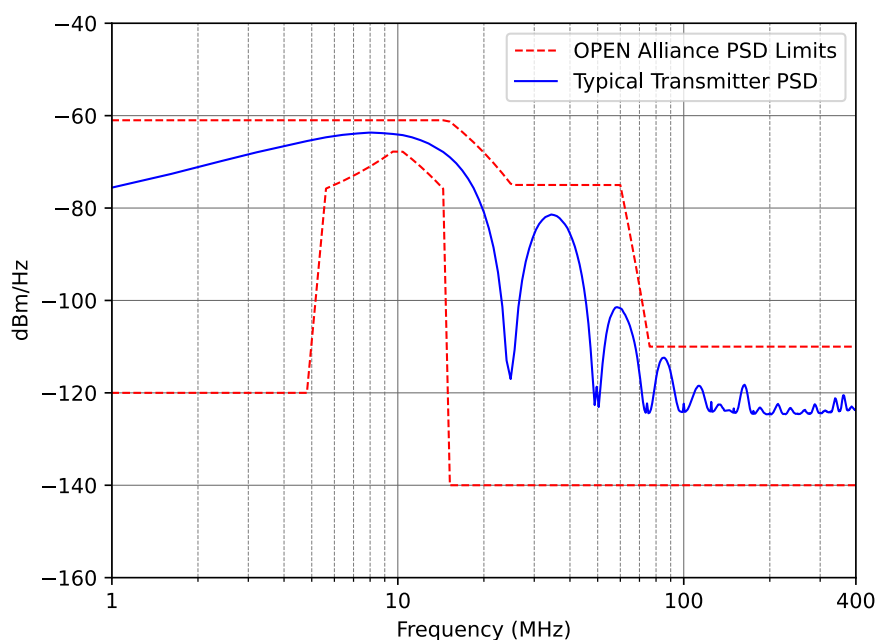


**Figure 9-5.** Transmitter Output Rise/Fall Test Fixture



**Figure 9-6.** Transmitter Power Spectral Density (Typical)

Power spectral density was measured in a multidrop configuration (50 Ω termination) as shown in [Figure 9-4](#) with the transmitter in the IEEE Transmitter PSD mask test mode 3. The upper and lower limits shown are as proposed by the OPEN Alliance *TC14 10BASE-T1S System Implementation Specification*, Version 1.0.



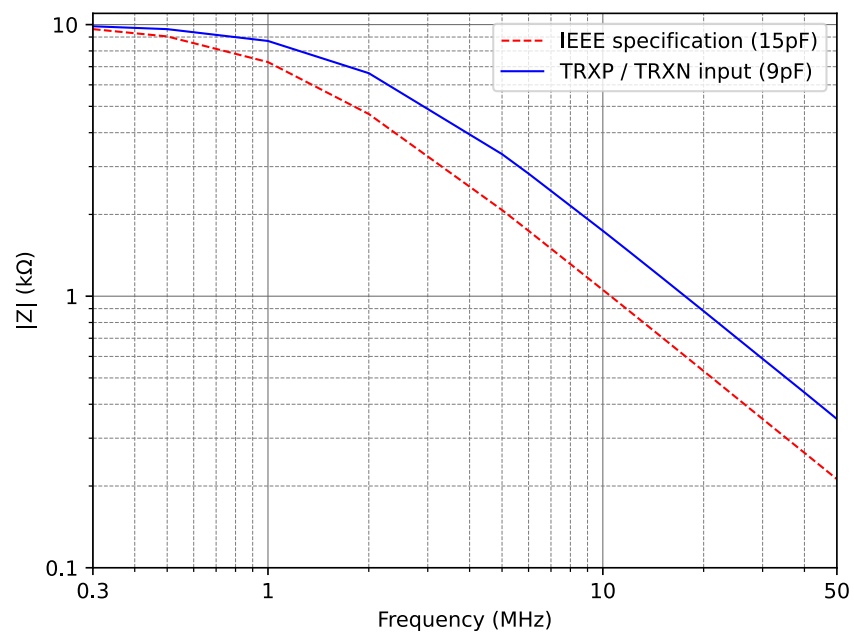
### 9.6.5.2 10BASE-T1S PMA Receiver Characteristics

**Table 9-11.** 10BASE-T1S PMA Receiver Electrical Characteristics

| Parameter                         | Symbol     | Min | Typ  | Max | Units           | Additional Information |
|-----------------------------------|------------|-----|------|-----|-----------------|------------------------|
| Receiver differential sensitivity | $V_{th}$   |     | 0    |     | mV              |                        |
| Single-ended Input Resistance     | $R_{SE}$   |     | 5.4  | 6   | k $\Omega$      | Note 1                 |
| Differential Input Resistance     | $R_{DIFF}$ |     | 14.5 |     | k $\Omega$      | Note 1                 |
| Differential input Capacitance    | $C_{DIFF}$ | 6.5 |      | 8.5 | pF              | 20 MHz<br>Note 1       |
| Common Mode Voltage Range         | $V_{CM}$   | -30 |      | +30 | V <sub>pp</sub> | 2Mhz<br>Note 1         |

**Note:**

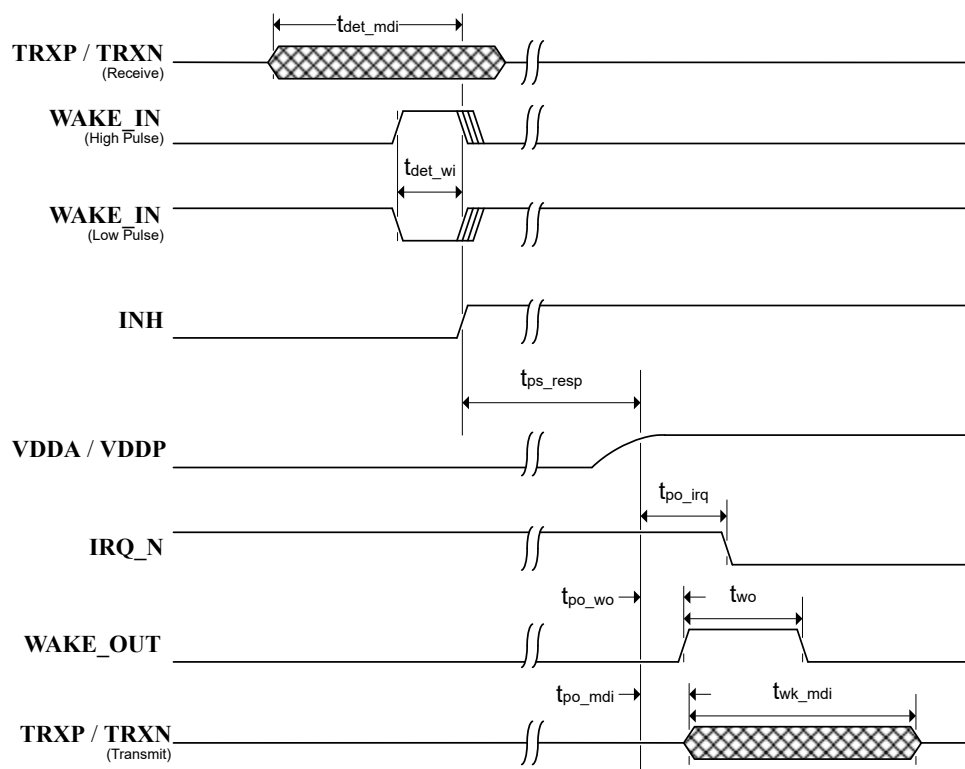
1. C = Characterized on samples

**Figure 9-7. Differential Input Impedance (Typical)**

### 9.6.6 Wake-up Signal Characteristics and Timing

The following diagram illustrates the timing characteristics as the device wakes from sleep.

**Figure 9-8. Wake Signal Timing**



**Table 9-12. 10BASE-T1S PMA Receiver Wake Signal Characteristics**

| Parameter                 | Symbol            | Min | Typ | Max | Units            | Additional Information |
|---------------------------|-------------------|-----|-----|-----|------------------|------------------------|
| MDI wake detection time   | $t_{det\_mdi}$    | 250 |     | 450 | $\mu s$          | Note 1                 |
| MDI wake signal threshold | $V_{thresh\_mdi}$ | 100 |     | 700 | mV <sub>pp</sub> | Note 2                 |

**Notes:**

1. The device will not wake if the signal duration is less than or equal to the minimum value of  $t_{det\_mdi}$ . It will wake if the signal duration is greater than or equal to the maximum value of  $t_{det\_mdi}$ . The behavior is undefined for signal duration between these limits.
2. The device will not wake if the signal amplitude is less than or equal to the minimum  $V_{thresh\_mdi}$ . It will wake if the signal amplitude is greater than or equal to the maximum value  $V_{thresh\_mdi}$ . The behavior is undefined for amplitudes between these limits.

**Table 9-13. WAKE\_IN Signal Characteristics**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Symbol        | Min | Typ | Max | Units   | Additional Information |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----|-----|-----|---------|------------------------|
| WAKE_IN detection time                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | $t_{det\_wi}$ | 15  |     | 40  | $\mu s$ | Notes 1, 2             |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>The device will not wake if the signal duration is less than or equal to the minimum value of <math>t_{det\_wi}</math>. It will wake if the signal duration is greater than or equal to the maximum value of <math>t_{det\_wi}</math>. The behavior is undefined for signal duration between these limits.</li> <li>The WAKE_IN pin is a standard VI-VDDAU type input buffer. See the section DC Electrical Characteristics (other than 10BASE-T1S PMA) for details.</li> </ol> |               |     |     |     |         |                        |

**Table 9-14. Wake Signal Time**

| Description                                                                                                                                                                                                                                                                                                                                                                          | Symbol               | Min                  | Typ | Max | Units | Additional Information |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|-----|-----|-------|------------------------|
| IRQ_N assertion time after all power supplies valid                                                                                                                                                                                                                                                                                                                                  | t <sub>po_irq</sub>  |                      | 6.6 |     | μs    |                        |
| MDI wake forward signaling activity start after all power supplies valid                                                                                                                                                                                                                                                                                                             | t <sub>po_mdi</sub>  |                      | 2   |     | μs    |                        |
| WAKE_OUT wake forward assertion time after all power supplies valid                                                                                                                                                                                                                                                                                                                  | t <sub>po_wo</sub>   |                      | 1.8 |     | μs    |                        |
| WAKE_OUT pulse width                                                                                                                                                                                                                                                                                                                                                                 | t <sub>wo</sub>      |                      | 90  |     | μs    |                        |
| MDI wake signaling time                                                                                                                                                                                                                                                                                                                                                              | t <sub>wk_mdi</sub>  |                      | 1   |     | ms    |                        |
| SPI valid after all power supplies valid                                                                                                                                                                                                                                                                                                                                             | t <sub>po_spi</sub>  |                      |     |     |       |                        |
| Power supply response time                                                                                                                                                                                                                                                                                                                                                           | t <sub>ps_resp</sub> | Application Specific |     |     |       | Note 1                 |
| <b>Note:</b><br>1. The power supply response time is the length of time from the power supplies being enabled by INH being driven high to the time the VDDP, VDDA, and VDDC supplies are high enough to release the internal power-on reset circuits. This time is dependent upon the implementation of the external power supply circuits and therefore is implementation specific. |                      |                      |     |     |       |                        |

**Related Links**

[9.5. DC Specifications \(other than 10BASE-T1S PMA\)](#)

## 9.7 Crystal Specifications

A 25 MHz crystal must be placed between XTO and XT1. This crystal should meet the requirements in [Table 9-15](#) below.

**Table 9-15.** Recommended Crystal Specifications

| Parameter                                              | Min                    | Typ    | Max  | Units | Notes     |
|--------------------------------------------------------|------------------------|--------|------|-------|-----------|
| Crystal Cut                                            | AT (typical)           |        |      |       |           |
| Crystal Oscillation Mode                               | Fundamental            |        |      |       |           |
| Crystal Calibration Mode                               | Parallel Resonant Mode |        |      |       |           |
| Frequency                                              |                        | 25.000 |      | MHz   |           |
| Tolerance                                              |                        |        | ±100 | ppm   | Note 1, 2 |
| Recommended Maximum Shunt Capacitance                  |                        |        | 6    | pF    |           |
| Recommended Load Capacitance                           |                        | 10-22  |      | pF    | Note 3    |
| Drive Level                                            |                        | 50     |      | μW    |           |
| Recommended Maximum Equivalent Series Resistance (ESR) |                        |        | 100  | Ω     |           |
| XT1/XTO Pin Capacitance                                |                        | 2      |      | pF    | Note 4    |

**Notes:**

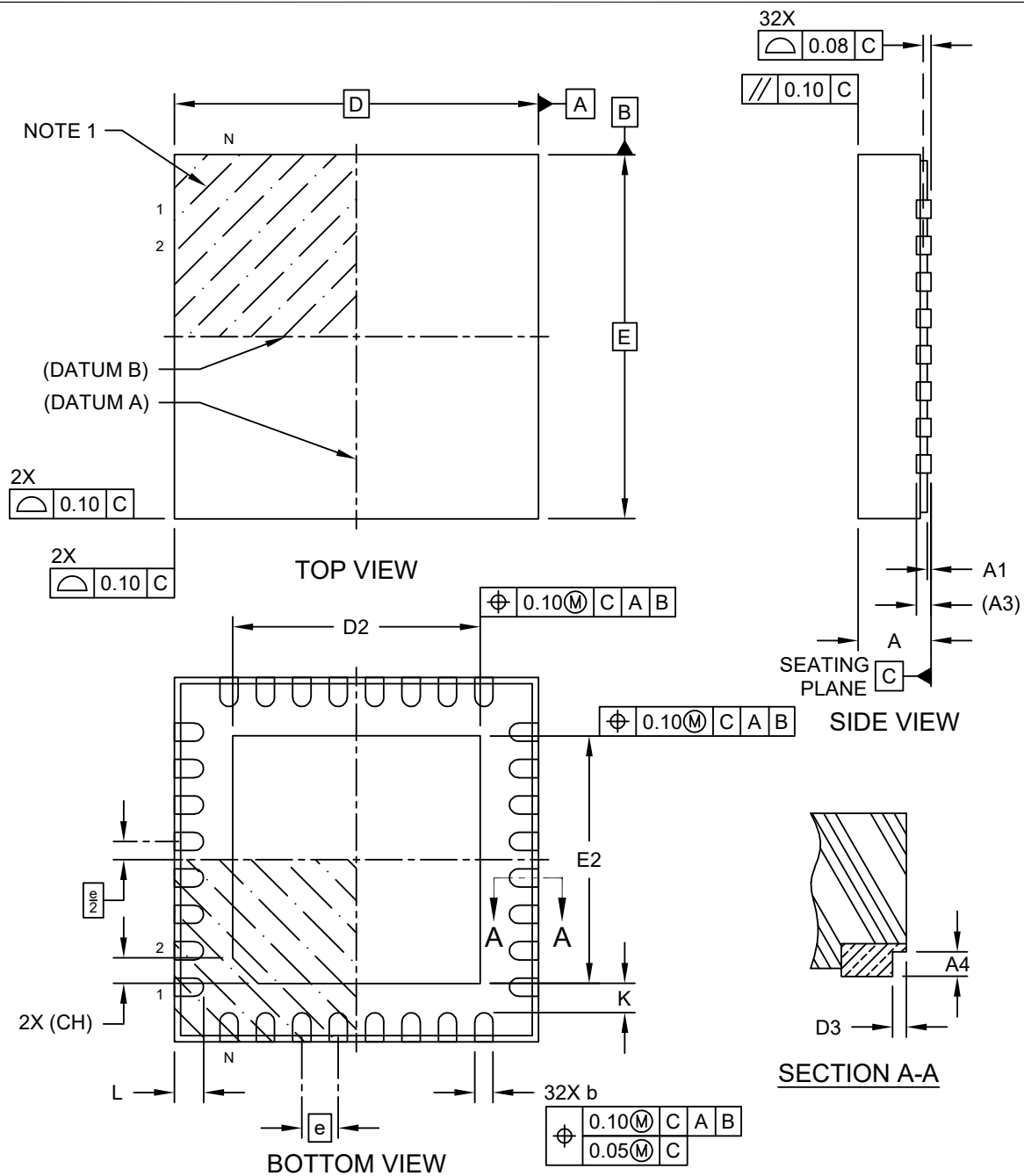
1. The total deviation for the transmitter clock frequency is specified by IEEE 802.3cg as ±100 ppm.
2. This parameter must include increased variation over the expected operational lifetime of the application (aging), temperature, and load capacitance.
3. Load capacitance per crystal terminal. The terminals should each see the same load.
4. This number includes the pad, the bond wire and the lead frame. Printed circuit board trace capacitance is not included in this value. The XT1/XTO pin and PCB trace capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

## 10. Packaging Information

## 10.1 32-VQFN

### 32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

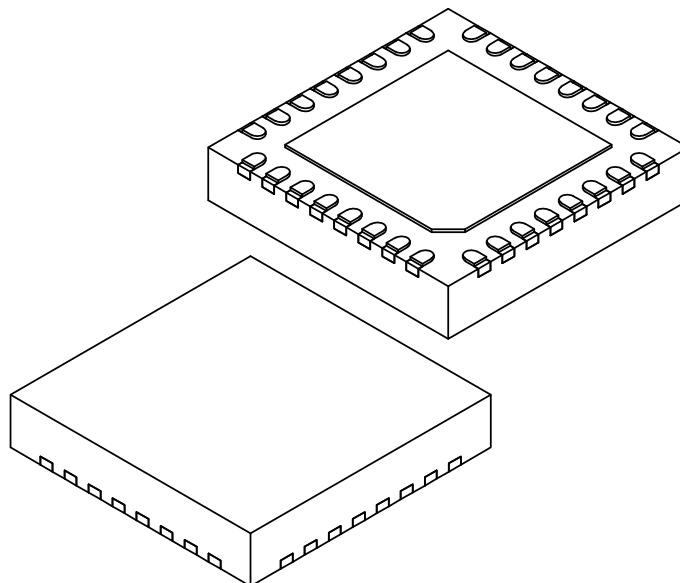


Microchip Technology Drawing C04-500 Rev B Sheet 1 of 2



### 32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                      |    | MILLIMETERS |       |       |
|----------------------------|----|-------------|-------|-------|
| Dimension Limits           |    | MIN         | NOM   | MAX   |
| Number of Terminals        | N  | 32          |       |       |
| Pitch                      | e  | 0.50 BSC    |       |       |
| Overall Height             | A  | 0.80        | 0.90  | 1.00  |
| Standoff                   | A1 | 0.00        | 0.02  | 0.05  |
| Terminal Thickness         | A3 | 0.203 REF   |       |       |
| Overall Length             | D  | 5.00 BSC    |       |       |
| Exposed Pad Length         | D2 | 3.30        | 3.40  | 3.50  |
| Overall Width              | E  | 5.00 BSC    |       |       |
| Exposed Pad Width          | E2 | 3.30        | 3.40  | 3.50  |
| Terminal Width             | b  | 0.20        | 0.25  | 0.30  |
| Terminal Length            | L  | 0.30        | 0.40  | 0.50  |
| Terminal-to-Exposed Pad    | K  | 0.20        | -     | -     |
| Exposed Pad Corner Chamfer | CH | 0.35 REF    |       |       |
| Step Height                | A4 | 0.10        | -     | 0.19  |
| Step Length                | D3 | 0.035       | 0.060 | 0.085 |

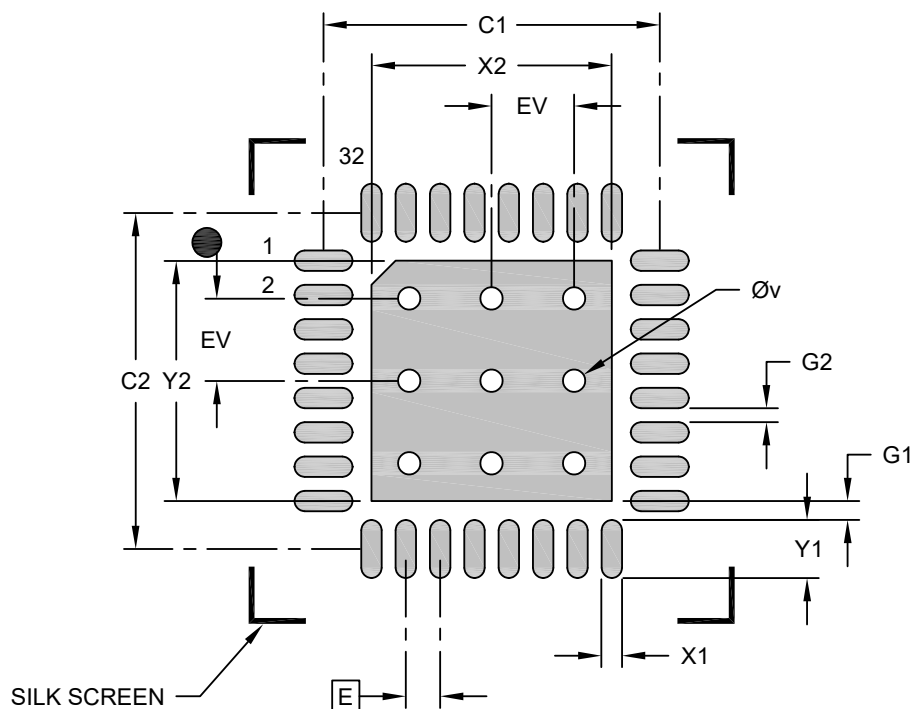
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-500 Rev B Sheet 1 of 2

**32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN]  
With 3.4 mm Exposed Pad and Stepped Wettable Flanks**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



**RECOMMENDED LAND PATTERN**

| Dimension                        | Units | MILLIMETERS |      |      |
|----------------------------------|-------|-------------|------|------|
|                                  |       | MIN         | NOM  | MAX  |
| Contact Pitch                    | E     | 0.50 BSC    |      |      |
| Optional Center Pad Width        | X2    |             |      | 3.50 |
| Center Pad Length                | Y2    |             |      | 3.50 |
| Contact Pad Spacing              | C1    |             | 4.90 |      |
| Contact Pad Spacing              | C2    |             | 4.90 |      |
| Contact Pad Width (32)           | X1    |             |      | 0.30 |
| Contact Pad Length (32)          | Y1    |             |      | 0.85 |
| Contact Pad to Center Pad (32)   | G1    | 0.20        |      |      |
| Contact Pad to Contact Pad (X28) | G2    | 0.20        |      |      |
| Thermal Via Diameter             | V     |             | 0.33 |      |
| Thermal Via Pitch                | EV    |             | 1.20 |      |

**Notes:**

- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2500 Rev B

## 10.2 Package Marking Information

Figure 10-1. LAN8650 Top Mark



**Legend:**

|         |                                                                                                                    |
|---------|--------------------------------------------------------------------------------------------------------------------|
| LAN8650 | Device Identifier                                                                                                  |
| rr      | Product Revision Code                                                                                              |
| yy      | last two digits of Assembly Year                                                                                   |
| ww      | Assembly Work Week                                                                                                 |
| nnn     | Tracking Number                                                                                                    |
| cc      | Country of Origin Abbreviation (optional)                                                                          |
| (e3)    | Pb-free JEDEC designator for Matte Tin (Sn)                                                                        |
| *       | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

Figure 10-2. LAN8651 Top Mark



**Legend:**

|         |                                                                                                                    |
|---------|--------------------------------------------------------------------------------------------------------------------|
| LAN8651 | Device Identifier                                                                                                  |
| rr      | Product Revision Code                                                                                              |
| yy      | last two digits of Assembly Year                                                                                   |
| ww      | Assembly Work Week                                                                                                 |
| nnn     | Tracking Number                                                                                                    |
| cc      | Country of Origin Abbreviation (optional)                                                                          |
| (e3)    | Pb-free JEDEC designator for Matte Tin (Sn)                                                                        |
| *       | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

## 11. Register Descriptions

The OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification defines the register memory map selector (MMS) field as a 4 bit field which allows for up to 16 different memory maps. The standard further defines which MMS should be used for required registers and register classes in a compliant device, including mapping of registers required by the 10BASE-T1S standard. The standard also includes areas for vendor specific information.

This chapter describes the device registers of the LAN8650/1, organized by MMS value.

**Table 11-1.** Control and Status Register Memory Map Selector (MMS)

| MMS   | Width (bits) | Description of Registers                                                                                                                                |
|-------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | 32/16        | <a href="#">11.1. Open Alliance 10BASE-T1x MAC-PHY Standard Registers</a><br>including <a href="#">PHY Clause 22 Basic Control and Status Registers</a> |
| 1     | 32           | <a href="#">11.2. MAC Registers</a>                                                                                                                     |
| 2     | 16           | <a href="#">11.3. PHY PCS Registers</a>                                                                                                                 |
| 3     | 16           | <a href="#">11.4. PHY PMA/PMD Registers</a>                                                                                                             |
| 4     | 16           | <a href="#">11.5. PHY Vendor Specific Registers</a>                                                                                                     |
| 5-9   | -            | Reserved                                                                                                                                                |
| 10    | 16           | <a href="#">11.6. Miscellaneous Register Descriptions</a>                                                                                               |
| 11-15 | -            | Reserved                                                                                                                                                |

For details on register bit attribute notation, refer to the section Register Bit Types.

### Related Links

[1.3. Register Bit Types](#)

## 11.1 Open Alliance 10BASE-T1x MAC-PHY Standard Registers

The OPEN Alliance standard defines Memory Map Selector (MMS) 0 as the location for control and status registers that are specific to this standard. Some of these registers are optional. The section defines the various registers implemented in the LAN8650/1.

The various Clause 22 Control and Status Registers (CSRs) are included in MMS0, beginning at offset 0xFF00. These CSRs follow the IEEE 802.3 (Clause 22.2.4) management register set. All functionality and bit definitions comply with these standards.



RESERVED address space must not be written except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Refer to the Register Bit Types section for details on register bit attribute notation.

| Address | Name       | Bit Pos. | 7           | 6       | 5        | 4      | 3              | 2       | 1        | 0       |
|---------|------------|----------|-------------|---------|----------|--------|----------------|---------|----------|---------|
| 0x00    | OA_ID      | 31:24    |             |         |          |        |                |         |          |         |
|         |            | 23:16    |             |         |          |        |                |         |          |         |
|         |            | 15:8     |             |         |          |        |                |         |          |         |
|         |            | 7:0      | MAJVER[3:0] |         |          |        | MINVER[3:0]    |         |          |         |
| 0x01    | OA_PHYID   | 31:24    |             |         |          |        | OUI[21:14]     |         |          |         |
|         |            | 23:16    |             |         |          |        | OUI[13:6]      |         |          |         |
|         |            | 15:8     |             |         |          |        | MODEL[5:4]     |         |          |         |
|         |            | 7:0      | MODEL[3:0]  |         |          |        | REVISION[3:0]  |         |          |         |
| 0x02    | OA_STDCAP  | 31:24    |             |         |          |        |                |         |          |         |
|         |            | 23:16    |             |         |          |        |                |         |          |         |
|         |            | 15:8     |             |         |          |        |                | TXFCSVC | IPRAC    | DPRAC   |
|         |            | 7:0      | CTC         | FTSC    | AIDC     | SEQC   | MINBPS[2:0]    |         |          |         |
| 0x03    | OA_RESET   | 31:24    |             |         |          |        |                |         |          |         |
|         |            | 23:16    |             |         |          |        |                |         |          |         |
|         |            | 15:8     |             |         |          |        |                |         |          |         |
|         |            | 7:0      |             |         |          |        |                |         |          | SWRESET |
| 0x04    | OA_CONFIG0 | 31:24    |             |         |          |        |                |         |          |         |
|         |            | 23:16    |             |         |          |        |                |         |          |         |
|         |            | 15:8     | SYNC        | TXFCSVE | RFA[1:0] |        | TXCTHRESH[1:0] |         | TXCTE    | RXCTE   |
|         |            | 7:0      | FTSE        | FTSS    | PROTE    | SEQE   | BPS[2:0]       |         |          |         |
| 0x08    | OA_STATUS0 | 31:24    |             |         |          |        |                |         |          |         |
|         |            | 23:16    |             |         |          |        |                |         |          |         |
|         |            | 15:8     |             |         |          | CPDE   | TXFCSE         | TTSCAC  | TTSCAB   | TTSCAA  |
|         |            | 7:0      | PHYINT      | RESETC  | HDRE     | LOFE   | RXBOE          | TXBUE   | TXBOE    | TXPE    |
| 0x09    | OA_STATUS1 | 31:24    |             |         |          | SEV    |                | TTSCMC  | TTSCMB   | TTSCMA  |
|         |            | 23:16    | TTSCOFB     | TTSCOFB | TTSCOFB  | BUSER  | UV18           | ECC     | FSMSTER  |         |
|         |            | 15:8     |             |         |          |        |                |         |          |         |
|         |            | 7:0      |             |         |          |        |                |         | TXNER    | RXNER   |
| 0x0B    | OA_BUFSTS  | 31:24    |             |         |          |        |                |         |          |         |
|         |            | 23:16    |             |         |          |        |                |         |          |         |
|         |            | 15:8     | TXC[7:0]    |         |          |        |                |         |          |         |
|         |            | 7:0      | RBA[7:0]    |         |          |        |                |         |          |         |
| 0x0C    | OA_IMASK0  | 31:24    |             |         |          |        |                |         |          |         |
|         |            | 23:16    |             |         |          |        |                |         |          |         |
|         |            | 15:8     |             |         |          | CPDEM  | TXFCSEM        | TTSCACM | TTSCABM  | TTSCAAM |
|         |            | 7:0      | PHYINTM     | RESETCM | HDREM    | LOFEM  | RXBOEM         | TXBUEM  | TXBOEM   | TXPEM   |
| 0x0D    | OA_IMASK1  | 31:24    |             |         |          | SEVM   |                | TTSCMCM | TTSCMBM  | TTSCMAM |
|         |            | 23:16    | TTSCOFB     | TTSCOFB | TTSCOFB  | BUSERM | UV18M          | ECCM    | FSMSTERM |         |
|         |            | 15:8     |             |         |          |        |                |         |          |         |
|         |            | 7:0      |             |         |          |        |                |         | TXNERM   | RXNERM  |

.....continued

| Address                 | Name          | Bit Pos. | 7              | 6          | 5          | 4          | 3                  | 2         | 1         | 0        |
|-------------------------|---------------|----------|----------------|------------|------------|------------|--------------------|-----------|-----------|----------|
| 0x10                    | TTSCAH        | 31:24    |                |            |            |            | TIMESTAMP_A[63:56] |           |           |          |
|                         |               | 23:16    |                |            |            |            | TIMESTAMP_A[55:48] |           |           |          |
|                         |               | 15:8     |                |            |            |            | TIMESTAMP_A[47:40] |           |           |          |
|                         |               | 7:0      |                |            |            |            | TIMESTAMP_A[39:32] |           |           |          |
| 0x11                    | TTSCAL        | 31:24    |                |            |            |            | TIMESTAMP_A[31:24] |           |           |          |
|                         |               | 23:16    |                |            |            |            | TIMESTAMP_A[23:16] |           |           |          |
|                         |               | 15:8     |                |            |            |            | TIMESTAMP_A[15:8]  |           |           |          |
|                         |               | 7:0      |                |            |            |            | TIMESTAMP_A[7:0]   |           |           |          |
| 0x12                    | TTSCBH        | 31:24    |                |            |            |            | TIMESTAMP_B[63:56] |           |           |          |
|                         |               | 23:16    |                |            |            |            | TIMESTAMP_B[55:48] |           |           |          |
|                         |               | 15:8     |                |            |            |            | TIMESTAMP_B[47:40] |           |           |          |
|                         |               | 7:0      |                |            |            |            | TIMESTAMP_B[39:32] |           |           |          |
| 0x13                    | TTSCBL        | 31:24    |                |            |            |            | TIMESTAMP_B[31:24] |           |           |          |
|                         |               | 23:16    |                |            |            |            | TIMESTAMP_B[23:16] |           |           |          |
|                         |               | 15:8     |                |            |            |            | TIMESTAMP_B[15:8]  |           |           |          |
|                         |               | 7:0      |                |            |            |            | TIMESTAMP_B[7:0]   |           |           |          |
| 0x14                    | TTSCCH        | 31:24    |                |            |            |            | TIMESTAMP_C[63:56] |           |           |          |
|                         |               | 23:16    |                |            |            |            | TIMESTAMP_C[55:48] |           |           |          |
|                         |               | 15:8     |                |            |            |            | TIMESTAMP_C[47:40] |           |           |          |
|                         |               | 7:0      |                |            |            |            | TIMESTAMP_C[39:32] |           |           |          |
| 0x15                    | TTSCCL        | 31:24    |                |            |            |            | TIMESTAMP_C[31:24] |           |           |          |
|                         |               | 23:16    |                |            |            |            | TIMESTAMP_C[23:16] |           |           |          |
|                         |               | 15:8     |                |            |            |            | TIMESTAMP_C[15:8]  |           |           |          |
|                         |               | 7:0      |                |            |            |            | TIMESTAMP_C[7:0]   |           |           |          |
| 0x19<br>...<br>0xFEFF   | Reserved      |          |                |            |            |            |                    |           |           |          |
| 0xFF00                  | BASIC_CONTROL | 15:8     | SW_RESET       | LOOPBACK   | SPD_SEL[0] | AUTONEGEN  | PD                 |           | REAUTONEG | DUPLEXMD |
|                         |               | 7:0      |                | SPD_SEL[1] |            |            |                    |           |           |          |
| 0xFF01                  | BASIC_STATUS  | 15:8     | 100BT4A        | 100BTXFDA  | 100BTXHDA  | 10BTFDA    | 10BTHDA            | 100BT2FDA | 100BT2HDA | EXTSTS   |
|                         |               | 7:0      |                |            | AUTONEGC   | RMTFLTD    | AUTONEGA           | LNKSTS    | JABDET    | EXTCAPA  |
| 0xFF02                  | PHY_ID1       | 15:8     | OUI[2:9]       |            |            |            |                    |           |           |          |
|                         |               | 7:0      | OUI[10:17]     |            |            |            |                    |           |           |          |
| 0xFF03                  | PHY_ID2       | 15:8     | OUI[18:23]     |            |            |            | MODEL[5:4]         |           |           |          |
|                         |               | 7:0      | MODEL[3:0]     |            |            |            | REV[3:0]           |           |           |          |
| 0xFF05<br>...<br>0xFF0C | Reserved      |          |                |            |            |            |                    |           |           |          |
| 0xFF0D                  | MMDCTRL       | 15:8     | FNCTN[1:0]     |            |            |            |                    |           |           |          |
|                         |               | 7:0      |                |            |            | DEVAD[4:0] |                    |           |           |          |
| 0xFF0E                  | MMDAD         | 15:8     | ADR_DATA[15:8] |            |            |            |                    |           |           |          |
|                         |               | 7:0      | ADR_DATA[7:0]  |            |            |            |                    |           |           |          |

## Related Links

### 1.3. Register Bit Types

**11.1.1 Identification Register****Name:** OA\_ID**Address:** 0x000

|        |             |    |    |    |             |    |    |    |
|--------|-------------|----|----|----|-------------|----|----|----|
| Bit    | 31          | 30 | 29 | 28 | 27          | 26 | 25 | 24 |
| Access | RO          | RO | RO | RO | RO          | RO | RO | RO |
| Reset  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  |
| Bit    | 23          | 22 | 21 | 20 | 19          | 18 | 17 | 16 |
| Access | RO          | RO | RO | RO | RO          | RO | RO | RO |
| Reset  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  |
| Bit    | 15          | 14 | 13 | 12 | 11          | 10 | 9  | 8  |
| Access | RO          | RO | RO | RO | RO          | RO | RO | RO |
| Reset  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  |
| Bit    | 7           | 6  | 5  | 4  | 3           | 2  | 1  | 0  |
|        | MAJVER[3:0] |    |    |    | MINVER[3:0] |    |    |    |
| Access | RO          | RO | RO | RO | RO          | RO | RO | RO |
| Reset  | 0           | 0  | 0  | 1  | 0           | 0  | 0  | 1  |

**Bits 7:4 – MAJVER[3:0] Major Version**

This field contains the major version identifier of the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification supported by this device.

**Note:** This device is designed to conform to version 1.1 of the OPEN Alliance specification.

**Bits 3:0 – MINVER[3:0] Minor Version**

This field contains the minor version identifier of the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification supported by this device.

**Note:** This device is designed to conform to version 1.1 of the OPEN Alliance specification.

### 11.1.2 PHY Identification Register

**Name:** OA\_PHYID  
**Address:** 0x001



**Attention:** This register is a reflection of the integrated PHY Clause 22 PHY\_ID0 and PHY\_ID1 registers.



**Tip:** The product ID and hardware revision number may be found in the Device Identification (11.6.6. DEVID) register.

|        |            |    |    |    |               |    |            |    |
|--------|------------|----|----|----|---------------|----|------------|----|
| Bit    | 31         | 30 | 29 | 28 | 27            | 26 | 25         | 24 |
|        | OUI[21:14] |    |    |    |               |    |            |    |
| Access | RO         | RO | RO | RO | RO            | RO | RO         | RO |
| Reset  | 0          | 0  | 0  | 0  | 0             | 0  | 0          | 0  |
| Bit    | 23         | 22 | 21 | 20 | 19            | 18 | 17         | 16 |
|        | OUI[13:6]  |    |    |    |               |    |            |    |
| Access | RO         | RO | RO | RO | RO            | RO | RO         | RO |
| Reset  | 0          | 0  | 0  | 0  | 0             | 1  | 1          | 1  |
| Bit    | 15         | 14 | 13 | 12 | 11            | 10 | 9          | 8  |
|        | OUI[5:0]   |    |    |    |               |    | MODEL[5:4] |    |
| Access | RO         | RO | RO | RO | RO            | RO | RO         | RO |
| Reset  | 1          | 1  | 0  | 0  | 0             | 0  | 0          | 1  |
| Bit    | 7          | 6  | 5  | 4  | 3             | 2  | 1          | 0  |
|        | MODEL[3:0] |    |    |    | REVISION[3:0] |    |            |    |
| Access | RO         | RO | RO | RO | RO            | RO | RO         | RO |
| Reset  | 1          | 0  | 1  | 1  | 0             | 0  | 1          | 1  |

**Bits 31:10 – OUI[21:0]** Organizationally Unique Identifier

This field contains the 19<sup>th</sup> through the 24<sup>th</sup> bits of the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22. OUI = 00800Fh

**Bits 9:4 – MODEL[5:0]** Manufacturer's Model Number

Six-bit manufacturer's integrated PHY identification number.

| Value  | Description              |
|--------|--------------------------|
| 011011 | LAN8650/1 Integrated PHY |

**Bits 3:0 – REVISION[3:0]** Manufacturer's Revision Number

Four-bit integrated PHY revision number.

| Value | Description               |
|-------|---------------------------|
| 0011  | Integrated PHY Revision 3 |



### 11.1.3 Standard Capabilities

**Name:** OA\_STDCAP**Address:** 0x0002

|        |     |      |      |      |    |             |       |       |
|--------|-----|------|------|------|----|-------------|-------|-------|
| Bit    | 31  | 30   | 29   | 28   | 27 | 26          | 25    | 24    |
| Access | RO  | RO   | RO   | RO   | RO | RO          | RO    | RO    |
| Reset  | 0   | 0    | 0    | 0    | 0  | 0           | 0     | 0     |
| Bit    | 23  | 22   | 21   | 20   | 19 | 18          | 17    | 16    |
| Access | RO  | RO   | RO   | RO   | RO | RO          | RO    | RO    |
| Reset  | 0   | 0    | 0    | 0    | 0  | 0           | 0     | 0     |
| Bit    | 15  | 14   | 13   | 12   | 11 | 10          | 9     | 8     |
| Access | RO  | RO   | RO   | RO   | RO | TXFCSVC     | IPRAC | DPRAC |
| Reset  | 0   | 0    | 0    | 0    | 0  | 1           | 0     | 1     |
| Bit    | 7   | 6    | 5    | 4    | 3  | 2           | 1     | 0     |
| Access | CTC | FTSC | AIDC | SEQC |    | MINBPS[2:0] |       |       |
| Reset  | 1   | 1    | 1    | 0    | 0  | 1           | 0     | 1     |

**Bit 10 – TXFCSVC** Transmit Frame Check Sequence Validation Capability

This bit indicates the ability for the MAC to validate the frame check sequence appended by and received from the SPI host. Frames received from the SPI host with an invalid frame check sequence will not be transmitted to the network.

**Note:** Transmit frame sequence validation is supported as indicated by this bit reading as '1'.

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | Transmit frame check sequence validation is not supported |
| 1     | Transmit frame check sequence validation is supported     |

**Bit 9 – IPRAC** Indirect PHY Register access Capability

This bit indicates that the registers of the integrated PHY may be indirectly accessed using the optional OPEN Alliance MDIO Access 0-7 (MDIOACCn) registers.

**Note:** Indirect PHY register access via the optional OPEN Alliance MDIO Access 0-7 (MDIOACCn) is not supported and this bit always reads as '0'. PHY registers, however, may be accessed indirectly through the standard Clause 22 MMD Access Control (11.1.21. MMDCTRL) and MMD Access Address/Data (11.1.22. MMDAD) registers mapped directly into the SPI MMS0 register space.

| Value | Description                                   |
|-------|-----------------------------------------------|
| 0     | Indirect PHY register access is not supported |
| 1     | Indirect PHY register access is supported     |

**Bit 8 – DPRAC** Direct PHY Register Access Capability

This bit indicates that the integrated PHY registers are directly accessible in SPI MMS0 (Clause 22), MMS2 (PCS), MMS3 (PMA/PMD), and MMS4 (PHY vendor specific) as specified by the OPEN Alliance.

**Note:** PHY registers are directly accessible as indicated by this bit reading as '1'.

| Value | Description                                 |
|-------|---------------------------------------------|
| 0     | Direct PHY register access is not supported |
| 1     | Direct PHY register access is supported     |

**Bit 7 – CTC** Cut-through Capability

This bit indicates the support for cut-through transfer of frames through the device to/from the network.

**Note:** Frame cut-through is supported as indicated by this bit reading as '1'.

| Value | Description                                 |
|-------|---------------------------------------------|
| 0     | Cut-through frame transfer is not supported |
| 1     | Cut-through frame transfer is supported     |

**Bit 6 – FTSC** Frame Timestamp Capability

This bit indicates support for the capturing of timestamps on frame network ingress/egress.

**Note:** Frame ingress/egress timestamping is supported as indicated by this bit reading as '1'.

| Value | Description                                                |
|-------|------------------------------------------------------------|
| 0     | Timestamp capture on frame ingress/egress is not supported |
| 1     | Timestamp capture on frame ingress/egress is supported     |

**Bit 5 – AIDC** Address Increment Disable Capability

This bit indicates support for disabling the automatic post-increment of the register address for control command reads and writes. When supported, disabling of the automatic address post-increment is done through the Automatic Increment Disable (AID) bit in the control command header.

**Note:** The register address auto-increment may be disabled as indicated by this bit reading as '1'.

| Value | Description                                                     |
|-------|-----------------------------------------------------------------|
| 0     | Control command address post-increment disable is not supported |
| 1     | Control command address post-increment disable is supported     |

**Bit 4 – SEQC** Transmit Data Block Sequence and Retry Capability

This bit indicates support for monitoring of the transmit data block header Sequence (SEQ) bit as sent by the host MCU.

**Note:** Transmit data block header Sequence bit (SEQ) is not supported as indicated by this bit reading as '0'.

| Value | Description                                                     |
|-------|-----------------------------------------------------------------|
| 0     | Transmit data block header sequence monitoring is not supported |
| 1     | Transmit data block header sequence monitoring is supported     |

**Bits 2:0 – MINBPS[2:0]** Minimum Block Payload Size Capability

This field indicates the minimum supported data block payload size. The minimum supported data payload size is  $2^N$  where N is the value of this bitfield.

**Note:** The minimum supported data payload size is 32 bytes as indicated by this field reading as '101'.

**Note:** This field is referred to as the Minimum Chunk Payload Size Capability (MINCPS) in the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification.

| Value | Description                                     |
|-------|-------------------------------------------------|
| 011   | Minimum supported data payload size is 8 bytes  |
| 100   | Minimum supported data payload size is 16 bytes |
| 101   | Minimum supported data payload size is 32 bytes |
| 110   | Minimum supported data payload size is 64 bytes |

**11.1.4 Reset Control and Status Register****Name:** OA\_RESET**Address:** 0x03

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |             |
|--------|----|----|----|----|----|----|----|-------------|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0           |
|        |    |    |    |    |    |    |    |             |
| Access | RO | RO | RO | RO | RO | RO | RO | SWRESET     |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | R/W SC<br>0 |

**Bit 0 – SWRESET** Software Reset

Writing a '1' to this bit will fully reset the device including the integrated PHY. When set, the reset will not occur until the CS\_N pin has been deasserted high following the SPI transaction performing the write.

**Note:** This bit is self clearing upon reset of the device.

| Value | Description             |
|-------|-------------------------|
| 0     | Normal operation        |
| 1     | Device performs a reset |

### 11.1.5 Configuration 0 Register

**Name:** OA\_CONFIG0**Address:** 0x004

|        |       |         |          |      |                |          |       |       |
|--------|-------|---------|----------|------|----------------|----------|-------|-------|
| Bit    | 31    | 30      | 29       | 28   | 27             | 26       | 25    | 24    |
| Access | RO    | RO      | RO       | RO   | RO             | RO       | RO    | RO    |
| Reset  | 0     | 0       | 0        | 0    | 0              | 0        | 0     | 0     |
| Bit    | 23    | 22      | 21       | 20   | 19             | 18       | 17    | 16    |
| Access | RO    | RO      | RO       | RO   | RO             | RO       | RO    | RO    |
| Reset  | 0     | 0       | 0        | 0    | 0              | 0        | 0     | 0     |
| Bit    | 15    | 14      | 13       | 12   | 11             | 10       | 9     | 8     |
|        | SYNC  | TXFCSVE | RFA[1:0] |      | TXCTHRESH[1:0] |          | TXCTE | RXCTE |
| Access | R/W1S | R/W     | R/W      | R/W  | R/W            | R/W      | R/W   | R/W   |
| Reset  | 0     | 0       | 0        | 0    | 0              | 0        | 0     | 0     |
| Bit    | 7     | 6       | 5        | 4    | 3              | 2        | 1     | 0     |
|        | FTSE  | FTSS    | PROTE    | SEQE |                | BPS[2:0] |       |       |
| Access | R/W   | R/W     | R/W      | RO   | RO             | R/W      | R/W   | R/W   |
| Reset  | 0     | 0       | 0        | 0    | 0              | 1        | 1     | 0     |

#### Bit 15 – SYNC Configuration Synchronization

Once the device has been configured and is ready for Ethernet frames to be transferred between the network and SPI, the host MCU sets this bit to a '1'. This bit is reflected in the data footer SYNC bit.

**Note:** Once set, this bit may only be cleared by a reset of the device.

| Value | Description                                                                     |
|-------|---------------------------------------------------------------------------------|
| 0     | Device has not been configured and transfer of Ethernet frames is not permitted |
| 1     | Device has been configured and transfer of Ethernet frames may occur            |

#### Bit 14 – TXFCSVE Transmit Frame Check Sequence Validation Enable

When this bit is set, the MAC will interpret the final four bytes of frames received from the SPI host as an Ethernet frame check sequence. The MAC will validate the received frame to verify correct reception via SPI. Should an error be detected in the frame received from the host over SPI, the device will drop the frame and not transmit it onto the network.

**Note:** When enabling this feature, the SPI host must pad the frame to the minimum size and append the calculated 32-bit frame check sequence.

| Value | Description                                                                                                                                                                                                                                                              |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Transmit frame check sequence validation is not performed. The internal MAC will pad frames received from the host to the minimum packet size and append the correct frame check sequence prior to transmitting the packet onto the network.                             |
| 1     | Transmit frame check sequence validation is performed. The SPI host must pad all frames to the minimum packet size and append the correct frame check sequence. The internal MAC will validate the frame received from the host before transmitting it onto the network. |

#### Bits 13:12 – RFA[1:0] Receive Frame Alignment

This field configures the alignment of receive frames within the receive data blocks. When this field is '00', receive Ethernet frames may begin at any word of any receive SPI data block payload.

When this field is '01', the start of all receive Ethernet frames will be output to the SPI aligned to the beginning of *any* receive data block payload with a Start Word Offset (SWO) of zero. When this field is configured to '10', the start of all receive Ethernet frames will be output to the SPI beginning with the first receive data block payload following CS\_N assertion. The Start Word Offset (SWO) will always be zero. Only one frame may be received per assertion of CS\_N.

**Note:** Writing this field to '11' is invalid and will result in undefined operation.

| Value | Description                                                                                                                                                          |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00    | Receive Ethernet frames may begin at any word of any receive data block. (Default)                                                                                   |
| 01    | Zero-Align Receive Frame Enable (ZARFE)<br>Receive Ethernet frames will begin only at the first word of the receive data payload in any data block.                  |
| 10    | CS_N Align Receive Frame Enable (CSARFE)<br>Receive Ethernet frames only begin in the first word of the first receive data block payload following assertion of CS_N |
| 11    | Invalid                                                                                                                                                              |

#### Bits 11:10 – TXCTHRESH[1:0] Transmit Credit Threshold

This field configures the minimum number of transmit credits (TXC) of free buffers that must be available within the device before IRQ\_N will be asserted. This guarantees a minimum number of Ethernet frame data blocks the SPI host may send to the device in a burst.

| Value | Description                                                                              |
|-------|------------------------------------------------------------------------------------------|
| 00    | IRQ_N will be asserted when enough buffer space is available for at least 1 data block   |
| 01    | IRQ_N will be asserted when enough buffer space is available for at least 4 data blocks  |
| 10    | IRQ_N will be asserted when enough buffer space is available for at least 8 data blocks  |
| 11    | IRQ_N will be asserted when enough buffer space is available for at least 16 data blocks |

#### Bit 9 – TXCTE Transmit Cut-Through Enable

When set, this bit will enable the cut-through mode of egress frame transfer from the SPI to the network.

| Value | Description                            |
|-------|----------------------------------------|
| 0     | Transmit frame cut-through is disabled |
| 1     | Transmit frame cut-through is enabled  |

#### Bit 8 – RXCTE Receive Cut-Through Enable

When set, this bit will enable the cut-through mode of ingress frame transfer from the network to the SPI.

| Value | Description                           |
|-------|---------------------------------------|
| 0     | Receive frame cut-through is disabled |
| 1     | Receive frame cut-through is enabled  |

#### Bit 7 – FTSE Frame Timestamp Enable

When set, this bit enables the capturing of frame ingress/egress timestamps.

| Value | Description                                   |
|-------|-----------------------------------------------|
| 0     | Frame ingress/egress timestamping is disabled |
| 1     | Frame ingress/egress timestamping is enabled  |

#### Bit 6 – FTSS Frame Timestamp Select

When frame timestamping is enabled (see [FTSE](#)), this bit selects the size and format of the timestamps added to the beginning of ingress frames and captured on request of egress frames.

| Value | Description       |
|-------|-------------------|
| 0     | 32-bit timestamps |
| 1     | 64-bit timestamps |

#### Bit 5 – PROTE Control Data Read/Write Protection Enable

When set, this bit will enable the protection of control command register data against bit errors during transfer over the SPI.

**Note:** Control data read/write protection is disabled by default. Therefore, to enable control data read/write protection, this field must be initially written without write protection.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | Control data read/write protection is disabled |
| 1     | Control data read/write protection is enabled  |

#### Bit 4 – SEQE Transmit data block header Sequence bit support Enable

If supported, setting this bit would enable the MAC-PHY monitoring of the Sequence (SEQ) bit sent by the SPI host in the transmit data block header.

**Note:** This feature is not supported. This bit is read-only and cannot be set.

| Value | Description                                                                    |
|-------|--------------------------------------------------------------------------------|
| 0     | Transmit data block header Sequence bit monitoring is disabled.                |
| 1     | Transmit data block header Sequence bit monitoring is enabled. (Not supported) |

#### Bits 2:0 – BPS[2:0] Block Payload Size

This field configures the receive and transmit data block payload size. The data payload size is configured to  $2^N$  where N is the value of this bitfield.



**Important:** This field shall be changed prior to setting the Configuration Synchronization (SYNC) bit in this register enabling Ethernet packet transfer.



**Important:** When changing this field, the Buffer Size (BUFSZ) field in the Queue Transmit Configuration (QTXCFG) and Queue Receive Configuration (QRXCFG) must also be changed.

**Note:** This field is referred to as the *Chunk* Payload Size Capability (CPS) in the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification.

| Value  | Description                               |
|--------|-------------------------------------------|
| 101    | 32 byte data block payload size           |
| 110    | 64 byte data block payload size (default) |
| others | Reserved                                  |

**11.1.6 Status 0 Register****Name:** OA\_STATUS0**Address:** 0x008

|        |        |        |      |       |        |        |        |        |
|--------|--------|--------|------|-------|--------|--------|--------|--------|
| Bit    | 31     | 30     | 29   | 28    | 27     | 26     | 25     | 24     |
| Access | RO     | RO     | RO   | RO    | RO     | RO     | RO     | RO     |
| Reset  | 0      | 0      | 0    | 0     | 0      | 0      | 0      | 0      |
| Bit    | 23     | 22     | 21   | 20    | 19     | 18     | 17     | 16     |
| Access | RO     | RO     | RO   | RO    | RO     | RO     | RO     | RO     |
| Reset  | 0      | 0      | 0    | 0     | 0      | 0      | 0      | 0      |
| Bit    | 15     | 14     | 13   | 12    | 11     | 10     | 9      | 8      |
| Access | RO     | RO     | RO   | CPDE  | TXFCSE | TTSCAC | TTSCAB | TTSCAA |
| Reset  | 0      | 0      | 0    | R/W1C | R/W1C  | R/W1C  | R/W1C  | R/W1C  |
| Bit    | 7      | 6      | 5    | 4     | 3      | 2      | 1      | 0      |
| Access | PHYINT | RESETC | HDRE | LOFE  | RXBOE  | TXBUE  | TXBOE  | TXPE   |
| Reset  | 0      | 0      | 0    | 0     | 0      | 0      | 0      | 0      |

**Bit 12 – CPDE** Control Data Protection Error

When control register data protection is enabled (see [PROTE](#)), this bit is set when a bit error has been detected in a control command received from the SPI host.

| Value | Description                                        |
|-------|----------------------------------------------------|
| 0     | A control command data error has not been detected |
| 1     | A control command data error has been detected     |

**Bit 11 – TXFCSE** Transmit Frame Check Sequence Error

When transmit frame check sequence validation is enabled (see [TXFCSVE](#)), this bit will be set when the MAC-PHY receives an Ethernet frame from the SPI host with an invalid frame check sequence.

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | Transmit frame check sequence error has not been detected |
| 1     | Transmit frame check sequence error has been detected     |

**Bit 10 – TTSCAC** Transmit Timestamp Capture Available C

This bit is set when a frame has been transmitted to the network and a timestamp has been captured in the Transmit Timestamp Capture C (TTSCC) register and is ready for reading.

| Value | Description                                                                            |
|-------|----------------------------------------------------------------------------------------|
| 0     | Timestamp has not been captured into the Transmit Timestamp Capture C (TTSCC) register |
| 1     | Timestamp has been captured into the Transmit Timestamp Capture C (TTSCC) register     |

**Bit 9 – TTSCAB** Transmit Timestamp Capture Available B

This bit is set when a frame has been transmitted to the network and a timestamp has been captured in the Transmit Timestamp Capture B (TTSCB) register and is ready for reading.

| Value | Description                                                                            |
|-------|----------------------------------------------------------------------------------------|
| 0     | Timestamp has not been captured into the Transmit Timestamp Capture B (TTSCB) register |
| 1     | Timestamp has been captured into the Transmit Timestamp Capture B (TTSCB) register     |

**Bit 8 – TTSCAA** Transmit Timestamp Capture Available A

This bit is set when a frame has been transmitted to the network and a timestamp has been captured in the Transmit Timestamp Capture A (TTSCA) register and is ready for reading.

| Value | Description                                                                            |
|-------|----------------------------------------------------------------------------------------|
| 0     | Timestamp has not been captured into the Transmit Timestamp Capture A (TTSCA) register |
| 1     | Timestamp has been captured into the Transmit Timestamp Capture A (TTSCA) register     |

**Bit 7 – PHYINT** PHY Interrupt

This bit is set when the integrated PHY has signaled an interrupt service request. The host must read the PHY status registers to determine the source of the PHY interrupt.

**Note:** This bit is cleared by clearing the underlying PHY interrupt source(s).

| Value | Description                         |
|-------|-------------------------------------|
| 0     | PHY interrupt has not been detected |
| 1     | PHY interrupt has been detected     |

**Bit 6 – RESETC** Reset Complete

This bit is set upon a reset of the device.

| Value | Description                                      |
|-------|--------------------------------------------------|
| 0     | Device has not been reset (normal operation)     |
| 1     | Device has been reset and requires configuration |

**Bit 5 – HDRE** Header Error Status

This bit is set when a header was received which failed the parity check.

| Value | Description               |
|-------|---------------------------|
| 0     | No header error detected  |
| 1     | Header error has occurred |

**Bit 4 – LOFE** Loss of Framing Error Status

This bit is set when an early deassertion of CS\_N has been detected and the MAC-PHY has lost transaction framing with the host.

| Value | Description                                 |
|-------|---------------------------------------------|
| 0     | Loss of framing error has not been detected |
| 1     | Loss of framing error has been detected     |

**Bit 3 – RXBOE** Receive Buffer Overflow Error Status

This bit is set when received data from the network has overflowed the internal receive buffer and Ethernet frame data has been lost.

| Value | Description                                             |
|-------|---------------------------------------------------------|
| 0     | Receive buffer overflow condition has not been detected |
| 1     | Receive buffer overflow condition has been detected     |

**Bit 2 – TXBUE** Transmit Buffer Underflow Error Status

This bit is set when transmit data from the SPI host has under-flowed the internal transmit buffer while the MAC was transmitting the Ethernet frame data to the network in transmit cut-through operation.

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | Transmit buffer underflow condition has not been detected |
| 1     | Transmit buffer underflow condition has been detected     |

**Bit 1 – TXBOE** Transmit Buffer Overflow Error Status

This bit is set when transmit Ethernet frame data from the SPI host has over-flowed the internal transmit buffers.

| Value | Description                                              |
|-------|----------------------------------------------------------|
| 0     | Transmit buffer overflow condition has not been detected |
| 1     | Transmit buffer overflow condition has been detected     |



**Bit 0 – TXPE** Transmit Protocol Error Status

This bit is set when a transmit data protocol error has been detected.

| Value | Description                                   |
|-------|-----------------------------------------------|
| 0     | Transmit protocol error has not been detected |
| 1     | Transmit protocol error has been detected     |

### 11.1.7 Status 1 Register

**Name:** OA\_STATUS1

**Address:** 0x009

This register contains vendor specific status.

|        |    |    |    |     |    |        |        |        |
|--------|----|----|----|-----|----|--------|--------|--------|
| Bit    | 31 | 30 | 29 | 28  | 27 | 26     | 25     | 24     |
|        |    |    |    | SEV |    | TTSCMC | TTSCMB | TTSCMA |
| Access | RO | RO | RO | RO  | RO | R/W1C  | R/W1C  | R/W1C  |
| Reset  | 0  | 0  | 0  | 0   | 0  | 0      | 0      | 0      |

|        |         |         |         |       |       |       |         |    |
|--------|---------|---------|---------|-------|-------|-------|---------|----|
| Bit    | 23      | 22      | 21      | 20    | 19    | 18    | 17      | 16 |
|        | TTSCOFC | TTSCOFB | TTSCOFA | BUSER | UV18  | ECC   | FSMSTER |    |
| Access | R/W1C   | R/W1C   | R/W1C   | R/W1C | R/W1C | R/W1C | R/W1C   | RO |
| Reset  | 0       | 0       | 0       | 0     | 0     | 0     | 0       | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |       |       |
|--------|----|----|----|----|----|----|-------|-------|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1     | 0     |
|        |    |    |    |    |    |    | TXNER | RXNER |
| Access | RO | RO | RO | RO | RO | RO | R/W1C | R/W1C |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0     | 0     |

#### Bit 28 – SEV Synchronization Event

This bit is set when any of the bits within the Synchronization Event Status (SEVSTS) register are set and the associated bit is not disabled in the Synchronization Event Interrupt Mask (SEVIM) register.

**Note:** This bit is cleared by reading the Synchronization Event Status Register (SEVSTS).

| Value | Description                                            |
|-------|--------------------------------------------------------|
| 0     | At least one enabled bit is set in the SEVSTS register |
| 1     | No enabled bits are set in the SEVSTS register         |

#### Bit 26 – TTSCMC Transmit Timestamp Capture Missed C

This bit is set when a requested timestamp was requested for a transmit frame into Transmit Timestamp Capture C (TTSCC), however, the transmit event was missed. This may be due to failing the transmit packet pattern match, if enabled.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | No error.                                      |
| 1     | Requested frame timestamp capture C was missed |

#### Bit 25 – TTSCMB Transmit Timestamp Capture Missed B

This bit is set when a requested timestamp was requested for a transmit frame into Transmit Timestamp Capture B (TTSCB), however, the transmit event was missed. This may be due to failing the transmit packet pattern match, if enabled.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | No error.                                      |
| 1     | Requested frame timestamp capture B was missed |

**Bit 24 – TTSCMA** Transmit Timestamp Capture Missed A

This bit is set when a requested timestamp was requested for a transmit frame into Transmit Timestamp Capture A (TTSCA), however, the transmit event was missed. This may be due to failing the transmit packet pattern match, if enabled.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | No error.                                      |
| 1     | Requested frame timestamp capture A was missed |

**Bit 23 – TTSCOF C** Transmit Timestamp Capture Overflow C

This bit is set when a requested timestamp was requested for a transmit frame into Transmit Timestamp Capture C (TTSCC), however, the previous captured timestamp stored in TTSCC has not been read yet. The timestamp stored in TTSCC is not overwritten, and the new transmit packet timestamp will not be captured.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | No error.                                      |
| 1     | Requested frame timestamp capture C overflowed |

**Bit 22 – TTSCOFB** Transmit Timestamp Capture Overflow B

This bit is set when a requested timestamp was requested for a transmit frame into Transmit Timestamp Capture B (TTSCB), however, the previous captured timestamp stored in TTSCB has not been read yet. The timestamp stored in TTSCB is not overwritten, and the new transmit packet timestamp will not be captured.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | No error.                                      |
| 1     | Requested frame timestamp capture B overflowed |

**Bit 21 – TTSCOFA** Transmit Timestamp Capture Overflow A

This bit is set when a requested timestamp was requested for a transmit frame into Transmit Timestamp Capture A (TTSCA), however, the previous captured timestamp stored in TTSCA has not been read yet. The timestamp stored in TTSCA is not overwritten, and the new transmit packet timestamp will not be captured.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | No error.                                      |
| 1     | Requested frame timestamp capture A overflowed |

**Bit 20 – BUSER** Internal Bus Error

This bit is set when an internal bus error has been detected. This may occur due to a bus parity error or uncorrectable SRAM error. When this error occurs, the host controller must perform a hardware or software reset of the device.

| Value | Description                    |
|-------|--------------------------------|
| 0     | No internal bus error detected |
| 1     | Internal bus error detected    |

**Bit 19 – UV18** 1.8V supply Under-Voltage Status

Set when an under-voltage condition has been detected on the 1.8V supply.

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | 1.8V supply under-voltage condition has not been detected |
| 1     | 1.8V supply under-voltage condition has occurred          |

**Bit 18 – ECC** SRAM ECC Error Status

Set when an SRAM ECC error has been detected.

| Value | Description                    |
|-------|--------------------------------|
| 0     | No SRAM ECC error detected     |
| 1     | An SRAM ECC error has occurred |

**Bit 17 – FSMSTER** FSM State Error Status

This bit is set when an internal state machine error has been detected. This may occur due to a random failure that causes a state machine to transition into an unexpected or invalid state. When this error occurs, the host controller must perform a hardware or software reset of the device.

| Value | Description                               |
|-------|-------------------------------------------|
| 0     | No internal state machine errors detected |
| 1     | Internal state machine error has occurred |

**Bit 1 – TXNER** Transmit Non-Recoverable Error Status

This bit is set when an internal non-recoverable transmit error has been detected. When this error occurs, the host controller must perform a hardware or software reset of the device.

| Value | Description                                 |
|-------|---------------------------------------------|
| 0     | No transmit non-recoverable errors          |
| 1     | Transmit non-recoverable error has occurred |

**Bit 0 – RXNER** Receive Non-Recoverable Error Status

This bit is set when an internal non-recoverable receive error has been detected. When this error occurs, the host controller must perform a hardware or software reset of the device.

| Value | Description                                |
|-------|--------------------------------------------|
| 0     | No receive non-recoverable errors          |
| 1     | Receive non-recoverable error has occurred |

### 11.1.8 Buffer Status Register

**Name:** OA\_BUFSTS

**Address:** 0x000B

Internal SPI<->MAC Transmit and Receive Buffer Status

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |          |    |    |    |    |    |    |    |
|--------|----------|----|----|----|----|----|----|----|
| Bit    | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TXC[7:0] |    |    |    |    |    |    |    |
| Access | RO       | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0        | 0  | 1  | 1  | 0  | 0  | 0  | 0  |

|        |          |    |    |    |    |    |    |    |
|--------|----------|----|----|----|----|----|----|----|
| Bit    | 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | RBA[7:0] |    |    |    |    |    |    |    |
| Access | RO       | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

#### Bits 15:8 – TXC[7:0] Transmit Credits Available

This field contains the number of Ethernet frame segments that the host MCU can write in a single burst without causing a Transmit Buffer Overflow Error.

**Note:** This field is saturated to five bits (0x1F) and sent over SPI to the host MCU within the TXC field of every receive data footer.

| Value | Description                                                                                       |
|-------|---------------------------------------------------------------------------------------------------|
| ≥0x31 | Not supported                                                                                     |
| 0x30  | The host MCU may write up to 48 segments of Ethernet frame data without overflow.                 |
| 0x2F  | The host MCU may write up to 47 segments of Ethernet frame data without overflow.                 |
| ...   | ...                                                                                               |
| 0x01  | The host MCU may write 1 segments of Ethernet frame data without overflow.                        |
| 0x00  | The host MCU cannot write any segments of Ethernet frame data without causing an overflow error . |

#### Bits 7:0 – RBA[7:0] Receive Blocks Available

This field contains the number of receive data blocks (segments) of Ethernet frame data that is available to the host MCU for reading. If the MCU host reads more data blocks than is available, either empty data blocks with the footer Data Valid flag set to zero or additional frame data may be sent to the host if the MAC-PHY has received data from the network since the beginning of the frame data transaction burst.

**Note:** This field is saturated to five bits (0x1F) and sent over SPI to the host within the RBA field of every receive data footer.

| Value | Description                                                          |
|-------|----------------------------------------------------------------------|
| ≥0x31 | Not supported                                                        |
| 0x30  | At least 48 blocks of Ethernet frame data are available for reading. |
| 0x2F  | 47 blocks of Ethernet frame data are available for reading.          |
| ...   | ...                                                                  |
| 0x01  | One block of Ethernet frame data is available for reading.           |

| Value | Description                                            |
|-------|--------------------------------------------------------|
| 0x00  | There is no Ethernet frame data available for reading. |

**11.1.9 Interrupt Mask 0 Register****Name:** OA\_IMASK0**Address:** 0x00C

|        |         |         |       |       |         |         |         |         |
|--------|---------|---------|-------|-------|---------|---------|---------|---------|
| Bit    | 31      | 30      | 29    | 28    | 27      | 26      | 25      | 24      |
| Access | RO      | RO      | RO    | RO    | RO      | RO      | RO      | RO      |
| Reset  | 0       | 0       | 0     | 0     | 0       | 0       | 0       | 0       |
| Bit    | 23      | 22      | 21    | 20    | 19      | 18      | 17      | 16      |
| Access | RO      | RO      | RO    | RO    | RO      | RO      | RO      | RO      |
| Reset  | 0       | 0       | 0     | 0     | 0       | 0       | 0       | 0       |
| Bit    | 15      | 14      | 13    | 12    | 11      | 10      | 9       | 8       |
| Access | RO      | RO      | RO    | CPDEM | TXFCSEM | TTSCACM | TTSCABM | TTSCAAM |
| Reset  | 0       | 0       | 1     | 1     | 1       | 1       | 1       | 1       |
| Bit    | 7       | 6       | 5     | 4     | 3       | 2       | 1       | 0       |
| Access | PHYINTM | RESETCM | HDREM | LOFEM | RXBOEM  | TXBUEM  | TXBOEM  | TXPEM   |
| Reset  | 1       | 0       | 1     | 1     | 1       | 1       | 1       | 1       |

**Bit 12 – CPDEM** Control Data Protection Error Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Control Data Protection Error (CPDE) status bit is set in the Status 0 register.

| Value | Description                                             |
|-------|---------------------------------------------------------|
| 0     | Control data protection error status interrupt enabled  |
| 1     | Control data protection error status interrupt disabled |

**Bit 11 – TXFCSEM** Transmit Frame Check Sequence Error Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Frame Check Sequence Error (TXFCSE) status bit is set in the Status 0 register.

| Value | Description                                                   |
|-------|---------------------------------------------------------------|
| 0     | Transmit frame check sequence error status interrupt enabled  |
| 1     | Transmit frame check sequence error status interrupt disabled |

**Bit 10 – TTSCACM** Transmit Timestamp Capture Available C Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Timestamp Capture Available C (TTSCAC) status bit is set in the Status 0 register.

| Value | Description                                                      |
|-------|------------------------------------------------------------------|
| 0     | Transmit timestamp capture available C status interrupt enabled  |
| 1     | Transmit timestamp capture available C status interrupt disabled |

**Bit 9 – TTSCABM** Transmit Timestamp Capture Available B Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Timestamp Capture Available B (TTSCAB) status bit is set in the Status 0 register.

| Value | Description                                                      |
|-------|------------------------------------------------------------------|
| 0     | Transmit timestamp capture available B status interrupt enabled  |
| 1     | Transmit timestamp capture available B status interrupt disabled |

**Bit 8 – TTSCAAM** Transmit Timestamp Capture Available A Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Timestamp Capture Available A (TTSCAA) status bit is set in the Status 0 register.

| Value | Description                                                      |
|-------|------------------------------------------------------------------|
| 0     | Transmit timestamp capture available A status interrupt enabled  |
| 1     | Transmit timestamp capture available A status interrupt disabled |

**Bit 7 – PHYINTM** PHY Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the PHY Interrupt (PHYINT) status bit is set in the Status 0 register.

| Value | Description                   |
|-------|-------------------------------|
| 0     | PHY status interrupt enabled  |
| 1     | PHY status interrupt disabled |

**Bit 6 – RESETCM** Reset Complete Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Reset Complete (RESETC) status bit is set in the Status 0 register.

**Note:** The Reset Complete interrupt cannot be disabled. A Reset will always cause the IRQ\_N pin to be asserted upon setting of the Reset Complete (RESETC) status bit in the Status 0 register.

| Value | Description                             |
|-------|-----------------------------------------|
| 0     | Reset complete status interrupt enabled |
| 1     | Invalid state (cannot be written)       |

**Bit 5 – HDREM** Header Error Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Header Error (HDRE) status bit is set in the Status 0 register.

| Value | Description                            |
|-------|----------------------------------------|
| 0     | Header error status interrupt enabled  |
| 1     | Header error status interrupt disabled |

**Bit 4 – LOFEM** Loss of Framing Error Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Loss of Framing Error (LOFE) status bit is set in the Status 0 register.

| Value | Description                                     |
|-------|-------------------------------------------------|
| 0     | Loss of framing error status interrupt enabled  |
| 1     | Loss of framing error status interrupt disabled |

**Bit 3 – RXBOEM** Receive Buffer Overflow Error Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Receive Buffer Overflow Error (RXBOE) status bit is set in the Status 0 register.

| Value | Description                                       |
|-------|---------------------------------------------------|
| 0     | Receive buffer overflow status interrupt enabled  |
| 1     | Receive buffer overflow status interrupt disabled |

**Bit 2 – TXBUEM** Transmit Buffer Underflow Error Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Buffer Underflow Error (TXBUE) status bit is set in the Status 0 register.

| Value | Description                                         |
|-------|-----------------------------------------------------|
| 0     | Transmit buffer underflow status interrupt enabled  |
| 1     | Transmit buffer underflow status interrupt disabled |

**Bit 1 – TXBOEM** Transmit Buffer Overflow Error Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Buffer Overflow Error (TXBOE) status bit is set in the Status 0 register.

| Value | Description                                       |
|-------|---------------------------------------------------|
| 0     | Transmit buffer overflow status interrupt enabled |



| Value | Description                                        |
|-------|----------------------------------------------------|
| 1     | Transmit buffer overflow status interrupt disabled |

**Bit 0 – TXPEM** Transmit Protocol Error Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Protocol Error (TXPE) status bit is set in the Status 0 register.

| Value | Description                                       |
|-------|---------------------------------------------------|
| 0     | Transmit protocol error status interrupt enabled  |
| 1     | Transmit protocol error status interrupt disabled |

**11.1.10 Interrupt Mask 1 Register****Name:** OA\_IMASK1**Address:** 0x00D

This register contains vendor specific status interrupt masks.

|        |    |    |     |      |     |         |         |         |
|--------|----|----|-----|------|-----|---------|---------|---------|
| Bit    | 31 | 30 | 29  | 28   | 27  | 26      | 25      | 24      |
|        |    |    |     | SEVM |     | TTSCMCM | TTSCMBM | TTSCMAM |
| Access | RO | RO | R/W | R/W  | R/W | R/W     | R/W     | R/W     |
| Reset  | 0  | 0  | 1   | 1    | 1   | 1       | 1       | 1       |

|        |          |          |          |        |       |      |          |    |
|--------|----------|----------|----------|--------|-------|------|----------|----|
| Bit    | 23       | 22       | 21       | 20     | 19    | 18   | 17       | 16 |
|        | TTSCOFAM | TTSCOFBM | TTSCOFAM | BUSERM | UV18M | ECCM | FSMSTERM |    |
| Access | R/W      | R/W      | R/W      | R/W    | R/W   | R/W  | R/W      | RO |
| Reset  | 1        | 1        | 1        | 1      | 1     | 1    | 1        | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |        |        |
|--------|----|----|----|----|----|----|--------|--------|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1      | 0      |
|        |    |    |    |    |    |    | TXNERM | RXNERM |
| Access | RO | RO | RO | RO | RO | RO | R/W    | R/W    |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 1      | 1      |

**Bit 28 – SEVM** Synchronization Event Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Synchronization Event status bit is set in the Status 1 register.

| Value | Description                              |
|-------|------------------------------------------|
| 0     | Synchronization event interrupt enabled  |
| 1     | Synchronization event interrupt disabled |

**Bit 26 – TTSCMCM** Transmit Timestamp Capture Missed C Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Timestamp Capture Missed C (TTSCMC) status bit is set in the Status 1 register.

| Value | Description                                            |
|-------|--------------------------------------------------------|
| 0     | Transmit Timestamp Capture Missed C interrupt enabled  |
| 1     | Transmit Timestamp Capture Missed C interrupt disabled |

**Bit 25 – TTSCMBM** Transmit Timestamp Capture Missed B Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Timestamp Capture Missed B (TTSCMB) status bit is set in the Status 1 register.

| Value | Description                                            |
|-------|--------------------------------------------------------|
| 0     | Transmit Timestamp Capture Missed B interrupt enabled  |
| 1     | Transmit Timestamp Capture Missed B interrupt disabled |

**Bit 24 – TTSCMAM** Transmit Timestamp Capture Missed A Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Timestamp Capture Missed A (TTSCMA) status bit is set in the Status 1 register.

| Value | Description                                            |
|-------|--------------------------------------------------------|
| 0     | Transmit Timestamp Capture Missed A interrupt enabled  |
| 1     | Transmit Timestamp Capture Missed A interrupt disabled |

**Bit 23 – TTSCOFM** Transmit Timestamp Capture Overflow C Interrupt Mask  
When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Timestamp Capture Overflow C (TTSCMC) status bit is set in the Status 1 register.

| Value | Description                                              |
|-------|----------------------------------------------------------|
| 0     | Transmit Timestamp Capture Overflow C interrupt enabled  |
| 1     | Transmit Timestamp Capture Overflow C interrupt disabled |

**Bit 22 – TTSCOFB** Transmit Timestamp Capture Overflow B Interrupt Mask  
When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Timestamp Capture Overflow B (TTSCMB) status bit is set in the Status 1 register.

| Value | Description                                              |
|-------|----------------------------------------------------------|
| 0     | Transmit Timestamp Capture Overflow B interrupt enabled  |
| 1     | Transmit Timestamp Capture Overflow B interrupt disabled |

**Bit 21 – TTSCOFAM** Transmit Timestamp Capture Overflow A Interrupt Mask  
When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Timestamp Capture Overflow A (TTSCMA) status bit is set in the Status 1 register.

| Value | Description                                              |
|-------|----------------------------------------------------------|
| 0     | Transmit Timestamp Capture Overflow A interrupt enabled  |
| 1     | Transmit Timestamp Capture Overflow A interrupt disabled |

**Bit 20 – BUSERM** Internal Bus Error Interrupt Mask  
When clear, this bit will enable the assertion of the IRQ\_N pin when the internal Bus Error (BUSER) status bit is set in the Status 1 register.

| Value | Description                           |
|-------|---------------------------------------|
| 0     | Internal bus error interrupt enabled  |
| 1     | Internal bus error interrupt disabled |

**Bit 19 – UV18M** 1.8V supply Under-Voltage Interrupt Mask  
When clear, this bit will enable the assertion of the IRQ\_N pin when the 1.8V supply Under-voltage (UV18) status bit is set in the Status 1 register.

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | 1.8V supply under-voltage interrupt enabled  |
| 1     | 1.8V supply under-voltage interrupt disabled |

**Bit 18 – ECCM** SRAM ECC Error Interrupt Mask  
When clear, this bit will enable the assertion of the IRQ\_N pin when the SRAM ECC Error (ECC) status bit is set in the Status 1 register.

| Value | Description                       |
|-------|-----------------------------------|
| 0     | SRAM ECC error interrupt enabled  |
| 1     | SRAM ECC error interrupt disabled |

**Bit 17 – FSMSTERM** FSM State Error Interrupt Mask  
When clear, this bit will enable the assertion of the IRQ\_N pin when the FSM State Error (FSMSTER) status bit is set in the Status 1 register.

| Value | Description                        |
|-------|------------------------------------|
| 0     | FSM state error interrupt enabled  |
| 1     | FSM state error interrupt disabled |

**Bit 1 – TXNERM** Transmit Non-Recoverable Error Interrupt Mask  
When clear, this bit will enable the assertion of the IRQ\_N pin when the Transmit Non-Recoverable Error (TXNER) status bit is set in the Status 1 register.

| Value | Description                                       |
|-------|---------------------------------------------------|
| 0     | Transmit non-recoverable error interrupt enabled  |
| 1     | Transmit non-recoverable error interrupt disabled |

**Bit 0 – RXNERM** Receive Non-Recoverable Error Interrupt Mask

When clear, this bit will enable the assertion of the IRQ\_N pin when the Receive Non-Recoverable Error (RXNER) status bit is set in the Status 1 register.

| Value | Description                                      |
|-------|--------------------------------------------------|
| 0     | Receive non-recoverable error interrupt enabled  |
| 1     | Receive non-recoverable error interrupt disabled |

**11.1.11 Transmit Timestamp Capture A (High)****Name:** TTSCAH**Address:** 0x0010

|        |                    |    |    |    |    |    |    |    |
|--------|--------------------|----|----|----|----|----|----|----|
| Bit    | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TIMESTAMP_A[63:56] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TIMESTAMP_A[55:48] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TIMESTAMP_A[47:40] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TIMESTAMP_A[39:32] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – TIMESTAMP\_A[63:32] Captured Egress Timestamp**

This field contains the 32 most significant bits of the 64-bit captured egress frame timestamp. The format of the timestamp is determined by the state of the Frame Timestamp Select (**FTSS**) bit in the OPEN Alliance Configuration 0 (**11.1.5. OA\_CONFIG0**) register.

**11.1.12 Transmit Timestamp Capture A (Low)****Name:** TTSCAL**Address:** 0x0011

|        |                    |    |    |    |    |    |    |    |
|--------|--------------------|----|----|----|----|----|----|----|
| Bit    | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TIMESTAMP_A[31:24] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TIMESTAMP_A[23:16] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TIMESTAMP_A[15:8]  |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TIMESTAMP_A[7:0]   |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – TIMESTAMP\_A[31:0] Captured Egress Timestamp A**

This field contains the 32 least significant bits of the 64-bit captured egress frame timestamp. The format of the timestamp is determined by the state of the Frame Timestamp Select ([FTSS](#)) bit in the OPEN Alliance Configuration 0 ([11.1.5. OA\\_CONFIG0](#)) register.

**11.1.13 Transmit Timestamp Capture B (High)****Name:** TTSCBH**Address:** 0x0012

|        |                   |    |    |    |    |    |    |    |
|--------|-------------------|----|----|----|----|----|----|----|
| Bit    | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TIMESTAMPB[63:56] |    |    |    |    |    |    |    |
| Access | RO                | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TIMESTAMPB[55:48] |    |    |    |    |    |    |    |
| Access | RO                | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TIMESTAMPB[47:40] |    |    |    |    |    |    |    |
| Access | RO                | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TIMESTAMPB[39:32] |    |    |    |    |    |    |    |
| Access | RO                | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – TIMESTAMPB[63:32] Captured Egress Timestamp B**

This field contains the 32 most significant bits of the 64-bit captured egress frame timestamp. The format of the timestamp is determined by the state of the Frame Timestamp Select ([FTSS](#)) bit in the OPEN Alliance Configuration 0 ([11.1.5. OA\\_CONFIG0](#)) register.

**11.1.14 Transmit Timestamp Capture B (Low)****Name:** TTSCBL**Address:** 0x0013

|        |                   |    |    |    |    |    |    |    |
|--------|-------------------|----|----|----|----|----|----|----|
| Bit    | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TIMESTAMPB[31:24] |    |    |    |    |    |    |    |
| Access | RO                | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TIMESTAMPB[23:16] |    |    |    |    |    |    |    |
| Access | RO                | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TIMESTAMPB[15:8]  |    |    |    |    |    |    |    |
| Access | RO                | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TIMESTAMPB[7:0]   |    |    |    |    |    |    |    |
| Access | RO                | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – TIMESTAMPB[31:0] Captured Egress Timestamp B**

This field contains the 32 least significant bits of the 64-bit captured egress frame timestamp. The format of the timestamp is determined by the state of the Frame Timestamp Select ([FTSS](#)) bit in the OPEN Alliance Configuration 0 ([11.1.5. OA\\_CONFIG0](#)) register.



**11.1.15 Transmit Timestamp Capture C (High)****Name:** TTSCCH**Address:** 0x0014

|        |                    |    |    |    |    |    |    |    |
|--------|--------------------|----|----|----|----|----|----|----|
| Bit    | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TIMESTAMP_C[63:56] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TIMESTAMP_C[55:48] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TIMESTAMP_C[47:40] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TIMESTAMP_C[39:32] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – TIMESTAMP\_C[63:32] Captured Egress Timestamp C**

This field contains the 32 most significant bits of the 64-bit captured egress frame timestamp. The format of the timestamp is determined by the state of the Frame Timestamp Select ([FTSS](#)) bit in the OPEN Alliance Configuration 0 ([11.1.5. OA\\_CONFIG0](#)) register.

**11.1.16 Transmit Timestamp Capture C (Low)****Name:** TTSCCL**Address:** 0x0015

|        |                    |    |    |    |    |    |    |    |
|--------|--------------------|----|----|----|----|----|----|----|
| Bit    | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TIMESTAMP_C[31:24] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TIMESTAMP_C[23:16] |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TIMESTAMP_C[15:8]  |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TIMESTAMP_C[7:0]   |    |    |    |    |    |    |    |
| Access | RO                 | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – TIMESTAMP\_C[31:0] Captured Egress Timestamp C**

This field contains the 32 least significant bits of the 64-bit captured egress frame timestamp. The format of the timestamp is determined by the state of the Frame Timestamp Select ([FTSS](#)) bit in the OPEN Alliance Configuration 0 ([11.1.5. OA\\_CONFIG0](#)) register.

### 11.1.17 Basic Control

**Name:** BASIC\_CONTROL

**Address:** 0xFF00

Clause 22 Basic Control Register

| Bit    | 15       | 14       | 13         | 12        | 11  | 10  | 9         | 8        |
|--------|----------|----------|------------|-----------|-----|-----|-----------|----------|
|        | SW_RESET | LOOPBACK | SPD_SEL[0] | AUTONEGEN | PD  |     | REAUTONEG | DUPLEXMD |
| Access | R/W SC   | R/W      | RO         | RO        | R/W | R/W | RO        | RO       |
| Reset  | 0        | 0        | 0          | 0         | 0   | 0   | 0         | 0        |

| Bit    | 7   | 6          | 5  | 4  | 3  | 2  | 1  | 0  |
|--------|-----|------------|----|----|----|----|----|----|
|        |     | SPD_SEL[1] |    |    |    |    |    |    |
| Access | R/W | RO         | RO | RO | RO | RO | RO | RO |
| Reset  | 0   | 0          | 0  | 0  | 0  | 0  | 0  | 0  |

#### Bit 15 – SW\_RESET PHY Soft Reset

Writing a '1' to this bit will initiate a software reset of the integrated PHY. A software reset will restore all integrated PHY registers to their default state, except for those fields identified as "NASR", Not Affected by Software Reset.

**Note:** This bit is self-clearing. When setting this bit, do not set other bits in this register.

| Value | Description                   |
|-------|-------------------------------|
| 0     | Normal operation              |
| 1     | integrated PHY software reset |

#### Bit 14 – LOOPBACK Near-End Loopback

When set, this bit enables a near-end loopback. When enabled, transmit data (TXD) pins from the MAC will be looped back onto the receive data (RXD) pins to the MAC. In this mode, no signal is transmitted onto the network media.



**Important:** PLCA must be disabled or configured as the PLCA Coordinator (Local ID = 0) when the near-end loopback mode is enabled.

| Value | Description                   |
|-------|-------------------------------|
| 0     | Normal operation              |
| 1     | Enable near-end loopback mode |

#### Bit 13 – SPD\_SEL[0] PHY Speed Select

Together with [SPD\\_SEL\[1\]](#), sets the network communication speed.

**Note:** Only 10 Mbit/s is supported. This bit is always '0'.

| Value | Description |
|-------|-------------|
| 00    | 10 Mbit/s   |
| 01    | 100 Mbit/s  |
| 10    | 1000 Mbit/s |
| 11    | Reserved    |

#### Bit 12 – AUTONEGEN Auto-Negotiation Enable

**Note:** Auto-negotiation is not supported. This bit is always '0'.

| Value | Description                    |
|-------|--------------------------------|
| 0     | Disable auto-negotiate process |
| 1     | Enable auto-negotiate process  |

**Bit 11 – PD** Power Down

Setting this bit will power down the PMA transceiver leaving the remainder of the device functional.

**Note:** This bit is the same as the Low Power Enable bit in the 10BASE-T1S PMA Control register.

| Value | Description              |
|-------|--------------------------|
| 0     | Normal operation         |
| 1     | PMA will be powered down |

**Bit 9 – REAUTONEG** Restart Auto-Negotiation

**Note:** Auto-negotiation is not supported. This bit is always '0'.

| Value | Description                    |
|-------|--------------------------------|
| 0     | Normal operation               |
| 1     | Restart auto-negotiate process |

**Bit 8 – DUPLEXMD** Duplex Mode

This bit configures the PHY for full-duplex or half-duplex network communication.

**Note:** Only half duplex operation is supported. This bit is always '0'.

| Value | Description |
|-------|-------------|
| 0     | Half duplex |
| 1     | Full duplex |

**Bit 6 – SPD\_SEL[1]** PHY Speed Select

See description for [SPD\\_SEL\[0\]](#) for details.

**Note:** Only 10 Mbit/s operation is supported. This bit is always '0'.

**11.1.18 Basic Status****Name:** BASIC\_STATUS**Address:** 0xFF01

Clause 22 Basic Status Register

| Bit    | 15      | 14        | 13        | 12      | 11      | 10        | 9         | 8      |
|--------|---------|-----------|-----------|---------|---------|-----------|-----------|--------|
|        | 100BT4A | 100BTXFDA | 100BTXHDA | 10BTFDA | 10BTHDA | 100BT2FDA | 100BT2HDA | EXTSTS |
| Access | RO      | RO        | RO        | RO      | RO      | RO        | RO        | RO     |
| Reset  | 0       | 0         | 0         | 0       | 1       | 0         | 0         | 0      |

| Bit    | 7  | 6  | 5        | 4      | 3        | 2      | 1      | 0       |
|--------|----|----|----------|--------|----------|--------|--------|---------|
|        |    |    | AUTONEGC | RMTFLT | AUTONEGA | LNKSTS | JABDET | EXTCAPA |
| Access | RO | RO | RO       | RO     | RO       | RO     | RC     | RO      |
| Reset  | 0  | 0  | 0        | 0      | 0        | 1      | 0      | 1       |

**Bit 15 – 100BT4A** 100BASE-T4 Ability**Note:** 100BASE-T4 operation is not supported. This bit is always '0'.

| Value | Description                           |
|-------|---------------------------------------|
| 0     | PHY not able to operate at 100BASE-T4 |
| 1     | PHY able to operate at 100BASE-T4     |

**Bit 14 – 100BTXFDA** 100BASE-TX Full Duplex Ability**Note:** 100BASE-TX full duplex operation is not supported. This bit is always '0'.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | PHY not able to perform full duplex 100BASE-TX |
| 1     | PHY able to perform full duplex 100BASE-TX     |

**Bit 13 – 100BTXHDA** 100BASE-TX Half Duplex Ability**Note:** 100BASE-TX half duplex operation is not supported. This bit is always '0'.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | PHY not able to perform half duplex 100BASE-TX |
| 1     | PHY able to perform half duplex 100BASE-TX     |

**Bit 12 – 10BTFDA** 10BASE-T Full Duplex Ability**Note:** Full duplex operation is not supported. This bit is always '0'.

| Value | Description                                         |
|-------|-----------------------------------------------------|
| 0     | PHY not able to operate at 10 Mbit/s in full duplex |
| 1     | PHY able to operate at 10 Mbit/s in full duplex     |

**Bit 11 – 10BTHDA** 10BASE-T Half Duplex Ability**Note:** Half duplex operation is supported. This bit is always '1'.

| Value | Description                                         |
|-------|-----------------------------------------------------|
| 0     | PHY not able to operate at 10 Mbit/s in half duplex |
| 1     | PHY able to operate at 10 Mbit/s in half duplex     |

**Bit 10 – 100BT2FDA** 100BASE-T2 Full Duplex Ability**Note:** 100BASE-T2 full duplex operation is not supported. This bit is always '0'.

| Value | Description                                          |
|-------|------------------------------------------------------|
| 0     | PHY not able to operate at 100BASE-T2 in full duplex |
| 1     | PHY able to operate at 100BASE-T2 in full duplex     |

**Bit 9 – 100BT2HDA** 100BASE-T2 Half Duplex Ability**Note:** 100BASE-T2 half duplex operation is not supported. This bit is always '0'.

| Value | Description                                          |
|-------|------------------------------------------------------|
| 0     | PHY not able to operate at 100BASE-T2 in half duplex |
| 1     | PHY able to operate at 100BASE-T2 in half duplex     |

**Bit 8 – EXTSTS** Extended status information ability**Note:** Extended status information is not available. This bit is always '0'.

| Value | Description                                       |
|-------|---------------------------------------------------|
| 0     | No extended status information in register 0xFF0F |
| 1     | Extended status information in register 0xFF0F    |

**Bit 5 – AUTONEGC** Auto-Negotiation Complete**Note:** Auto-negotiation is not supported. This bit is always '0'.

| Value | Description                                |
|-------|--------------------------------------------|
| 0     | Auto-negotiation process has not completed |
| 1     | Auto-negotiation process has completed     |

**Bit 4 – RMTFLT** Remote Fault Detection**Note:** Remote fault detection is not supported. This bit is always '0'.

| Value | Description                        |
|-------|------------------------------------|
| 0     | No remote fault condition detected |
| 1     | Remote fault condition detected    |

**Bit 3 – AUTONEGA** Auto-Negotiation Ability**Note:** Auto-negotiation is not supported. This bit is always '0'.

| Value | Description                                 |
|-------|---------------------------------------------|
| 0     | PHY is not able to perform auto-negotiation |
| 1     | PHY is able to perform auto-negotiation     |

**Bit 2 – LNKSTS** Link Status**Note:** Link status indication is not supported. This bit is always '1'.

| Value | Description          |
|-------|----------------------|
| 0     | Network link is down |
| 1     | Network link is up   |

**Bit 1 – JABDET** Jabber Detection Status

This bit is set on detection of a jabber condition.

| Value | Description                  |
|-------|------------------------------|
| 0     | No jabber condition detected |
| 1     | Jabber condition detected    |

**Bit 0 – EXTCAPA** Extended Capabilities Ability

When this bit is clear, it indicates that only the basic capability registers BASIC\_CONTROL and BASIC\_STATUS are available. When set, then extended registers in the range of 0xFF02-0xFF0F are available in addition to the basic capability registers.

**Note:** Extended capabilities registers are supported. This bit is always '1'.

| Value | Description                                                                                                                                                            |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Extended capabilities registers between 0xFF02-0xFF0F are not supported. Only the basic capabilities registers BASIC_CONTROL and BASIC_STATUS registers are supported. |
| 1     | Extended capabilities registers between 0xFF02-0xFF0F are supported in addition to basic capabilities registers BASIC_CONTROL and BASIC_STATUS.                        |

### 11.1.19 PHY Identifier 1 Register

**Name:** PHY\_ID1

**Address:** 0xFF02

|        |            |    |    |    |    |    |    |    |
|--------|------------|----|----|----|----|----|----|----|
| Bit    | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | OUI[2:9]   |    |    |    |    |    |    |    |
| Access | RO         | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | OUI[10:17] |    |    |    |    |    |    |    |
| Access | RO         | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0          | 0  | 0  | 0  | 0  | 1  | 1  | 1  |

**Bits 15:8 – OUI[2:9]** Organizationally Unique Identifier

This field contains the 3<sup>rd</sup> through the 10<sup>th</sup> bits of the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22. OUI = 00800Fh

**Bits 7:0 – OUI[10:17]** Organizationally Unique Identifier

This field contains the 11<sup>th</sup> through the 18<sup>th</sup> bits of the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22. OUI = 00800Fh

### 11.1.20 PHY Identifier 2 Register

**Name:** PHY\_ID2  
**Address:** 0xFF03

This register contains the model number and hardware revision for the integrated PHY block only.

|        |            |    |    |    |    |    |            |    |
|--------|------------|----|----|----|----|----|------------|----|
| Bit    | 15         | 14 | 13 | 12 | 11 | 10 | 9          | 8  |
|        | OUI[18:23] |    |    |    |    |    | MODEL[5:4] |    |
| Access | RO         | RO | RO | RO | RO | RO | RO         | RO |
| Reset  | 1          | 1  | 0  | 0  | 0  | 0  | 0          | 1  |

|        |            |    |    |    |          |    |    |    |
|--------|------------|----|----|----|----------|----|----|----|
| Bit    | 7          | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
|        | MODEL[3:0] |    |    |    | REV[3:0] |    |    |    |
| Access | RO         | RO | RO | RO | RO       | RO | RO | RO |
| Reset  | 1          | 0  | 1  | 1  | 0        | 0  | 1  | 1  |

#### Bits 15:10 – OUI[18:23] Organizationally Unique Identifier

This field contains the 19<sup>th</sup> through the 24<sup>th</sup> bits of the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22. OUI = 00800Fh

#### Bits 9:4 – MODEL[5:0] Manufacturer's Model Number

Six-bit manufacturer's integrated PHY identification number.

| Value  | Description              |
|--------|--------------------------|
| 011011 | LAN8650/1 Integrated PHY |

#### Bits 3:0 – REV[3:0] Manufacturer's Revision Number

Four-bit integrated PHY revision number.

| Value | Description        |
|-------|--------------------|
| 0011  | Silicon revision 3 |



### 11.1.21 MMD Access Control Register

**Name:** MMDCTRL  
**Address:** 0xFF0D

|        |            |     |    |            |     |     |     |     |
|--------|------------|-----|----|------------|-----|-----|-----|-----|
| Bit    | 15         | 14  | 13 | 12         | 11  | 10  | 9   | 8   |
|        | FNCTN[1:0] |     |    |            |     |     |     |     |
| Access | R/W        | R/W | RO | RO         | RO  | RO  | RO  | RO  |
| Reset  | 0          | 0   | 0  | 0          | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5  | 4          | 3   | 2   | 1   | 0   |
|        |            |     |    | DEVAD[4:0] |     |     |     |     |
| Access | RO         | RO  | RO | R/W        | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0  | 0          | 0   | 0   | 0   | 0   |

#### Bits 15:14 – FNCTN[1:0] MMD Function

This field specifies the action to be performed when reading or writing the MMD Access Address/Data register.

| Value | Description                               |
|-------|-------------------------------------------|
| 00    | Address                                   |
| 01    | Data - No post increment                  |
| 10    | Data - Post increment on reads and writes |
| 11    | Data - Post increment on writes only      |

#### Bits 4:0 – DEVAD[4:0] Device Address

Address of the MDIO Manageable Device to access.

| Value  | Description              |
|--------|--------------------------|
| 00001  | PMA/PMD                  |
| 00011  | PCS                      |
| 11111  | Vendor Specific 2        |
| Others | Reserved - do not access |

**11.1.22 MMD Access Address/Data Register****Name:** MMDAD**Address:** 0xFF0E

|        |                |     |     |     |     |     |     |     |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15             | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ADR_DATA[15:8] |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7              | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ADR_DATA[7:0]  |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:0 – ADR\_DATA[15:0] MMD Address / Data**

Functionality depends on the MMD Function (FNCTN) bits in the MMD Access Control (MMDCTRL) register as specified in IEEE Std 802.3 Annex 22D:

- 00b = Writing this field sets the offset of the register within the MMD to access
- 01b, 10b, 11b = When written, the contents are written into the MMD register
- 01b, 10b, 11b = When read, the contents from the MMD register are returned

## 11.2 MAC Registers

The MAC registers are located within Memory Map Selector 1 (MMS1).



RESERVED address space must not be written except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Refer to the Register Bit Types section for details on register bit attribute notation.

| Address             | Name     | Bit Pos. | 7           | 6      | 5    | 4          | 3    | 2      | 1     | 0     |
|---------------------|----------|----------|-------------|--------|------|------------|------|--------|-------|-------|
| 0x00                | NCR      | 31:24    |             |        |      |            |      |        |       |       |
|                     |          | 23:16    |             |        |      |            |      |        |       |       |
|                     |          | 15:8     |             |        |      |            |      |        |       |       |
|                     |          | 7:0      |             |        |      |            | TXEN | RXEN   | LBL   |       |
| 0x01                | NCFGR    | 31:24    |             |        | RXBP |            |      | IRXFCS | EFRHD |       |
|                     |          | 23:16    |             |        |      |            |      |        | RFCS  | LFERD |
|                     |          | 15:8     |             |        |      |            |      |        |       | MAXFS |
|                     |          | 7:0      | UNIHEN      | MTIHEN | NBC  | CAF        |      | DNVLAN |       |       |
| 0x05<br>...<br>0x1F | Reserved |          |             |        |      |            |      |        |       |       |
| 0x20                | HRB      | 31:24    | ADDR[31:24] |        |      |            |      |        |       |       |
|                     |          | 23:16    | ADDR[23:16] |        |      |            |      |        |       |       |
|                     |          | 15:8     | ADDR[15:8]  |        |      |            |      |        |       |       |
|                     |          | 7:0      | ADDR[7:0]   |        |      |            |      |        |       |       |
| 0x21                | HRT      | 31:24    | ADDR[31:24] |        |      |            |      |        |       |       |
|                     |          | 23:16    | ADDR[23:16] |        |      |            |      |        |       |       |
|                     |          | 15:8     | ADDR[15:8]  |        |      |            |      |        |       |       |
|                     |          | 7:0      | ADDR[7:0]   |        |      |            |      |        |       |       |
| 0x22                | SAB1     | 31:24    | ADDR[31:24] |        |      |            |      |        |       |       |
|                     |          | 23:16    | ADDR[23:16] |        |      |            |      |        |       |       |
|                     |          | 15:8     | ADDR[15:8]  |        |      |            |      |        |       |       |
|                     |          | 7:0      | ADDR[7:0]   |        |      |            |      |        |       |       |
| 0x23                | SAT1     | 31:24    |             |        |      |            |      |        |       |       |
|                     |          | 23:16    |             |        |      |            |      |        |       | FLTTP |
|                     |          | 15:8     | ADDR[47:40] |        |      |            |      |        |       |       |
|                     |          | 7:0      | ADDR[39:32] |        |      |            |      |        |       |       |
| 0x24                | SAB2     | 31:24    | ADDR[31:24] |        |      |            |      |        |       |       |
|                     |          | 23:16    | ADDR[23:16] |        |      |            |      |        |       |       |
|                     |          | 15:8     | ADDR[15:8]  |        |      |            |      |        |       |       |
|                     |          | 7:0      | ADDR[7:0]   |        |      |            |      |        |       |       |
| 0x25                | SAT2     | 31:24    |             |        |      | FLTBM[5:0] |      |        |       |       |
|                     |          | 23:16    |             |        |      |            |      |        |       | FLTTP |
|                     |          | 15:8     | ADDR[47:40] |        |      |            |      |        |       |       |
|                     |          | 7:0      | ADDR[39:32] |        |      |            |      |        |       |       |
| 0x26                | SAB3     | 31:24    | ADDR[31:24] |        |      |            |      |        |       |       |
|                     |          | 23:16    | ADDR[23:16] |        |      |            |      |        |       |       |
|                     |          | 15:8     | ADDR[15:8]  |        |      |            |      |        |       |       |
|                     |          | 7:0      | ADDR[7:0]   |        |      |            |      |        |       |       |
| 0x27                | SAT3     | 31:24    |             |        |      | FLTBM[5:0] |      |        |       |       |
|                     |          | 23:16    |             |        |      |            |      |        |       | FLTTP |
|                     |          | 15:8     | ADDR[47:40] |        |      |            |      |        |       |       |
|                     |          | 7:0      | ADDR[39:32] |        |      |            |      |        |       |       |
| 0x28                | SAB4     | 31:24    | ADDR[31:24] |        |      |            |      |        |       |       |
|                     |          | 23:16    | ADDR[23:16] |        |      |            |      |        |       |       |
|                     |          | 15:8     | ADDR[15:8]  |        |      |            |      |        |       |       |
|                     |          | 7:0      | ADDR[7:0]   |        |      |            |      |        |       |       |

.....continued

| Address               | Name     | Bit Pos. | 7            | 6 | 5           | 4 | 3 | 2 | 1 | 0      |
|-----------------------|----------|----------|--------------|---|-------------|---|---|---|---|--------|
| 0x29                  | SAT4     | 31:24    |              |   | FLTBM[5:0]  |   |   |   |   |        |
|                       |          | 23:16    |              |   |             |   |   |   |   | FLTTYP |
|                       |          | 15:8     | ADDR[47:40]  |   |             |   |   |   |   |        |
|                       |          | 7:0      | ADDR[39:32]  |   |             |   |   |   |   |        |
| 0x2A                  | TIDM1    | 31:24    | ENID         |   |             |   |   |   |   |        |
|                       |          | 23:16    |              |   |             |   |   |   |   |        |
|                       |          | 15:8     | TID[15:8]    |   |             |   |   |   |   |        |
|                       |          | 7:0      | TID[7:0]     |   |             |   |   |   |   |        |
| 0x2B                  | TIDM2    | 31:24    | ENID         |   |             |   |   |   |   |        |
|                       |          | 23:16    |              |   |             |   |   |   |   |        |
|                       |          | 15:8     | TID[15:8]    |   |             |   |   |   |   |        |
|                       |          | 7:0      | TID[7:0]     |   |             |   |   |   |   |        |
| 0x2C                  | TIDM3    | 31:24    | ENID         |   |             |   |   |   |   |        |
|                       |          | 23:16    |              |   |             |   |   |   |   |        |
|                       |          | 15:8     | TID[15:8]    |   |             |   |   |   |   |        |
|                       |          | 7:0      | TID[7:0]     |   |             |   |   |   |   |        |
| 0x2D                  | TIDM4    | 31:24    | ENID         |   |             |   |   |   |   |        |
|                       |          | 23:16    |              |   |             |   |   |   |   |        |
|                       |          | 15:8     | TID[15:8]    |   |             |   |   |   |   |        |
|                       |          | 7:0      | TID[7:0]     |   |             |   |   |   |   |        |
| 0x31                  | Reserved |          |              |   |             |   |   |   |   |        |
| 0x32                  | SAMB1    | 31:24    | ADDR[31:24]  |   |             |   |   |   |   |        |
|                       |          | 23:16    | ADDR[23:16]  |   |             |   |   |   |   |        |
|                       |          | 15:8     | ADDR[15:8]   |   |             |   |   |   |   |        |
|                       |          | 7:0      | ADDR[7:0]    |   |             |   |   |   |   |        |
| 0x33                  | SAMT1    | 31:24    |              |   |             |   |   |   |   |        |
|                       |          | 23:16    |              |   |             |   |   |   |   |        |
|                       |          | 15:8     | ADDR[47:40]  |   |             |   |   |   |   |        |
|                       |          | 7:0      | ADDR[39:32]  |   |             |   |   |   |   |        |
| 0x37<br>...<br>0x6E   | Reserved |          |              |   |             |   |   |   |   |        |
| 0x6F                  | TISUBN   | 31:24    | LSBTIR[7:0]  |   |             |   |   |   |   |        |
|                       |          | 23:16    |              |   |             |   |   |   |   |        |
|                       |          | 15:8     | MSBTIR[15:8] |   |             |   |   |   |   |        |
|                       |          | 7:0      | MSBTIR[7:0]  |   |             |   |   |   |   |        |
| 0x70                  | TSH      | 31:24    |              |   |             |   |   |   |   |        |
|                       |          | 23:16    |              |   |             |   |   |   |   |        |
|                       |          | 15:8     | TCS[47:40]   |   |             |   |   |   |   |        |
|                       |          | 7:0      | TCS[39:32]   |   |             |   |   |   |   |        |
| 0x74                  | TSL      | 31:24    | TCS[31:24]   |   |             |   |   |   |   |        |
|                       |          | 23:16    | TCS[23:16]   |   |             |   |   |   |   |        |
|                       |          | 15:8     | TCS[15:8]    |   |             |   |   |   |   |        |
|                       |          | 7:0      | TCS[7:0]     |   |             |   |   |   |   |        |
| 0x75                  | TN       | 31:24    |              |   | TNS[29:24]  |   |   |   |   |        |
|                       |          | 23:16    | TNS[23:16]   |   |             |   |   |   |   |        |
|                       |          | 15:8     | TNS[15:8]    |   |             |   |   |   |   |        |
|                       |          | 7:0      | TNS[7:0]     |   |             |   |   |   |   |        |
| 0x76                  | TA       | 31:24    | ADJ          |   | ITDT[29:24] |   |   |   |   |        |
|                       |          | 23:16    | ITDT[23:16]  |   |             |   |   |   |   |        |
|                       |          | 15:8     | ITDT[15:8]   |   |             |   |   |   |   |        |
|                       |          | 7:0      | ITDT[7:0]    |   |             |   |   |   |   |        |
| 0x77                  | TI       | 31:24    |              |   |             |   |   |   |   |        |
|                       |          | 23:16    |              |   |             |   |   |   |   |        |
|                       |          | 15:8     |              |   |             |   |   |   |   |        |
|                       |          | 7:0      | CNS[7:0]     |   |             |   |   |   |   |        |
| 0x7B<br>...<br>0x01FF | Reserved |          |              |   |             |   |   |   |   |        |

.....continued

| Address | Name     | Bit Pos. | 7 | 6 | 5         | 4        | 3             | 2 | 1 | 0 |
|---------|----------|----------|---|---|-----------|----------|---------------|---|---|---|
| 0x0200  | BMGR_CTL | 31:24    |   |   |           |          |               |   |   |   |
|         |          | 23:16    |   |   |           |          |               |   |   |   |
|         |          | 15:8     |   |   |           |          |               |   |   |   |
|         |          | 7:0      |   |   | SNAPSTATS | CLRSTATS |               |   |   |   |
| 0x0204  | Reserved |          |   |   |           |          |               |   |   |   |
| ...     |          |          |   |   |           |          |               |   |   |   |
| 0x0207  |          |          |   |   |           |          |               |   |   |   |
| 0x0208  | STATS0   | 31:24    |   |   |           |          | RXSE[7:0]     |   |   |   |
|         |          | 23:16    |   |   |           |          | LFER[7:0]     |   |   |   |
|         |          | 15:8     |   |   |           |          | OFRX[7:0]     |   |   |   |
|         |          | 7:0      |   |   |           |          | UFRX[7:0]     |   |   |   |
| 0x0209  | STATS1   | 31:24    |   |   |           |          | RXRER[7:0]    |   |   |   |
|         |          | 23:16    |   |   |           |          | RXBOVR[7:0]   |   |   |   |
|         |          | 15:8     |   |   |           |          | RXFOVR[7:0]   |   |   |   |
|         |          | 7:0      |   |   |           |          |               |   |   |   |
| 0x020A  | STATS2   | 31:24    |   |   |           |          |               |   |   |   |
|         |          | 23:16    |   |   |           |          |               |   |   |   |
|         |          | 15:8     |   |   |           |          |               |   |   |   |
|         |          | 7:0      |   |   |           |          | FCSE[7:0]     |   |   |   |
| 0x020B  | STATS3   | 31:24    |   |   |           |          | TID4MCNT[7:0] |   |   |   |
|         |          | 23:16    |   |   |           |          | TID3MCNT[7:0] |   |   |   |
|         |          | 15:8     |   |   |           |          | TID2MCNT[7:0] |   |   |   |
|         |          | 7:0      |   |   |           |          | TID1MCNT[7:0] |   |   |   |
| 0x020C  | STATS4   | 31:24    |   |   |           |          | SA4MCNT[7:0]  |   |   |   |
|         |          | 23:16    |   |   |           |          | SA3MCNT[7:0]  |   |   |   |
|         |          | 15:8     |   |   |           |          | SA2MCNT[7:0]  |   |   |   |
|         |          | 7:0      |   |   |           |          | SA1MCNT[7:0]  |   |   |   |
| 0x020D  | STATS5   | 31:24    |   |   |           |          | UHMFRX[7:0]   |   |   |   |
|         |          | 23:16    |   |   |           |          | MHMFRX[7:0]   |   |   |   |
|         |          | 15:8     |   |   |           |          | BFRX[7:0]     |   |   |   |
|         |          | 7:0      |   |   |           |          | VTRX[7:0]     |   |   |   |
| 0x020E  | STATS6   | 31:24    |   |   |           |          | TFRX[31:24]   |   |   |   |
|         |          | 23:16    |   |   |           |          | TFRX[23:16]   |   |   |   |
|         |          | 15:8     |   |   |           |          | TFRX[15:8]    |   |   |   |
|         |          | 7:0      |   |   |           |          | TFRX[7:0]     |   |   |   |
| 0x020F  | STATS7   | 31:24    |   |   |           |          | FRX[31:24]    |   |   |   |
|         |          | 23:16    |   |   |           |          | FRX[23:16]    |   |   |   |
|         |          | 15:8     |   |   |           |          | FRX[15:8]     |   |   |   |
|         |          | 7:0      |   |   |           |          | FRX[7:0]      |   |   |   |
| 0x0210  | STATS8   | 31:24    |   |   |           |          |               |   |   |   |
|         |          | 23:16    |   |   |           |          |               |   |   |   |
|         |          | 15:8     |   |   |           |          |               |   |   |   |
|         |          | 7:0      |   |   |           |          | TXAIE[7:0]    |   |   |   |
| 0x0211  | STATS9   | 31:24    |   |   |           |          | TXAEE[7:0]    |   |   |   |
|         |          | 23:16    |   |   |           |          | TXFUR[7:0]    |   |   |   |
|         |          | 15:8     |   |   |           |          | TXBUR[7:0]    |   |   |   |
|         |          | 7:0      |   |   |           |          |               |   |   |   |
| 0x0212  | STATS10  | 31:24    |   |   |           |          |               |   |   |   |
|         |          | 23:16    |   |   |           |          |               |   |   |   |
|         |          | 15:8     |   |   |           |          |               |   |   |   |
|         |          | 7:0      |   |   |           |          | XCOL[7:0]     |   |   |   |
| 0x0213  | STATS11  | 31:24    |   |   |           |          | TFTX[31:24]   |   |   |   |
|         |          | 23:16    |   |   |           |          | TFTX[23:16]   |   |   |   |
|         |          | 15:8     |   |   |           |          | TFTX[15:8]    |   |   |   |
|         |          | 7:0      |   |   |           |          | TFTX[7:0]     |   |   |   |
| 0x0214  | STATS12  | 31:24    |   |   |           |          | FTX[31:24]    |   |   |   |
|         |          | 23:16    |   |   |           |          | FTX[23:16]    |   |   |   |
|         |          | 15:8     |   |   |           |          | FTX[15:8]     |   |   |   |
|         |          | 7:0      |   |   |           |          | FTX[7:0]      |   |   |   |

## Related Links

[1.3. Register Bit Types](#)

### 11.2.1 MAC Network Control Register

**Name:** MAC\_NCR  
**Address:** 0x000  
**Reset:** 0x00000000  
**Property:** -



**Important:** Reserved fields must be written with their default value.

|        |     |     |     |     |      |      |     |     |
|--------|-----|-----|-----|-----|------|------|-----|-----|
| Bit    | 31  | 30  | 29  | 28  | 27   | 26   | 25  | 24  |
| Access | RO  | RO  | RO  | RO  | RO   | R/W  | R/W | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0    | 0    | 0   | 0   |
| Bit    | 23  | 22  | 21  | 20  | 19   | 18   | 17  | 16  |
| Access | R/W | R/W | R/W | R/W | R/W  | WO   | WO  | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0    | 0    | 0   | 0   |
| Bit    | 15  | 14  | 13  | 12  | 11   | 10   | 9   | 8   |
| Access | R/W | R/W | WO  | WO  | WO   | WO   | WO  | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0    | 0    | 0   | 0   |
| Bit    | 7   | 6   | 5   | 4   | 3    | 2    | 1   | 0   |
| Access | R/W | WO  | WO  | R/W | TXEN | RXEN | LBL | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0    | 0    | 0   | 0   |

#### Bit 3 – TXEN Transmit Enable

Writing a '1' to this bit enables the MAC transmitter to send data.

Writing a '0' to this bit stops transmission immediately, the transmit pipeline is cleared.

| Value | Description          |
|-------|----------------------|
| 0     | Transmit is disabled |
| 1     | Transmit is enabled  |

#### Bit 2 – RXEN Receive Enable

Writing a '1' to this bit enables the MAC to receive data.

Writing a '0' to this bit stops frame reception immediately, and the receive pipeline is cleared.

| Value | Description         |
|-------|---------------------|
| 0     | Receive is disabled |
| 1     | Receive is enabled  |

#### Bit 1 – LBL Loop Back Local

Writing '1' to this bit connects internal MII signals TXD[3:0] to RXD[3:0], TXEN to RXDV, and forces full duplex mode.

RXCK and TXCK to the internal PHY may malfunction as the MAC is switched into and out of internal loop back. It is important that receive and transmit circuits have already been disabled when making the switch into and out of internal loop back.

| Value | Description                 |
|-------|-----------------------------|
| 0     | Loop back local is disabled |
| 1     | Loop back local is enabled  |



### 11.2.2 MAC Network Configuration Register

**Name:** MAC\_NCFGR  
**Address:** 0x001  
**Reset:** 0x00080000  
**Property:** Read/Write



**Important:** Reserved fields must be written with their default value.

|        |        |        |      |     |     |        |       |       |
|--------|--------|--------|------|-----|-----|--------|-------|-------|
| Bit    | 31     | 30     | 29   | 28  | 27  | 26     | 25    | 24    |
|        |        |        | RXBP |     |     | IRXFCS | EFRHD |       |
| Access | R/W    | R/W    | R/W  | R/W | R/W | R/W    | R/W   | R/W   |
| Reset  | 0      | 0      | 0    | 0   | 0   | 0      | 0     | 0     |
| Bit    | 23     | 22     | 21   | 20  | 19  | 18     | 17    | 16    |
|        |        |        |      |     |     |        | RFCS  | LFERD |
| Access | R/W    | R/W    | R/W  | R/W | R/W | R/W    | R/W   | R/W   |
| Reset  | 0      | 0      | 0    | 0   | 1   | 0      | 0     | 0     |
| Bit    | 15     | 14     | 13   | 12  | 11  | 10     | 9     | 8     |
|        |        |        |      |     |     |        |       | MAXFS |
| Access | R/W    | R/W    | R/W  | R/W | R/W | R/W    | R/W   | R/W   |
| Reset  | 0      | 0      | 0    | 0   | 0   | 0      | 0     | 0     |
| Bit    | 7      | 6      | 5    | 4   | 3   | 2      | 1     | 0     |
|        | UNIHEN | MTIHEN | NBC  | CAF |     | DNVLAN |       |       |
| Access | R/W    | R/W    | R/W  | R/W | R/W | R/W    | R/W   | R/W   |
| Reset  | 0      | 0      | 0    | 0   | 0   | 0      | 0     | 0     |

**Bit 29 – RXBP** Receive Bad Preamble

When written to '1', frames with non-standard preamble are not rejected.

**Bit 26 – IRXFCS** Ignore RX FCS

For normal operation this bit must be written to zero.

When this bit is written to '1', frames with FCS/CRC errors will not be rejected. FCS error statistics will still be collected for frames with bad FCS, and FCS status will be recorded in the DMA descriptor of the frame.

**Bit 25 – EFRHD** Enable Frames Received in half-duplex

Writing a '1' to this bit enables frames to be received in half-duplex mode while transmitting.

**Bit 17 – RFCS** Remove FCS

Writing this bit to '1' will cause received frames to be written to memory without their frame check sequence (last 4 bytes). The indicated frame length will be reduced by four bytes in this mode.

**Bit 16 – LFERD** Length Field Error Frame Discard

Writing a '1' to this bit discards frames with a measured length shorter than the extracted length field (as indicated by bytes 13 and 14 in a non-VLAN tagged frame). This only applies to frames with a length field less than 0x0600.

**Bit 8 – MAXFS** 1536 Maximum Frame Size

Writing a '1' to this bit increases the maximum accepted frame size to 1536 bytes in length. When written to '0', any frame above 1518 bytes in length is rejected.

**Note:** To receive maximum sized VLAN tagged frame, 1536 setting is needed.

**Bit 7 – UNIHEN** Unicast Hash Enable

When writing a '1' to this bit, unicast frames will be accepted when the 6-bit hash function of the destination address points to a bit that is set in the Hash Register.

Writing a '0' to this bit disables unicast hashing.

**Bit 6 – MTIHEN** Multicast Hash Enable

When writing a '1' to this bit, multicast frames will be accepted when the 6-bit hash function of the destination address points to a bit that is set in the Hash Register.

Writing a '0' to this bit disables multicast hashing.

**Bit 5 – NBC** No Broadcast

Writing a '1' to this bit will reject frames addressed to the broadcast address 0xFFFFFFFF (all '1').

Writing a '0' to this bit allows broadcasting to 0xFFFFFFFF.

**Bit 4 – CAF** Copy All Frames

When writing a '1' to this bit, all valid frames will be accepted.

**Bit 2 – DNVLAN** Discard Non-VLAN Frames

Writing a '1' to this bit allows only VLAN-tagged frames to pass to the address matching logic.

Writing a '0' to this bit allows both VLAN-tagged and untagged frames to pass to the address matching logic.

### 11.2.3 MAC Hash Register Bottom

**Name:** MAC\_HRB  
**Address:** 0x020  
**Reset:** 0x00000000  
**Property:** Read/Write

The unicast hash enable (UNIHEN) and the multicast hash enable (MITIHEN) bits in the Network Configuration Register (MAC\_NCFGR) enable the reception of hash matched frames.

|        |             |     |     |     |     |     |     |     |
|--------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ADDR[31:24] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | ADDR[23:16] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ADDR[15:8]  |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ADDR[7:0]   |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

#### Bits 31:0 – ADDR[31:0] Hash Address

The first 32 bits of the Hash Address Register.

## 11.2.4 MAC Hash Register Top

**Name:** MAC\_HRT  
**Address:** 0x021  
**Reset:** 0x00000000  
**Property:** Read/Write

The Unicast Hash Enable (UNIHEN) and the Multicast Hash Enable (MITHEN) bits in the Network Configuration Register (MAC\_NCFGR) enable the reception of hash matched frames.

|        |             |     |     |     |     |     |     |     |
|--------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ADDR[31:24] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | ADDR[23:16] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ADDR[15:8]  |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ADDR[7:0]   |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – ADDR[31:0]** Hash Address  
 Bits 63 to 32 of the Hash Address Register.

**11.2.5 MAC Specific Address 1 Bottom Register**

**Name:** MAC\_SAB1  
**Address:** 0x022  
**Reset:** 0x00000000  
**Property:** Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

|        |             |     |     |     |     |     |     |     |
|--------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ADDR[31:24] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | ADDR[23:16] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ADDR[15:8]  |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ADDR[7:0]   |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – ADDR[31:0] Specific Address 1**

Least significant 32 bits of the destination address, that is, bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

### 11.2.6 MAC Specific Address 1 Top Register

**Name:** MAC\_SAT1  
**Address:** 0x023  
**Reset:** 0x00000000  
**Property:** Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

|        |             |     |     |     |     |     |     |       |
|--------|-------------|-----|-----|-----|-----|-----|-----|-------|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24    |
| Access | RO          | RO  | RO  | RO  | RO  | RO  | RO  | RO    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0     |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16    |
| Access | RO          | RO  | RO  | RO  | RO  | RO  | RO  | FLTYP |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0     |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8     |
|        | ADDR[47:40] |     |     |     |     |     |     |       |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W   |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0     |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0     |
|        | ADDR[39:32] |     |     |     |     |     |     |       |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W   |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0     |

#### Bit 16 – FLTYP Filter Type 1

This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter.

#### Bits 15:0 – ADDR[47:32] Specific Address 1

The most significant bits of the destination address, that is, bits 47:32.

**11.2.7 MAC Specific Address 2 Bottom Register**

**Name:** MAC\_SAB2  
**Address:** 0x024  
**Reset:** 0x00000000  
**Property:** Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

|        |             |     |     |     |     |     |     |     |
|--------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ADDR[31:24] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | ADDR[23:16] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ADDR[15:8]  |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ADDR[7:0]   |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – ADDR[31:0] Specific Address 2**

Least significant 32 bits of the destination address, that is, bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

### 11.2.8 MAC Specific Address 2 Top Register

**Name:** MAC\_SAT2  
**Address:** 0x025  
**Reset:** 0x00000000  
**Property:** Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

|        |             |     |     |     |     |     |     |        |
|--------|-------------|-----|-----|-----|-----|-----|-----|--------|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24     |
|        | FLTBM[5:0]  |     |     |     |     |     |     |        |
| Access | RO          | RO  | R/W | R/W | R/W | R/W | R/W | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16     |
|        |             |     |     |     |     |     |     | FLTTYP |
| Access | RO          | RO  | RO  | RO  | RO  | RO  | RO  | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8      |
|        | ADDR[47:40] |     |     |     |     |     |     |        |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0      |
|        | ADDR[39:32] |     |     |     |     |     |     |        |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |

**Bits 29:24 – FLTBM[5:0]** Filter Byte Mask 2

When set, the associated byte of the specific address will not be compared. Bit 24 controls whether the first byte received should be compared. Bit 29 controls whether the last byte received should be compared.

**Bit 16 – FLTTYP** Filter Type 2

This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter.

**Bits 15:0 – ADDR[47:32]** Specific Address 2

The most significant bits of the destination address, that is, bits 47:32.



### 11.2.9 MAC Specific Address 3 Bottom Register

**Name:** MAC\_SAB3  
**Address:** 0x026  
**Reset:** 0x00000000  
**Property:** Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

|        |             |     |     |     |     |     |     |     |
|--------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ADDR[31:24] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | ADDR[23:16] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ADDR[15:8]  |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ADDR[7:0]   |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – ADDR[31:0] Specific Address 3**

Least significant 32 bits of the destination address, that is, bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

**11.2.10 MAC Specific Address 3 Top Register**

**Name:** MAC\_SAT3  
**Address:** 0x027  
**Reset:** 0x00000000  
**Property:** Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

|        |             |     |     |     |     |     |     |        |
|--------|-------------|-----|-----|-----|-----|-----|-----|--------|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24     |
|        | FLTBM[5:0]  |     |     |     |     |     |     |        |
| Access | RO          | RO  | R/W | R/W | R/W | R/W | R/W | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16     |
|        |             |     |     |     |     |     |     | FLTTYP |
| Access | RO          | RO  | RO  | RO  | RO  | RO  | RO  | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8      |
|        | ADDR[47:40] |     |     |     |     |     |     |        |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0      |
|        | ADDR[39:32] |     |     |     |     |     |     |        |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |

**Bits 29:24 – FLTBM[5:0] Filter Byte Mask 3**

When set, the associated byte of the specific address will not be compared. Bit 24 controls whether the first byte received should be compared. Bit 29 controls whether the last byte received should be compared.

**Bit 16 – FLTTYP Filter Type 3**

This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter.

**Bits 15:0 – ADDR[47:32] Specific Address 3**

The most significant bits of the destination address, that is, bits 47:32.

**11.2.11 MAC Specific Address 4 Bottom Register**

**Name:** MAC\_SAB4  
**Address:** 0x028  
**Reset:** 0x00000000  
**Property:** Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

|        |             |     |     |     |     |     |     |     |
|--------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ADDR[31:24] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | ADDR[23:16] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ADDR[15:8]  |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ADDR[7:0]   |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – ADDR[31:0] Specific Address 4**

Least significant 32 bits of the destination address, that is, bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

**11.2.12 MAC Specific Address 4 Top Register**

**Name:** MAC\_SAT4  
**Address:** 0x029  
**Reset:** 0x00000000  
**Property:** Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

|        |             |     |     |     |     |     |     |        |
|--------|-------------|-----|-----|-----|-----|-----|-----|--------|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24     |
|        | FLTBM[5:0]  |     |     |     |     |     |     |        |
| Access | RO          | RO  | R/W | R/W | R/W | R/W | R/W | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16     |
|        |             |     |     |     |     |     |     | FLTTYP |
| Access | RO          | RO  | RO  | RO  | RO  | RO  | RO  | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8      |
|        | ADDR[47:40] |     |     |     |     |     |     |        |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0      |
|        | ADDR[39:32] |     |     |     |     |     |     |        |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W    |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0      |

**Bits 29:24 – FLTBM[5:0] Filter Byte Mask 4**

When set, the associated byte of the specific address will not be compared. Bit 24 controls whether the first byte received should be compared. Bit 29 controls whether the last byte received should be compared.

**Bit 16 – FLTTYP Filter Type 4**

This control bit selects whether this filter should be comparing the MAC source address or the MAC destination address of the received Ethernet frame. When set to zero, the filter is a destination address filter. When set to one, the filter is a source address filter.

**Bits 15:0 – ADDR[47:32] Specific Address 4**

The most significant bits of the destination address, that is, bits 47:32.

**11.2.13 MAC Type ID Match 1 Register**

**Name:** MAC\_TIDM1  
**Address:** 0x02A  
**Reset:** 0x00000000  
**Property:** Read/Write

|        |           |     |     |     |     |     |     |     |
|--------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ENID      |     |     |     |     |     |     |     |
| Access | R/W       | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        |           |     |     |     |     |     |     |     |
| Access | RO        | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TID[15:8] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TID[7:0]  |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bit 31 – ENID** Enable Copying of TID 1 Matched Frames

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | TID 1 is not part of the comparison match.   |
| 1     | TID 1 is processed for the comparison match. |

**Bits 15:0 – TID[15:0]** Type ID Match 1

For use in comparisons with received frames type ID/length frames.

## 11.2.14 MAC Type ID Match 2 Register

**Name:** MAC\_TIDM2  
**Address:** 0x02B  
**Reset:** 0x00000000  
**Property:** Read/Write

|        |           |     |     |     |     |     |     |     |
|--------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ENID      |     |     |     |     |     |     |     |
| Access | R/W       | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        |           |     |     |     |     |     |     |     |
| Access | RO        | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TID[15:8] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TID[7:0]  |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

### Bit 31 – ENID Enable Copying of TID 2 Matched Frames

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | TID 2 is not part of the comparison match.   |
| 1     | TID 2 is processed for the comparison match. |

### Bits 15:0 – TID[15:0] Type ID Match 2

For use in comparisons with received frames type ID/length frames.

### 11.2.15 MAC Type ID Match 3 Register

**Name:** MAC\_TIDM3  
**Address:** 0x02C  
**Reset:** 0x00000000  
**Property:** Read/Write

|        |           |     |     |     |     |     |     |     |
|--------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ENID      |     |     |     |     |     |     |     |
| Access | R/W       | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        |           |     |     |     |     |     |     |     |
| Access | RO        | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TID[15:8] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TID[7:0]  |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

#### Bit 31 – ENID Enable Copying of TID 3 Matched Frames

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | TID 3 is not part of the comparison match.   |
| 1     | TID 3 is processed for the comparison match. |

#### Bits 15:0 – TID[15:0] Type ID Match 3

For use in comparisons with received frames type ID/length frames.

## 11.2.16 MAC Type ID Match 4 Register

**Name:** MAC\_TIDM4  
**Address:** 0x02D  
**Reset:** 0x00000000  
**Property:** Read/Write

|        |           |     |     |     |     |     |     |     |
|--------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ENID      |     |     |     |     |     |     |     |
| Access | R/W       | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        |           |     |     |     |     |     |     |     |
| Access | RO        | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TID[15:8] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TID[7:0]  |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

### Bit 31 – ENID Enable Copying of TID 4 Matched Frames

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | TID 4 is not part of the comparison match.   |
| 1     | TID 4 is processed for the comparison match. |

### Bits 15:0 – TID[15:0] Type ID Match 4

For use in comparisons with received frames type ID/length frames.



**11.2.17 MAC Specific Address 1 Mask Bottom**

**Name:** MAC\_SAMB1  
**Address:** 0x032  
**Reset:** 0x00000000  
**Property:** -

|        |             |     |     |     |     |     |     |     |
|--------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | ADDR[31:24] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | ADDR[23:16] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ADDR[15:8]  |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ADDR[7:0]   |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – ADDR[31:0] Specific Address 1 Mask**

Setting a bit to '1' masks the corresponding bit in the Specific Address 1 Bottom register (MAC\_SAB1).

## 11.2.18 MAC Specific Address Mask 1 Top

**Name:** MAC\_SAMT1  
**Address:** 0x033  
**Reset:** 0x00000000  
**Property:** -

|        |             |     |     |     |     |     |     |     |
|--------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31          | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
| Access | RO          | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23          | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| Access | RO          | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15          | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ADDR[47:40] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ADDR[39:32] |     |     |     |     |     |     |     |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

### Bits 15:0 – ADDR[47:32] Specific Address 1 Mask

Setting a bit to '1' masks the corresponding bit in the Specific Address 1 register MAC\_SAT1.

**11.2.19 TSU Timer Increment Sub-nanoseconds Register**

**Name:** MAC\_TISUBN  
**Address:** 0x06F  
**Reset:** 0x00000000  
**Property:** Read/Write

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31           | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | LSBTIR[7:0]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23           | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        |              |     |     |     |     |     |     |     |
| Access | RO           | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | MSBTIR[15:8] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | MSBTIR[7:0]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:24 – LSBTIR[7:0]** Lower Significant Bits of Timer Increment Register

The least significant bits 16 bits of the sub nanosecond timer increment. This bitfield combines with LMSBTIR to provide a 24-bit timer\_increment counter. These 24 bits are the sub-ns value which the TSU timer will be incremented each clock cycle.

**Bits 15:0 – MSBTIR[15:0]** Most Significant Bits of Timer Increment Register

The most significant bits 16 bits of the sub nanosecond timer increment. This bitfield combines with LSBTIR to provide a 24-bit timer increment counter. These 24 bits are the sub-ns value which the TSU timer will be incremented each clock cycle. Bit  $n = 2^{(n-24)}$  ns giving a resolution of approximately  $5.86 \times 10^{-17}$  sec (16 bits give 15.2 femtoseconds).

## 11.2.20 TSU Timer Seconds High Register

**Name:** MAC\_TSH  
**Address:** 0x070  
**Reset:** 0x00000000  
**Property:** Read/Write

|        |            |     |     |     |     |     |     |     |
|--------|------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31         | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
| Access | RO         | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23         | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| Access | RO         | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15         | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TCS[47:40] |     |     |     |     |     |     |     |
| Access | R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TCS[39:32] |     |     |     |     |     |     |     |
| Access | R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

### Bits 15:0 – TCS[47:32] Timer Count in Seconds

This register contains the upper 16 bits of the 48-bit timestamp unit seconds counter. It increments by 1 when the TSU nanoseconds counter counts to one second. It may also be incremented when the Timer Adjust Register is written.

**11.2.21 TSU Timer Seconds Low Register**

**Name:** MAC\_TSL  
**Address:** 0x074  
**Reset:** 0x00000000  
**Property:** Read/Write

|        |            |     |     |     |     |     |     |     |
|--------|------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31         | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | TCS[31:24] |     |     |     |     |     |     |     |
| Access | R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23         | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | TCS[23:16] |     |     |     |     |     |     |     |
| Access | R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15         | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TCS[15:8]  |     |     |     |     |     |     |     |
| Access | R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TCS[7:0]   |     |     |     |     |     |     |     |
| Access | R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – TCS[31:0] Timer Count in Seconds**

This register contains the lower 32 bits of the 48-bit timestamp unit seconds counter. It increments by 1 when the TSU nanoseconds counter counts to one second. It may also be incremented when the Timer Adjust Register is written.

**11.2.22 TSU Timer Nanoseconds Register**

**Name:** MAC\_TN  
**Address:** 0x075  
**Reset:** 0x00000000  
**Property:** Read/Write

|        |            |     |            |     |     |     |     |     |
|--------|------------|-----|------------|-----|-----|-----|-----|-----|
| Bit    | 31         | 30  | 29         | 28  | 27  | 26  | 25  | 24  |
|        |            |     | TNS[29:24] |     |     |     |     |     |
| Access | RO         | RO  | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23         | 22  | 21         | 20  | 19  | 18  | 17  | 16  |
|        | TNS[23:16] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15         | 14  | 13         | 12  | 11  | 10  | 9   | 8   |
|        | TNS[15:8]  |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5          | 4   | 3   | 2   | 1   | 0   |
|        | TNS[7:0]   |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – TNS[29:0]** Timer Count in Nanoseconds

This register is writable. It can also be adjusted by writes to the TSU Timer Adjust Register. It increments by the value of the TSU Timer Increment Register each clock cycle.

**11.2.23 TSU Timer Adjust Register**

**Name:** MAC\_TA  
**Address:** 0x076  
**Reset:** 0x00000000  
**Property:** Write-Only

|        |             |    |             |    |    |    |    |    |
|--------|-------------|----|-------------|----|----|----|----|----|
| Bit    | 31          | 30 | 29          | 28 | 27 | 26 | 25 | 24 |
|        | ADJ         |    | ITDT[29:24] |    |    |    |    |    |
| Access | W           | RO | W           | W  | W  | W  | W  | W  |
| Reset  | 0           | 0  | 0           | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23          | 22 | 21          | 20 | 19 | 18 | 17 | 16 |
|        | ITDT[23:16] |    |             |    |    |    |    |    |
| Access | W           | W  | W           | W  | W  | W  | W  | W  |
| Reset  | 0           | 0  | 0           | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15          | 14 | 13          | 12 | 11 | 10 | 9  | 8  |
|        | ITDT[15:8]  |    |             |    |    |    |    |    |
| Access | W           | W  | W           | W  | W  | W  | W  | W  |
| Reset  | 0           | 0  | 0           | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7           | 6  | 5           | 4  | 3  | 2  | 1  | 0  |
|        | ITDT[7:0]   |    |             |    |    |    |    |    |
| Access | W           | W  | W           | W  | W  | W  | W  | W  |
| Reset  | 0           | 0  | 0           | 0  | 0  | 0  | 0  | 0  |

**Bit 31 – ADJ** TSU Timer Adjust

Write as '1' to subtract from the TSU timer. Write as '0' to add to it.

**Bits 29:0 – ITDT[29:0]** Increment/Decrement

The number of nanoseconds to increment or decrement the TSU Timer Nanoseconds Register. If necessary, the TSU Seconds Register will be incremented or decremented.

**11.2.24 TSU Timer Increment Register**

**Name:** MAC\_TI  
**Address:** 0x077  
**Reset:** 0x00000000  
**Property:** Read/Write

|        |          |     |     |     |     |     |     |     |
|--------|----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31       | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        |          |     |     |     |     |     |     |     |
| Access | RO       | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23       | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        |          |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15       | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        |          |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7        | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | CNS[7:0] |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 7:0 – CNS[7:0] Count Nanoseconds**

A count of nanoseconds by which the TSU Timer Nanoseconds Register will be incremented each clock cycle. The register TSU timer Increment Sub-nanoseconds (MAC\_TISUBN) contains the subnanosecond portion of the increment.



**11.2.25 MAC Buffer Manager Control**

**Name:** BMGR\_CTL  
**Address:** 0x0200

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |     |     |
|--------|----|----|----|----|----|----|-----|-----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9   | 8   |
|        |    |    |    |    |    |    |     |     |
| Access | RO | RO | RO | RO | RO | RO | R/W | R/W |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0   | 0   |

|        |    |    |           |          |     |     |     |     |
|--------|----|----|-----------|----------|-----|-----|-----|-----|
| Bit    | 7  | 6  | 5         | 4        | 3   | 2   | 1   | 0   |
|        |    |    | SNAPSTATS | CLRSTATS |     |     |     |     |
| Access | RO | RO | R/W       | R/W      | R/W | R/W | R/W | R/W |
| Reset  | 0  | 0  | 0         | 0        | 1   | 0   | 0   | 0   |

**Bit 5 – SNAPSTATS** Snapshot Statistics Counters

Write this bit to '1' to snapshot all statistics counters.

| Value | Description                                                      |
|-------|------------------------------------------------------------------|
| 0     | Normal Operation. Statistics counters increment normally.        |
| 1     | Snapshot. Statistics counters are frozen at their current value. |

**Bit 4 – CLRSTATS** Clear Statistics Counters

Writing this bit to '1' will clear all statistics counters.

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | Normal operation. Statistics counters increment normally. |
| 1     | Statistics counters are cleared to 0.                     |

**11.2.26 Statistics 0**

**Name:** STATS0  
**Address:** 0x0208  
**Reset:** 0x00000000  
**Property:** -

|        |           |    |    |    |    |    |    |    |
|--------|-----------|----|----|----|----|----|----|----|
| Bit    | 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | RXSE[7:0] |    |    |    |    |    |    |    |
| Access | RC        | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | LFRX[7:0] |    |    |    |    |    |    |    |
| Access | RC        | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | OFRX[7:0] |    |    |    |    |    |    |    |
| Access | RC        | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | UFRX[7:0] |    |    |    |    |    |    |    |
| Access | RC        | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:24 – RXSE[7:0]** Receive Symbol Errors

This bit field counts the number of frames that had RXER asserted during reception. Symbol errors are counted regardless of frame length checks. Receive symbol errors will also be counted as an FCS or alignment error if the frame is between 64 and 1518 bytes (1536 bytes if MAC\_NCFGR.MAXFS=1). If the frame is larger it will be recorded as an Oversize Frame Received (OFRX) error. This field will saturate at 0xFF and will be cleared on read.

**Bits 23:16 – LFRX[7:0]** Length Field Errors

This bit field counts the number of frames received that have a measured length shorter than that extracted from the length field (bytes 13 and 14). This condition is only counted if the value of the length field is less than 0x0600 (1536 bytes), the frame is not of excessive length and checking is enabled by writing a '1' to the Length Field Error Frame Discard bit in the Network Configuration Register (MAC\_NCFGR.LFERD). This field will saturate at 0xFF and will be cleared on read.

**Bits 15:8 – OFRX[7:0]** Oversize Frames Received

This bit field counts the number of frames received exceeding 1518 bytes in length (1536 bytes if MAC\_NCFGR.MAXFS is written to '1') but do not have either a CRC error, an alignment error, nor a receive symbol error. This field will saturate at 0xFF and will be cleared on read.

**Bits 7:0 – UFRX[7:0]** Undersize Frames Received

This bit field counts the number of frames received less than 64 bytes in length that do not have either a CRC error or an alignment error. This field will saturate at 0xFF and will be cleared on read.

**11.2.27 Statistics 1**

**Name:** STATS1  
**Address:** 0x0209  
**Reset:** 0x00000000  
**Property:** -

|        |             |    |    |    |    |    |    |    |
|--------|-------------|----|----|----|----|----|----|----|
| Bit    | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | RXRER[7:0]  |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | RXBOVR[7:0] |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | RXFOVR[7:0] |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        |             |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:24 – RXRER[7:0]** Receive Resource Errors

This bit field counts frames that were not received from the network because there was no internal memory resource available at the beginning of frame reception. The receive frame is ignored. This field will saturate at 0xFF and will be cleared on read.

**Bits 23:16 – RXBOVR[7:0]** Receive Buffer Overruns

This bit field counts the number of frames that are address recognized but dropped due to a receive buffer overrun during the middle of frame reception. This field will saturate at 0xFF and will be cleared on read.

**Bits 15:8 – RXFOVR[7:0]** Receive FIFO Overruns

This bit field counts the number of frames that are address recognized but dropped due to a receive FIFO overrun during the middle of frame reception. This field will saturate at 0xFF and will be cleared on read.

**11.2.28 Statistics 2**

**Name:** STATS2  
**Address:** 0x020A  
**Reset:** 0x00000000  
**Property:** -

|        |           |    |    |    |    |    |    |    |
|--------|-----------|----|----|----|----|----|----|----|
| Bit    | 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        |           |    |    |    |    |    |    |    |
| Access | RO        | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        |           |    |    |    |    |    |    |    |
| Access | RO        | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |           |    |    |    |    |    |    |    |
| Access | RO        | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | FCSE[7:0] |    |    |    |    |    |    |    |
| Access | RC        | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 7:0 – FCSE[7:0] Frame Check Sequence Errors**

The register counts frames that are an integral number of bytes, have bad CRC and are between 64 and 1518 bytes in length (1536 Bytes if MAC\_NCFGR.MAXFS is written to '1'). This register is also incremented if a symbol error is detected and the frame is of valid length and has an integral number of bytes.

This register is incremented for a frame with bad FCS, regardless of whether it is copied to memory due to ignore FCS mode (enabled by writing MAC\_NCFGR.IRXFCS=1).

This field will saturate at 0xFF and will be cleared on read.

**11.2.29 Statistics 3**

**Name:** STATS3  
**Address:** 0x020B  
**Reset:** 0x00000000  
**Property:** -

|        |               |    |    |    |    |    |    |    |
|--------|---------------|----|----|----|----|----|----|----|
| Bit    | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TID4MCNT[7:0] |    |    |    |    |    |    |    |
| Access | RC            | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TID3MCNT[7:0] |    |    |    |    |    |    |    |
| Access | RC            | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TID2MCNT[7:0] |    |    |    |    |    |    |    |
| Access | RC            | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TID1MCNT[7:0] |    |    |    |    |    |    |    |
| Access | RC            | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:24 – TID4MCNT[7:0]** Type ID 4 Match Count  
 This field will saturate at 0xFF and will be cleared on read.

**Bits 23:16 – TID3MCNT[7:0]** Type ID 3 Match Count  
 This field will saturate at 0xFF and will be cleared on read.

**Bits 15:8 – TID2MCNT[7:0]** Type ID 2 Match Count  
 This field will saturate at 0xFF and will be cleared on read.

**Bits 7:0 – TID1MCNT[7:0]** Type ID 1 Match Count  
 This field will saturate at 0xFF and will be cleared on read.

**11.2.30 Statistics 4**

**Name:** STATS4  
**Address:** 0x020C  
**Reset:** 0x00000000  
**Property:** -

|        |              |    |    |    |    |    |    |    |
|--------|--------------|----|----|----|----|----|----|----|
| Bit    | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | SA4MCNT[7:0] |    |    |    |    |    |    |    |
| Access | RC           | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | SA3MCNT[7:0] |    |    |    |    |    |    |    |
| Access | RC           | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | SA2MCNT[7:0] |    |    |    |    |    |    |    |
| Access | RC           | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | SA1MCNT[7:0] |    |    |    |    |    |    |    |
| Access | RC           | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:24 – SA4MCNT[7:0]** Specific Address 4 Match Count  
 This field will saturate at 0xFF and will be cleared on read.

**Bits 23:16 – SA3MCNT[7:0]** Specific Address 3 Match Count  
 This field will saturate at 0xFF and will be cleared on read.

**Bits 15:8 – SA2MCNT[7:0]** Specific Address 2 Match Count  
 This field will saturate at 0xFF and will be cleared on read.

**Bits 7:0 – SA1MCNT[7:0]** Specific Address 1 Match Count  
 This field will saturate at 0xFF and will be cleared on read.

**11.2.31 Statistics 5**

**Name:** STATS5  
**Address:** 0x020D  
**Reset:** 0x00000000  
**Property:** -

|        |             |    |    |    |    |    |    |    |
|--------|-------------|----|----|----|----|----|----|----|
| Bit    | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | UHMFRX[7:0] |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | MHMFRX[7:0] |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | BFRX[7:0]   |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | VTRX[7:0]   |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:24 – UHMFRX[7:0]** Unicast Hash Match Frames Received without Error

This register counts the number of unicast hash matching frames successfully received without error. It is only incremented if the frame is successfully filtered and copied to memory. This field will saturate at 0xFF and will be cleared on read.

**Bits 23:16 – MHMFRX[7:0]** Multicast Hash Match Frames Received without Error

This register counts the number of multicast hash matching frames successfully received without error. It is only incremented if the frame is successfully filtered and copied to memory. This field will saturate at 0xFF and will be cleared on read.

**Bits 15:8 – BFRX[7:0]** Broadcast Frames Received without Error

This bit field counts the number of broadcast frames successfully received without error. It is only incremented if the frame is successfully filtered and copied to memory. This field will saturate at 0xFF and will be cleared on read.

**Bits 7:0 – VTRX[7:0]** VLAN Tagged Frames Received without Error

This bit field counts the number of VLAN tagged frames successfully received without error. It is only incremented if the frame is successfully copied to memory. This field will saturate at 0xFF and will be cleared on read.

## 11.2.32 Statistics 6

**Name:** STATS6  
**Address:** 0x020E  
**Reset:** 0x00000000  
**Property:** -

|        |             |    |    |    |    |    |    |    |
|--------|-------------|----|----|----|----|----|----|----|
| Bit    | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TFRX[31:24] |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TFRX[23:16] |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TFRX[15:8]  |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TFRX[7:0]   |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – TFRX[31:0]** Total Frames Received (including errors)

This bit field counts the number of frames received, including those with errors.  
 This field will saturate at 0xFFFFFFFF and will be cleared on read.



### 11.2.33 Statistics 7

**Name:** STATS7  
**Address:** 0x020F  
**Reset:** 0x00000000  
**Property:** -

|        |            |    |    |    |    |    |    |    |
|--------|------------|----|----|----|----|----|----|----|
| Bit    | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | FRX[31:24] |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | FRX[23:16] |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | FRX[15:8]  |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | FRX[7:0]   |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

#### Bits 31:0 – FRX[31:0] Frames Received without Error

This bit field counts the number of frames successfully received. It is only incremented if the frame is successfully filtered and copied to memory.

This field will saturate at 0xFFFFFFFF and will be cleared on read.

## 11.2.34 Statistics 8

**Name:** STATS8  
**Address:** 0x0210  
**Reset:** 0x00000000  
**Property:** -

|        |            |    |    |    |    |    |    |    |
|--------|------------|----|----|----|----|----|----|----|
| Bit    | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        |            |    |    |    |    |    |    |    |
| Access | RO         | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        |            |    |    |    |    |    |    |    |
| Access | RO         | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |            |    |    |    |    |    |    |    |
| Access | RO         | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TXAIE[7:0] |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 7:0 – TXAIE[7:0]** Transmit Abort Internal Error

This bit field counts the number of frames that were aborted and dropped due to an internal error.  
 This field will saturate at 0xFF and will be cleared on read.

## 11.2.35 Statistics 9

**Name:** STATS9  
**Address:** 0x0211  
**Reset:** 0x00000000  
**Property:** -

|        |            |    |    |    |    |    |    |    |
|--------|------------|----|----|----|----|----|----|----|
| Bit    | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TXAEE[7:0] |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TXFUR[7:0] |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TXBUR[7:0] |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        |            |    |    |    |    |    |    |    |
| Access | RO         | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:24 – TXAEE[7:0]** Transmit Abort External Error

This bit field counts the number of frames that were aborted and dropped due to an external SPI host error. Such errors include:

- Repeated Frame Start - the device received two start-of-frame indication from the SPI host without an end-of-frame.
- Frame received from the SPI host exceeds 1536 bytes in length
- Transmit Frame Check Sequence Error - The SPI host appended Frame Check Sequence (FCS) does not match the frame data received from the host. This may indicate a bit error on SPI, or the host incorrectly calculated the FCS.

This field will saturate at 0xFF and will be cleared on read.

**Bits 23:16 – TXFUR[7:0]** Transmit FIFO Underruns

This bit field counts the number of frames that were dropped due to transmit FIFO underrun during the middle of frame transmission.

This field will saturate at 0xFF and will be cleared on read.

**Bits 15:8 – TXBUR[7:0]** Transmit Buffer Underruns

This bit field counts the number of frames that were dropped due to buffer underrun during the middle of frame transmission.

This field will saturate at 0xFF and will be cleared on read.

### 11.2.36 Statistics 10

**Name:** STATS10  
**Address:** 0x0212  
**Reset:** 0x00000000  
**Property:** -

|        |           |    |    |    |    |    |    |    |
|--------|-----------|----|----|----|----|----|----|----|
| Bit    | 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        |           |    |    |    |    |    |    |    |
| Access | RO        | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        |           |    |    |    |    |    |    |    |
| Access | RO        | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |           |    |    |    |    |    |    |    |
| Access | RO        | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | XCOL[7:0] |    |    |    |    |    |    |    |
| Access | RC        | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

#### Bits 7:0 – XCOL[7:0] Excessive Collisions

This register counts the number of frames that failed to be transmitted because they experienced 16 collisions.

This field will saturate at 0xFF and will be cleared on read.

**11.2.37 Statistics 11**

**Name:** STATS11  
**Address:** 0x0213  
**Reset:** 0x00000000  
**Property:** -

|        |             |    |    |    |    |    |    |    |
|--------|-------------|----|----|----|----|----|----|----|
| Bit    | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | TFTX[31:24] |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | TFTX[23:16] |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TFTX[15:8]  |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TFTX[7:0]   |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – TFTX[31:0] Total Frames Transmitted (including errors)**

This bit field counts the number of frames attempted to be transmitted. This count includes frames that incurred an error while being transmitted.

This field will saturate at 0xFFFFFFFF and will be cleared on read.

**11.2.38 Statistics 12**

**Name:** STATS12  
**Address:** 0x0214  
**Reset:** 0x00000000  
**Property:** -

|        |            |    |    |    |    |    |    |    |
|--------|------------|----|----|----|----|----|----|----|
| Bit    | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | FTX[31:24] |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | FTX[23:16] |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | FTX[15:8]  |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | FTX[7:0]   |    |    |    |    |    |    |    |
| Access | RC         | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – FTX[31:0]** Frames Transmitted without Error

This bit field counts the number of frames successfully transmitted, .i.e., no underrun and not too many retries.

This field will saturate at 0xFFFFFFFF and will be cleared on read.

## 11.3 PHY PCS Registers

The integrated PHY PCS registers are located within Memory Map Selector 2 (MMS2).



RESERVED address space must not be written except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Refer to the Register Bit Types section for details on register bit attribute notation.

| Address               | Name                        | Bit Pos. | 7               | 6   | 5 | 4 | 3 | 2 | 1 | 0      |
|-----------------------|-----------------------------|----------|-----------------|-----|---|---|---|---|---|--------|
| 0x00<br>...<br>0x08F2 | Reserved                    |          |                 |     |   |   |   |   |   |        |
| 0x08F3                | <a href="#">T1SPCCTL</a>    | 15:8     | RST             | LBE |   |   |   |   |   | DUPLEX |
|                       |                             | 7:0      |                 |     |   |   |   |   |   |        |
| 0x08F4                | <a href="#">T1SPCSSTS</a>   | 15:8     |                 |     |   |   |   |   |   |        |
|                       |                             | 7:0      | FAULT           |     |   |   |   |   |   |        |
| 0x08F5                | <a href="#">T1SPCSDIAG1</a> | 15:8     | RMTJABCNT[15:8] |     |   |   |   |   |   |        |
|                       |                             | 7:0      | RMTJABCNT[7:0]  |     |   |   |   |   |   |        |
| 0x08F6                | <a href="#">T1SPCSDIAG2</a> | 15:8     | CORTXCNT[15:8]  |     |   |   |   |   |   |        |
|                       |                             | 7:0      | CORTXCNT[7:0]   |     |   |   |   |   |   |        |

### Related Links

[1.3. Register Bit Types](#)

**11.3.1 10BASE-T1S PCS Control****Name:** T1SPCSCTL**Address:** 0x08F3

|        |        |     |    |    |    |    |    |        |
|--------|--------|-----|----|----|----|----|----|--------|
| Bit    | 15     | 14  | 13 | 12 | 11 | 10 | 9  | 8      |
|        | RST    | LBE |    |    |    |    |    | DUPLEX |
| Access | R/W SC | R/W | RO | RO | RO | RO | RO | RO     |
| Reset  | 0      | 0   | 0  | 0  | 0  | 0  | 0  | 1      |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bit 15 – RST** PCS Reset

When this bit is set, the PCS 4B5B encoder/decoder, scrambler/descrambler, and frame encoder/decoder blocks will be reset.

**Note:** This bit is self-clearing. When setting this bit, do not set other bits in this register.

| Value | Description      |
|-------|------------------|
| 0     | Normal Operation |
| 1     | PCS reset        |

**Bit 14 – LBE** PCS Loopback Enable

When this bit is set, data from the MAC will be passed through the PHY to the PCS and returned back to the MAC. This tests the full path from the MAC media interface through the PCS scrambler/descrambler and 4B/5B encoder/decoder.



**Important:** PLCA must be disabled when the PCS loopback mode is enabled.

| Value | Description               |
|-------|---------------------------|
| 0     | Disable PCS loopback mode |
| 1     | Enable PCS loopback mode  |

**Bit 8 – DUPLEX** Duplex Mode

**Note:** Only half-duplex operation is supported. This bit is always 1.

| Value | Description           |
|-------|-----------------------|
| 0     | Full-duplex operation |
| 1     | Half-duplex operation |



### 11.3.2 10BASE-T1S PCS Status

**Name:** T1SPCSSTS

**Address:** 0x08F4

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        |    |    |    |    |    |    |    |    |
| Access | RC | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

#### Bit 7 – FAULT PCS Fault Indication

This bit will be set when the PCS has detected a fault condition on the receive or transmit path.

**Note:** This bit always reads '0' as there are no detectable PCS faults.

| Value | Description                  |
|-------|------------------------------|
| 0     | No PCS fault detected        |
| 1     | PCS fault condition detected |

### 11.3.3 10BASE-T1S PCS Diagnostic 1

**Name:** T1SPCSDIAG1  
**Address:** 0x08F5

|        |                 |    |    |    |    |    |    |    |
|--------|-----------------|----|----|----|----|----|----|----|
| Bit    | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | RMTJABCNT[15:8] |    |    |    |    |    |    |    |
| Access | RC              | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | RMTJABCNT[7:0]  |    |    |    |    |    |    |    |
| Access | RC              | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 15:0 – RMTJABCNT[15:0] Remote Jabber Count**

Field counting the number of remote jabber events (ESDJAB) received since the last read of the register. This field will saturate at 0xFFFF.

### 11.3.4 10BASE-T1S PCS Diagnostic 2

**Name:** T1SPCSDIAG2

**Address:** 0x08F6

|        |                |    |    |    |    |    |    |    |
|--------|----------------|----|----|----|----|----|----|----|
| Bit    | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | CORTXCNT[15:8] |    |    |    |    |    |    |    |
| Access | RC             | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |               |    |    |    |    |    |    |    |
|--------|---------------|----|----|----|----|----|----|----|
| Bit    | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | CORTXCNT[7:0] |    |    |    |    |    |    |    |
| Access | RC            | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 15:0 – CORTXCNT[15:0] Corrupted Transmit Count**

Field containing the number of times a locally initiated transmission resulted in a corrupted signal at the MDI. Corruption during transmission would typically be due to collisions on the physical layer. This field is self-clearing when read. This field will saturate at 0xFFFF.

## 11.4 PHY PMA/PMD Registers

The integrated PHY PMA/PMD registers are located within Memory Map Selector 3 (MMS3).



RESERVED address space must not be written except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Refer to the Register Bit Types section for details on register bit attribute notation.

| Address                 | Name         | Bit Pos.    | 7           | 6   | 5   | 4 | 3           | 2      | 1    | 0   |
|-------------------------|--------------|-------------|-------------|-----|-----|---|-------------|--------|------|-----|
| 0x00<br>...<br>0x11     | Reserved     |             |             |     |     |   |             |        |      |     |
| 0x12                    | T1PMAPMDEXTA | 15:8<br>7:0 |             |     |     |   | T1SABL      | T1LABL |      |     |
| 0x14<br>...<br>0x0833   | Reserved     |             |             |     |     |   |             |        |      |     |
| 0x0834                  | T1PMAPMDCTL  | 15:8<br>7:0 |             |     |     |   | TYPSEL[3:0] |        |      |     |
| 0x0836<br>...<br>0x08F8 | Reserved     |             |             |     |     |   |             |        |      |     |
| 0x08F9                  | T1SPMACTL    | 15:8<br>7:0 | RST         | TXD |     |   | LPE         | MDE    |      | LBE |
| 0x08FA                  | T1SPMASTS    | 15:8<br>7:0 |             |     | LBA |   | LPA         | MDA    | RXFA |     |
|                         |              |             |             |     |     |   |             |        | RXFD |     |
| 0x08FB                  | T1STSTCTL    | 15:8<br>7:0 | TSTCTL[2:0] |     |     |   |             |        |      |     |

### Related Links

[1.3. Register Bit Types](#)

**11.4.1 BASE-T1 PMA/PMD Extended Ability****Name:** T1PMAPMDEXTA**Address:** 0x0012

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |        |        |    |    |
|--------|----|----|----|----|--------|--------|----|----|
| Bit    | 7  | 6  | 5  | 4  | 3      | 2      | 1  | 0  |
|        |    |    |    |    | T1SABL | T1LABL |    |    |
| Access | RO | RO | RO | RO | RO     | RO     | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 1      | 0      | 0  | 0  |

**Bit 3 – T1SABL** 10BASE-T1S Ability

This bit indicates the ability of the PHY to support 10BASE-T1S.

**Note:** 10BASE-T1S operation is supported. This bit always reads 1.

| Value | Description                                         |
|-------|-----------------------------------------------------|
| 0     | PMA/PMD is not able to perform 10BASE-T1S operation |
| 1     | PMA/PMD is able to perform 10BASE-T1S operation     |

**Bit 2 – T1LABL** 10BASE-T1L Ability

This bit indicates the ability of the PHY to support 10BASE-T1L.

**Note:** 10BASE-T1L operation is not supported. This bit always reads 0.

| Value | Description                                         |
|-------|-----------------------------------------------------|
| 0     | PMA/PMD is not able to perform 10BASE-T1L operation |
| 1     | PMA/PMD is able to perform 10BASE-T1L operation     |

### 11.4.2 BASE-T1 PMA/PMD Control

**Name:** T1PMAPMDCTL

**Address:** 0x0834

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  |

#### Bits 3:0 – TYPSEL[3:0] Type Selection

This field sets the PMA/PMD mode of operation.

**Note:** Only 10BASE-T1S operation is supported. This field always reads 0011b.

| Value | Description |
|-------|-------------|
| 0000b | 100BASE-T1  |
| 0001b | 1000BASE-T1 |
| 0010b | 10BASE-T1L  |
| 0011b | 10BASE-T1S  |
| 01xxb | Reserved    |
| 1xxxb | Reserved    |

### 11.4.3 10BASE-T1S PMA Control

**Name:** T1SPMACTL

**Address:** 0x08F9

|        |        |     |    |    |     |     |    |    |
|--------|--------|-----|----|----|-----|-----|----|----|
| Bit    | 15     | 14  | 13 | 12 | 11  | 10  | 9  | 8  |
|        | RST    | TXD |    |    | LPE | MDE |    |    |
| Access | R/W SC | R/W | RO | RO | R/W | R/W | RO | RO |
| Reset  | 0      | 0   | 0  | 0  | 0   | 0   | 0  | 0  |

|        |    |    |    |    |    |    |    |     |
|--------|----|----|----|----|----|----|----|-----|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
|        |    |    |    |    |    |    |    | LBE |
| Access | RO | RO | RO | RO | RO | RO | RO | R/W |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0   |

#### Bit 15 – RST PMA Reset

Setting this bit will reset the device PMA.

**Note:** This bit is self-clearing. When setting this bit, do not set other bits in this register.

| Value | Description      |
|-------|------------------|
| 0     | Normal Operation |
| 1     | PMA Reset        |

#### Bit 14 – TXD Transmit Disable

The PMA transmit path is disabled when this bit is set. This bit must be clear for normal operation.

| Value | Description      |
|-------|------------------|
| 0     | Normal operation |
| 1     | Transmit disable |

#### Bit 11 – LPE Low Power Enable

Setting this bit will power down the PMA.

**Note:** This bit has the same effect as the Power Down bit in the Clause 22 BASIC\_CONTROL register.

| Value | Description                   |
|-------|-------------------------------|
| 0     | Normal operation              |
| 1     | Place PMA into low-power mode |

#### Bit 10 – MDE Multidrop Enable

When set, this bit will enable multidrop operation on a mixing segment.

**Note:** This bit has no effect on the operation of the device.

| Value | Description                                            |
|-------|--------------------------------------------------------|
| 0     | Disable mixing segment operation (point-to-point mode) |
| 1     | Enable PMA multidrop (mixing segment) operation        |

#### Bit 0 – LBE PMA Loopback Enable

This bit will enable the PMA loopback test mode when set. Data received from the MAC via the media interface will be passed through the PCS scrambler/descrambler, 4B/5B encoder/decoder, and the PMA differential Manchester encoder/decoder and returned back to the MAC.



**Important:** PLCA must be disabled or configured as the PLCA Coordinator (Local ID = 0) when the PMA loopback mode is enabled.

| Value | Description               |
|-------|---------------------------|
| 0     | Disable PMA loopback mode |
| 1     | Enable PMA loopback mode  |



#### 11.4.4 10BASE-T1S PMA Status

**Name:** T1SPMASTS

**Address:** 0x08FA

|        |    |    |     |    |     |     |      |    |
|--------|----|----|-----|----|-----|-----|------|----|
| Bit    | 15 | 14 | 13  | 12 | 11  | 10  | 9    | 8  |
|        |    |    | LBA |    | LPA | MDA | RXFA |    |
| Access | RO | RO | RO  | RO | RO  | RO  | RO   | RO |
| Reset  | 0  | 0  | 1   | 0  | 1   | 1   | 0    | 0  |

|        |    |    |    |    |    |    |      |    |
|--------|----|----|----|----|----|----|------|----|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1    | 0  |
|        |    |    |    |    |    |    | RXFD |    |
| Access | RO | RO | RO | RO | RO | RO | RO   | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0  |

##### Bit 13 – LBA PMA Loopback Ability

This bit indicates that the device has PMA loopback ability.

**Note:** PMA loopback is supported. This bit always reads as 1.

| Value | Description                            |
|-------|----------------------------------------|
| 0     | PHY does not support PMA loopback mode |
| 1     | PHY supports PMA loopback mode         |

##### Bit 11 – LPA Low Power Ability

This bit is set to indicate that the device PMA supports a low power state.

**Note:** PMA low power mode is supported. This bit always reads as 1.

| Value | Description                         |
|-------|-------------------------------------|
| 0     | PMA does not have low power ability |
| 1     | PMA has low power ability           |

##### Bit 10 – MDA Multidrop Ability

This bit is set to indicate that the device supports multidrop operation on a mixing segment.

**Note:** Multidrop mixing segment operation is supported. This bit always reads as 1.

| Value | Description                                                         |
|-------|---------------------------------------------------------------------|
| 0     | PMA does not support mixing segment operation (point-to-point only) |
| 1     | PMA supports multidrop (mixing segment) operation                   |

##### Bit 9 – RXFA Receive Fault Ability

This bit indicates the ability of the device to detect a fault on the PMA receive path.

**Note:** The device is unable to detect a PMA receive path fault. This bit always reads as 0.

| Value | Description                                                  |
|-------|--------------------------------------------------------------|
| 0     | PHY does not have the ability to detect PMA faults           |
| 1     | PHY has the ability to detect faults in the PMA receive path |

##### Bit 1 – RXFD Receive Fault Detection

This bit will be set when the PMA has detected a fault on the receive path.

**Note:** The device PMA does not support PMA receive fault detection. This bit always reads 0.

| Value | Description                  |
|-------|------------------------------|
| 0     | No PMA fault detected        |
| 1     | PMA fault condition detected |

**11.4.5 10BASE-T1S Test Mode Control****Name:** T1STSTCTL**Address:** 0x08FB

|        |             |     |     |    |    |    |    |    |
|--------|-------------|-----|-----|----|----|----|----|----|
| Bit    | 15          | 14  | 13  | 12 | 11 | 10 | 9  | 8  |
|        | TSTCTL[2:0] |     |     |    |    |    |    |    |
| Access | R/W         | R/W | R/W | RO | RO | RO | RO | RO |
| Reset  | 0           | 0   | 0   | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7           | 6   | 5   | 4  | 3  | 2  | 1  | 0  |
|        |             |     |     |    |    |    |    |    |
| Access | RO          | RO  | RO  | RO | RO | RO | RO | RO |
| Reset  | 0           | 0   | 0   | 0  | 0  | 0  | 0  | 0  |

**Bits 15:13 – TSTCTL[2:0] Test Mode Control**

This field configures and enables the various IEEE specified test modes. For a description of the test modes, refer to Clause 147.5.2 of the IEEE 802.3cg™-2019 *Amendment 5: Physical Layers Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors*.

| Value | Description                                             |
|-------|---------------------------------------------------------|
| 000   | Normal (non-test) operation                             |
| 001   | Test mode 1 - Transmitter output voltage, timing jitter |
| 010   | Test mode 2 - Transmitter output droop                  |
| 011   | Test mode 3 - Transmitter PSD mask                      |
| 100   | Test mode 4 - Transmitter high impedance mode           |
| 101   | Reserved                                                |
| 11x   | Reserved                                                |

## 11.5 PHY Vendor Specific Registers

The integrated PHY vendor specific registers are located within Memory Map Selector 4 (MMS4).



RESERVED address space must not be written except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Refer to the Register Bit Types section for details on register bit attribute notation.

| Address             | Name     | Bit Pos.    | 7 | 6 | 5 | 4                              | 3               | 2                  | 1                 | 0               |
|---------------------|----------|-------------|---|---|---|--------------------------------|-----------------|--------------------|-------------------|-----------------|
| 0x00<br>...<br>0x0F | Reserved |             |   |   |   |                                |                 |                    |                   |                 |
| 0x10                | CTRL1    | 15:8<br>7:0 |   |   |   |                                | IWDE            |                    | DIGLBE            |                 |
| 0x12<br>...<br>0x17 | Reserved |             |   |   |   |                                |                 |                    |                   |                 |
| 0x18                | STS1     | 15:8<br>7:0 |   |   |   | SQI<br>BCNBFTO                 | PSTC<br>UNCRS   | TXCOL<br>PLCASYM   | TXJAB<br>ESDERR   | TSSI<br>DEC5B   |
| 0x19                | STS2     | 15:8<br>7:0 |   |   |   |                                |                 | WKEMDI             | WKEWI             | UV33            |
| 0x1A                | STS3     | 15:8<br>7:0 |   |   |   |                                |                 |                    |                   |                 |
| 0x1C                | IMSK1    | 15:8<br>7:0 |   |   |   | SQIM<br>BCNBFTOM               | PSTCM<br>UNCRSM | TXCOLM<br>PLCASYMM | TXJABM<br>ESDERRM | TSSIM<br>DEC5BM |
| 0x1D                | IMSK2    | 15:8<br>7:0 |   |   |   |                                |                 | WKEMDIM            | WKEWIM            | UV33M           |
| 0x1F                | Reserved |             |   |   |   |                                |                 |                    |                   |                 |
| 0x20                | CTRCTRL  | 15:8<br>7:0 |   |   |   |                                |                 |                    | TOCTRE            | BCNCTRE         |
| 0x22<br>...<br>0x23 | Reserved |             |   |   |   |                                |                 |                    |                   |                 |
| 0x24                | TOCNTH   | 15:8<br>7:0 |   |   |   | TOCNT[31:24]<br>TOCNT[23:16]   |                 |                    |                   |                 |
| 0x25                | TOCNTL   | 15:8<br>7:0 |   |   |   | TOCNT[15:8]<br>TOCNT[7:0]      |                 |                    |                   |                 |
| 0x26                | BCNCNTH  | 15:8<br>7:0 |   |   |   | BCNCNT[31:24]<br>BCNCNT[23:16] |                 |                    |                   |                 |
| 0x27                | BCNCNTL  | 15:8<br>7:0 |   |   |   | BCNCNT[15:8]<br>BCNCNT[7:0]    |                 |                    |                   |                 |
| 0x29<br>...<br>0x2F | Reserved |             |   |   |   |                                |                 |                    |                   |                 |
| 0x30                | MULTID0  | 15:8<br>7:0 |   |   |   | ID1[7:0]<br>ID2[7:0]           |                 |                    |                   |                 |
| 0x31                | MULTID1  | 15:8<br>7:0 |   |   |   | ID3[7:0]<br>ID4[7:0]           |                 |                    |                   |                 |
| 0x32                | MULTID2  | 15:8<br>7:0 |   |   |   | ID5[7:0]<br>ID6[7:0]           |                 |                    |                   |                 |
| 0x33                | MULTID3  | 15:8<br>7:0 |   |   |   | ID7[7:0]<br>ID8[7:0]           |                 |                    |                   |                 |
| 0x35                | Reserved |             |   |   |   |                                |                 |                    |                   |                 |
| 0x36                | PRSSTS   | 15:8<br>7:0 |   |   |   | MAXID[7:0]                     |                 |                    |                   |                 |
| 0x38<br>...<br>0x3C | Reserved |             |   |   |   |                                |                 |                    |                   |                 |

.....continued

| Address             | Name      | Bit Pos. | 7        | 6        | 5        | 4        | 3        | 2        | 1    | 0 |
|---------------------|-----------|----------|----------|----------|----------|----------|----------|----------|------|---|
| 0x3D                | PRTMGMT2  | 15:8     |          |          | MIRXWDEN | PRIW DEN | MITXWDEN |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x3E                | IWDTOH    | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x3F                | IWDTOL    | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x40                | TXMCTL    | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      | TXPMD ET |          |          |          |          | MACTXTSE | TXME |   |
| 0x41                | TXMPATH   | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x42                | TXMPATL   | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x43                | TXMMSKH   | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x44                | TXMMSKL   | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x45                | TXMLOC    | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x47<br>...<br>0x48 | Reserved  |          |          |          |          |          |          |          |      |   |
| 0x49                | TXMDLY    | 15:8     | TXMDLYEN |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x4B<br>...<br>0x4F | Reserved  |          |          |          |          |          |          |          |      |   |
| 0x50                | RXMCTL    | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          | RXPMD ET |          |          |          |          |      |   |
| 0x51                | RXMPATH   | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x52                | RXMPATL   | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x53                | RXMMSKH   | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x54                | RXMMSKL   | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x55                | RXMLOC    | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x57<br>...<br>0x58 | Reserved  |          |          |          |          |          |          |          |      |   |
| 0x59                | RXMDLY    | 15:8     | RXMDLYEN |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x5B<br>...<br>0x5F | Reserved  |          |          |          |          |          |          |          |      |   |
| 0x60                | CBSSPTHH  | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x61                | CBSSPTHL  | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x62                | CBSSTTHH  | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x63                | CBSSTTHL  | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x64                | CBSSLPCTL | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x65                | CBSTPLMTH | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |
| 0x66                | CBSTPLMTL | 15:8     |          |          |          |          |          |          |      |   |
|                     |           | 7:0      |          |          |          |          |          |          |      |   |

.....continued

| Address | Name       | Bit Pos. | 7             | 6           | 5           | 4              | 3                | 2            | 1        | 0         |  |
|---------|------------|----------|---------------|-------------|-------------|----------------|------------------|--------------|----------|-----------|--|
| 0x67    | CBSBTLMTH  | 15:8     |               |             |             |                |                  |              |          |           |  |
|         |            | 7:0      |               |             |             |                | BOTLIMIT[19:16]  |              |          |           |  |
| 0x68    | CBSBTLMTL  | 15:8     |               |             |             |                | BOTLIMIT[15:8]   |              |          |           |  |
|         |            | 7:0      |               |             |             |                | BOTLIMIT[7:0]    |              |          |           |  |
| 0x69    | CBSCRCTRH  | 15:8     |               |             |             |                |                  |              |          |           |  |
|         |            | 7:0      |               |             |             |                | CREDITCTR[19:16] |              |          |           |  |
| 0x6A    | CBSCRCTRL  | 15:8     |               |             |             |                | CREDITCTR[15:8]  |              |          |           |  |
|         |            | 7:0      |               |             |             |                | CREDITCTR[7:0]   |              |          |           |  |
| 0x6B    | CBSCTRL    | 15:8     |               |             |             |                |                  |              |          | ECCRDS[7] |  |
|         |            | 7:0      | ECCRDS[6:0]   |             |             |                |                  |              |          | CBSEN     |  |
| 0x6D    | Reserved   |          |               |             |             |                |                  |              |          |           |  |
| 0x6F    |            |          |               |             |             |                |                  |              |          |           |  |
| 0x70    | PLCASKPCTL | 15:8     |               |             |             |                |                  |              |          |           |  |
|         |            | 7:0      |               |             |             |                |                  |              | TOSKPEN  |           |  |
| 0x71    | PLCATOSKP  | 15:8     |               |             |             |                |                  |              |          |           |  |
|         |            | 7:0      | TOSKPNUM[7:0] |             |             |                |                  |              |          |           |  |
| 0x73    | Reserved   |          |               |             |             |                |                  |              |          |           |  |
| 0x74    | ACMACTL    | 15:8     |               |             |             |                |                  |              |          |           |  |
|         |            | 7:0      |               |             |             |                |                  |              |          | ACMAEN    |  |
| 0x76    | Reserved   |          |               |             |             |                |                  |              |          |           |  |
| 0x7F    |            |          |               |             |             |                |                  |              |          |           |  |
| 0x80    | SLPCTL0    | 15:8     | SLPEN         | WKINEN      | MDIWKEN     | SLPINHDLY[1:0] |                  |              |          |           |  |
|         |            | 7:0      |               | SLPCAL[3:0] |             |                |                  |              |          |           |  |
| 0x81    | SLPCTL1    | 15:8     |               |             |             |                |                  |              |          |           |  |
|         |            | 7:0      | WOPOL         |             | WIPOL       | WAKEIND        | CLRWKI           | MWKFWD       | WKOFWDEN | MDIFWDEN  |  |
| 0x83    | Reserved   |          |               |             |             |                |                  |              |          |           |  |
| 0x86    |            |          |               |             |             |                |                  |              |          |           |  |
| 0x87    | CDCTL0     | 15:8     | CDEN          |             |             |                |                  |              |          |           |  |
|         |            | 7:0      |               |             |             |                |                  |              |          |           |  |
| 0x89    | Reserved   |          |               |             |             |                |                  |              |          |           |  |
| 0x9F    |            |          |               |             |             |                |                  |              |          |           |  |
| 0xA0    | SQICTL     | 15:8     | SQIRST        | SQIEN       |             |                |                  |              |          |           |  |
|         |            | 7:0      |               |             |             |                |                  |              |          |           |  |
| 0xA1    | SQISTS0    | 15:8     |               |             |             |                |                  |              |          |           |  |
|         |            | 7:0      | SQIERR        | SQIVLD      | SQIVAL[2:0] |                |                  | SQIERRC[2:0] |          |           |  |
| 0xA3    | Reserved   |          |               |             |             |                |                  |              |          |           |  |
| 0xA9    |            |          |               |             |             |                |                  |              |          |           |  |
| 0xAA    | SQICFG0    | 15:8     |               |             |             |                | TOID[7:4]        |              |          |           |  |
|         |            | 7:0      | TOID[3:0]     |             |             |                |                  |              |          |           |  |
| 0xAC    | Reserved   |          |               |             |             |                |                  |              |          |           |  |
| 0xD4    |            |          |               |             |             |                |                  |              |          |           |  |
| 0xD5    | ANALOG5    | 15:8     | UV33FTM[7:0]  |             |             |                |                  |              |          |           |  |
|         |            | 7:0      |               |             |             |                |                  |              |          |           |  |
| 0xD7    | Reserved   |          |               |             |             |                |                  |              |          |           |  |
| 0xC9FF  |            |          |               |             |             |                |                  |              |          |           |  |
| 0xCA00  | MIDVER     | 15:8     | IDM[7:0]      |             |             |                |                  |              |          |           |  |
|         |            | 7:0      | VER[7:0]      |             |             |                |                  |              |          |           |  |
| 0xCA01  | PLCA_CTRL0 | 15:8     | EN            | RST         |             |                |                  |              |          |           |  |
|         |            | 7:0      |               |             |             |                |                  |              |          |           |  |
| 0xCA02  | PLCA_CTRL1 | 15:8     | NCNT[7:0]     |             |             |                |                  |              |          |           |  |
|         |            | 7:0      | ID[7:0]       |             |             |                |                  |              |          |           |  |
| 0xCA03  | PLCA_STS   | 15:8     | PST           |             |             |                |                  |              |          |           |  |
|         |            | 7:0      |               |             |             |                |                  |              |          |           |  |

| .....continued |            |          |            |   |   |   |   |   |   |   |
|----------------|------------|----------|------------|---|---|---|---|---|---|---|
| Address        | Name       | Bit Pos. | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0xCA04         | PLCA_TOTMR | 15:8     |            |   |   |   |   |   |   |   |
|                |            | 7:0      | TOTMR[7:0] |   |   |   |   |   |   |   |
| 0xCA05         | PLCA_BURST | 15:8     | MAXBC[7:0] |   |   |   |   |   |   |   |
|                |            | 7:0      | BTMR[7:0]  |   |   |   |   |   |   |   |

## Related Links

[1.3. Register Bit Types](#)

### 11.5.1 Control 1 Register

**Name:** CTRL1  
**Address:** 0x0010

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |      |    |        |    |
|--------|----|----|----|----|------|----|--------|----|
| Bit    | 7  | 6  | 5  | 4  | 3    | 2  | 1      | 0  |
|        |    |    |    |    | IWDE |    | DIGLBE |    |
| Access | RO | RO | RO | RO | R/W  | RO | R/W    | RO |
| Reset  | 0  | 0  | 0  | 0  | 0    | 0  | 0      | 0  |

#### Bit 3 – IWDE Inactivity Watchdog Enable

When set, this bit enables the internal MII and PHY register access inactivity watchdog.

| Value | Description                  |
|-------|------------------------------|
| 0     | Inactivity watchdog disabled |
| 1     | Inactivity watchdog enabled  |

#### Bit 1 – DIGLBE Digital Loopback Enable

Enables a digital loopback from the differential Manchester encoder to the decoder.

| Value | Description              |
|-------|--------------------------|
| 0     | Normal operation         |
| 1     | Digital loopback enabled |

## 11.5.2 Status 1 Register

**Name:** STS1  
**Address:** 0x0018

|        |    |    |    |     |      |       |       |      |
|--------|----|----|----|-----|------|-------|-------|------|
| Bit    | 15 | 14 | 13 | 12  | 11   | 10    | 9     | 8    |
|        |    |    |    | SQI | PSTC | TXCOL | TXJAB | TSSI |
| Access | RO | RO | RO | RC  | RC   | RC    | RC    | RC   |
| Reset  | 0  | 0  | 0  | 0   | 0    | 0     | 0     | 0    |

|        |        |        |        |         |       |         |        |       |
|--------|--------|--------|--------|---------|-------|---------|--------|-------|
| Bit    | 7      | 6      | 5      | 4       | 3     | 2       | 1      | 0     |
|        | EMPCYC | RXINTO | UNEXPB | BCNBFTO | UNCRS | PLCASYM | ESDERR | DEC5B |
| Access | RC     | RC     | RC     | RC      | RC    | RC      | RC     | RC    |
| Reset  | 0      | 0      | 0      | 0       | 0     | 0       | 0      | 0     |

### Bit 12 – SQI Signal Quality Indication Status

This bit is set to indicate an SQI status change.

| Value | Description                 |
|-------|-----------------------------|
| 0     | SQI status has not changed. |
| 1     | SQI status has changed.     |

### Bit 11 – PSTC PLCA Status Changed

This bit is set to indicate that the PLCA Status (PST) bit has changed within the PLCA Status (PLCA\_STS) register.

| Value | Description                  |
|-------|------------------------------|
| 0     | PLCA Status has not changed. |
| 1     | PLCA Status has changed.     |

### Bit 10 – TXCOL Transmit Collision Status

Physical collision on the network was detected. This does not include logical collisions due to normal operation of PLCA.

| Value | Description                           |
|-------|---------------------------------------|
| 0     | No collision detected during transmit |
| 1     | Collision detected during transmit    |

### Bit 9 – TXJAB Transmit Jabber Status

This bit indicates the occurrence of a transmit jabber condition. A jabber condition occurs when the PHY detects that the PCS has remained in the transmit state longer than 2 ms. When a jabber condition is detected, the transmitter is disabled for the duration of 16 ms.

| Value | Description                 |
|-------|-----------------------------|
| 0     | No transmit jabber detected |
| 1     | Transmit jabber detected    |

### Bit 8 – TSSI Time Synchronization Service Interface Status

This bit is set when the TSSI has indicated the transmission or reception of an Ethernet packet.

| Value | Description                                        |
|-------|----------------------------------------------------|
| 0     | No transmitted or received frames indicated        |
| 1     | A transmitted or received frame has been indicated |

### Bit 7 – EMPCYC PLCA Empty Cycle Status

This bit indicates the detection of an empty PLCA bus cycle. An empty bus cycle occurs when the node detects no transmissions in any of the possible transmit opportunities between two successive BEACONS.

| Value | Description |
|-------|-------------|
|-------|-------------|



| Value | Description                               |
|-------|-------------------------------------------|
| 0     | An empty PLCA cycle has not been detected |
| 1     | An empty PLCA cycle has been detected     |

**Bit 6 – RXINTO** Receive in Transmit Opportunity

This bit indicates the detection of another node transmitting in this node's local assigned transmit opportunity. This could indicate multiple nodes being assigned the same Local ID.

| Value | Description                                                       |
|-------|-------------------------------------------------------------------|
| 0     | Another node has not been detected transmitting in this node's TO |
| 1     | Another node has been detected transmitting in this node's TO     |

**Bit 5 – UNEXPB** Unexpected BEACON Received

When configured as the PLCA coordinator in charge of transmitting the periodic coordinating BEACONS, this bit indicates the detection of an unexpected BEACON on the segment. This condition may be due to the configuration of multiple PLCA coordinators on the segment.

| Value | Description                                                             |
|-------|-------------------------------------------------------------------------|
| 0     | Another node on the segment has not been detected transmitting a BEACON |
| 1     | Another node on the segment has been detected transmitting a BEACON     |

**Bit 4 – BCNBFTO** BEACON Received Before Transmit Opportunity

This bit indicates the detection of a BEACON before the node's assigned transmit opportunity. This condition could indicate the configuration of multiple PLCA coordinators on the segment. Other conditions that may cause this to occur include a PLCA coordinator with an incorrectly configured maximum node count resulting in a PLCA cycle that is too short, or a PLCA Local ID that is configured beyond the PLCA cycle.

| Value | Description                                                      |
|-------|------------------------------------------------------------------|
| 0     | A BEACON has not been detected before local transmit opportunity |
| 1     | A BEACON was detected before local transmit opportunity          |

**Bit 3 – UNCRS** Unexpected Carrier Sense

When operating in ACMA mode, this bit will indicate carrier sense during this PHY's transmit slot when ACMA is asserted.

| Value | Description                                            |
|-------|--------------------------------------------------------|
| 0     | No Carrier has been sensed during PHY's ACMA time slot |
| 1     | Carrier has been sensed during PHY's ACMA time slot    |

**Bit 2 – PLCASYM** PLCA Symbols Detected

This bit indicates the detection of PLCA BEACON symbols when PLCA is not enabled. This condition may indicate the local node is operating with PLCA disabled on a segment with PLCA enabled nodes.

| Value | Description                                                                     |
|-------|---------------------------------------------------------------------------------|
| 0     | PLCA BEACON symbols have not been detected from the network with PLCA disabled  |
| 1     | PLCA BEACON symbols have been detected from the network with PLCA with disabled |

**Bit 1 – ESDERR** End-of-Stream Delimiter Error

This bit indicates the reception of an End-of-Stream Delimiter Error (ESDERR) or End-of-Stream Jabber (ESDJAB) symbol.

| Value | Description                     |
|-------|---------------------------------|
| 0     | ESD error has not been detected |
| 1     | ESD error has been detected     |

**Bit 0 – DEC5B** 5B Decode Error

This bit indicates the 5B decoder encountered an unknown or reserved 5B codeword that could not be decoded.

| Value | Description                       |
|-------|-----------------------------------|
| 0     | 5B decoder error has not occurred |

| Value | Description                  |
|-------|------------------------------|
| 1     | 5B decode error has occurred |

### 11.5.3 Status 2 Register

**Name:** STS2  
**Address:** 0x0019

|        |    |    |    |    |    |        |       |      |
|--------|----|----|----|----|----|--------|-------|------|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10     | 9     | 8    |
|        |    |    |    |    |    | WKEMDI | WKEWI | UV33 |
| Access | RO | RO | RO | RO | RO | RC     | RC    | RC   |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0      | 0     | 0    |

|        |    |    |       |    |    |    |    |    |
|--------|----|----|-------|----|----|----|----|----|
| Bit    | 7  | 6  | 5     | 4  | 3  | 2  | 1  | 0  |
|        |    | OT | IWDTO |    |    |    |    |    |
| Access | RO | RC | RC    | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0     | 0  | 0  | 0  | 0  | 0  |

#### Bit 10 – WKEMDI MDI Wake-up Status

This indicates wake-up from MDI energy.

| Value | Description                    |
|-------|--------------------------------|
| 0     | Wake from MDI has not occurred |
| 1     | Wake from MDI has occurred     |

#### Bit 9 – WKEWI WAKE\_IN Wake-up Status

This indicates wake-up from WAKE\_IN pin.

| Value | Description                        |
|-------|------------------------------------|
| 0     | Wake from WAKE_IN has not occurred |
| 1     | Wake from WAKE_IN has occurred     |

#### Bit 8 – UV33 3.3V supply Under-Voltage Status

Set when an under-voltage condition has been detected on the 3.3V supply.

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | 3.3V supply under-voltage condition has not been detected |
| 1     | 3.3V supply under-voltage condition has been detected     |

#### Bit 6 – OT Over-Temperature Error Status

| Value | Description                        |
|-------|------------------------------------|
| 0     | No over-temperature error detected |
| 1     | Over-temperature error detected    |

#### Bit 5 – IWDTO Inactivity Watchdog Timeout Status

This bit is set to indicate a timeout of the inactivity watchdog has occurred.

| Value | Description                               |
|-------|-------------------------------------------|
| 0     | Inactivity watchdog timer has not expired |
| 1     | Inactivity watchdog timer has expired     |

### 11.5.4 Status 3 Register

**Name:** STS3  
**Address:** 0x001A

|        |              |    |    |    |    |    |    |    |
|--------|--------------|----|----|----|----|----|----|----|
| Bit    | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |              |    |    |    |    |    |    |    |
| Access | RO           | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | ERRTOID[7:0] |    |    |    |    |    |    |    |
| Access | RO           | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

#### Bits 7:0 – ERRTOID[7:0] PLCA Error Transmit Opportunity ID

This field captures the local PLCA current transmit opportunity counter ID when any unmasked interrupt status bit in the Status 1 register is set.

**Note:** This field is only accurate if one unmasked interrupt status bit is set in the Status 1 register. If multiple interrupt status bits are set, then this field represents the transmit opportunity for only the most recent interrupt status bit.

### 11.5.5 Interrupt Mask 1 Register

**Name:** IMSK1  
**Address:** 0x001C

|        |     |     |     |      |       |        |        |       |
|--------|-----|-----|-----|------|-------|--------|--------|-------|
| Bit    | 15  | 14  | 13  | 12   | 11    | 10     | 9      | 8     |
|        |     |     |     | SQIM | PSTCM | TXCOLM | TXJABM | TSSIM |
| Access | R/W | R/W | R/W | R/W  | R/W   | R/W    | R/W    | R/W   |
| Reset  | 1   | 1   | 1   | 1    | 1     | 1      | 1      | 1     |

|        |         |         |         |          |        |          |         |        |
|--------|---------|---------|---------|----------|--------|----------|---------|--------|
| Bit    | 7       | 6       | 5       | 4        | 3      | 2        | 1       | 0      |
|        | EMPCYCM | RXINTOM | UNEXPBM | BCNBFTOM | UNCRSM | PLCASYMM | ESDERRM | DEC5BM |
| Access | R/W     | R/W     | R/W     | R/W      | R/W    | R/W      | R/W     | R/W    |
| Reset  | 1       | 1       | 1       | 1        | 1      | 1        | 1       | 1      |

**Bit 12 – SQIM** Signal Quality Indication Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the Signal Quality Indication (SQI) status bit is set.

| Value | Description                    |
|-------|--------------------------------|
| 0     | SQI status interrupt enabled.  |
| 1     | SQI status interrupt disabled. |

**Bit 11 – PSTCM** PLCA Status Changed Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the PLCA Status Changed (PSTC) status bit is set.

| Value | Description                            |
|-------|----------------------------------------|
| 0     | PLCA status change interrupt enabled.  |
| 1     | PLCA status change interrupt disabled. |

**Bit 10 – TXCOLM** Transmit Collision Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the Transmit Collision (TXCOL) status bit is set.

| Value | Description                           |
|-------|---------------------------------------|
| 0     | Transmit collision interrupt enabled  |
| 1     | Transmit collision interrupt disabled |

**Bit 9 – TXJABM** Transmit Jabber Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the Transmit Jabber (TXJAB) status bit is set.

| Value | Description                        |
|-------|------------------------------------|
| 0     | Transmit jabber interrupt enabled  |
| 1     | Transmit jabber interrupt disabled |

**Bit 8 – TSSIM** Time Synchronization Service Interface Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the Time Synchronization Service Interface (TSSI) status bit is set.

| Value | Description             |
|-------|-------------------------|
| 0     | TSSI interrupt enabled  |
| 1     | TSSI interrupt disabled |

**Bit 7 – EMPCYCM** PLCA Empty Cycle Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the PLCA Empty Cycle (EMPCYC) status bit is set.

| Value | Description                         |
|-------|-------------------------------------|
| 0     | PLCA empty cycle interrupt enabled  |
| 1     | PLCA empty cycle interrupt disabled |

**Bit 6 – RXINTOM** Receive in Transmit Opportunity Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the Receive in Transmit Opportunity (RXINTO) status bit is set.

| Value | Description                                        |
|-------|----------------------------------------------------|
| 0     | Receive in transmit opportunity interrupt enabled  |
| 1     | Receive in transmit opportunity interrupt disabled |

**Bit 5 – UNEXPBM** Unexpected BEACON Received Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the Unexpected BEACON Received (UNEXPB) status bit is set.

| Value | Description                                   |
|-------|-----------------------------------------------|
| 0     | Unexpected BEACON received interrupt enabled  |
| 1     | Unexpected BEACON received interrupt disabled |

**Bit 4 – BCNBFTOM** BEACON Received Before Transmit Opportunity Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the BEACON Received Before Transmit Opportunity (BCNBFTO) status bit is set.

| Value | Description                                                    |
|-------|----------------------------------------------------------------|
| 0     | BEACON received before transmit opportunity interrupt enabled  |
| 1     | BEACON received before transmit opportunity interrupt disabled |

**Bit 3 – UNCRSM** Unexpected Carrier Sense Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the Unexpected Carrier Sense (UNCRS) status bit is set.

| Value | Description                                 |
|-------|---------------------------------------------|
| 0     | Unexpected carrier sense interrupt enabled  |
| 1     | Unexpected carrier sense interrupt disabled |

**Bit 2 – PLCASYMM** PLCA Symbols Detected Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the PLCA Symbols Detected (PLCASYM) status bit is set.

| Value | Description                                     |
|-------|-------------------------------------------------|
| 0     | PLCA BEACON symbols detected interrupt enabled  |
| 1     | PLCA BEACON symbols detected interrupt disabled |

**Bit 1 – ESDERRM** End-of-Stream Delimiter Error Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the End-of-Stream Delimiter Error (ESDERR) status bit is set.

| Value | Description                  |
|-------|------------------------------|
| 0     | ESD error interrupt enabled  |
| 1     | ESD error interrupt disabled |

**Bit 0 – DEC5BM** 5B Decode Error Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the 5B Decoder Error (DEC5B) status is set.

| Value | Description                        |
|-------|------------------------------------|
| 0     | 5B decode error interrupt enabled  |
| 1     | 5B decode error interrupt disabled |

## 11.5.6 Interrupt Mask 2 Register

**Name:** IMSK2

**Address:** 0x001D

|        |     |     |     |     |     |         |        |       |
|--------|-----|-----|-----|-----|-----|---------|--------|-------|
| Bit    | 15  | 14  | 13  | 12  | 11  | 10      | 9      | 8     |
|        |     |     |     |     |     | WKEMDIM | WKEWIM | UV33M |
| Access | R/W | R/W | R/W | R/W | R/W | R/W     | R/W    | R/W   |
| Reset  | 1   | 1   | 1   | 1   | 0   | 0       | 0      | 1     |

|        |     |     |        |     |     |     |     |     |
|--------|-----|-----|--------|-----|-----|-----|-----|-----|
| Bit    | 7   | 6   | 5      | 4   | 3   | 2   | 1   | 0   |
|        |     | OTM | IWDTOM |     |     |     |     |     |
| Access | R/W | R/W | R/W    | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1   | 1   | 1      | 1   | 1   | 1   | 1   | 1   |

### Bit 10 – WKEMDIM MDI Wakeup Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the MDI Wake-up (WKEMDI) status bit is set.

| Value | Description                    |
|-------|--------------------------------|
| 0     | MDI wake-up interrupt enabled  |
| 1     | MDI wake-up interrupt disabled |

### Bit 9 – WKEWIM WAKE\_IN Wake-up Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the WAKE\_IN Wake-up (WKEWI) status bit is set.

| Value | Description                        |
|-------|------------------------------------|
| 0     | WAKE_IN wake-up interrupt enabled  |
| 1     | WAKE_IN wake-up interrupt disabled |

### Bit 8 – UV33M 3.3V supply Under-Voltage Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the 3.3V supply Under-Voltage (UV33) status bit is set.

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | 3.3V supply under-voltage interrupt enabled  |
| 1     | 1.8V supply under-voltage interrupt disabled |

### Bit 6 – OTM Over-Temperature Error Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the Over-Temperature Error (OT) status bit is set.

| Value | Description                               |
|-------|-------------------------------------------|
| 0     | Over-temperature error interrupt enabled  |
| 1     | Over-temperature error interrupt disabled |

### Bit 5 – IWDTOM Inactivity Watchdog Timeout Interrupt Mask

When clear, this bit will enable assertion of the PHY Interrupt status (PHYINT) in the OPEN Alliance Status 0 (OA\_STATUS0) register when the Inactivity Watchdog Timeout (IWDTO) status bit is set.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | Inactivity watchdog timeout interrupt enabled  |
| 1     | Inactivity watchdog timeout interrupt disabled |

### 11.5.7 Counter Control Register

**Name:** CTRCTRL

**Address:** 0x0020

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |     |        |         |
|--------|----|----|----|----|----|-----|--------|---------|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2   | 1      | 0       |
|        |    |    |    |    |    |     | TOCTRE | BCNCTRE |
| Access | RO | RO | RO | RO | RO | R/W | R/W    | R/W     |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0   | 0      | 0       |

**Bit 1 – TOCTRE** Transmit Opportunity Counter Enable

Enables and disables the PLCA transmit opportunity counter in the Transmit Opportunity Count (High) and Transmit Opportunity Count (Low) registers.

| Value | Description                                   |
|-------|-----------------------------------------------|
| 0     | PLCA transmit opportunity counter is disabled |
| 1     | PLCA transmit opportunity counter is enabled  |

**Bit 0 – BCNCTRE** PLCA BEACON Counter Enable

Enables and disables the PLCA BEACON counter in BEACON Count (High) and BEACON Count (Low) registers.

| Value | Description                     |
|-------|---------------------------------|
| 0     | PLCA BEACON counter is disabled |
| 1     | PLCA BEACON counter is enabled  |



### 11.5.8 Transmit Opportunity Count (High)

**Name:** TOCNTH

**Address:** 0x0024

|        |              |    |    |    |    |    |    |    |
|--------|--------------|----|----|----|----|----|----|----|
| Bit    | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TOCNT[31:24] |    |    |    |    |    |    |    |
| Access | RC           | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |              |    |    |    |    |    |    |    |
|--------|--------------|----|----|----|----|----|----|----|
| Bit    | 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TOCNT[23:16] |    |    |    |    |    |    |    |
| Access | RC           | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

#### Bits 15:0 – TOCNT[31:16] Transmit Opportunity Count

This field maintains the upper 16 bits of the 32-bit count of the number of PLCA transmit opportunities the device may have utilized since the previous read.

**Note:** When this register is read, the contents of the 32-bit transmit opportunity counter will be latched into the high and low counter register pair. The high counter register will be updated prior to be driven to the station management entity.

**Note:** The 32-bit counter will be reset when the contents are latched into the high and low counter register pair.

### 11.5.9 Transmit Opportunity Count (Low)

**Name:** TOCNTL

**Address:** 0x0025

|        |             |    |    |    |    |    |    |    |
|--------|-------------|----|----|----|----|----|----|----|
| Bit    | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | TOCNT[15:8] |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | TOCNT[7:0]  |    |    |    |    |    |    |    |
| Access | RC          | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 15:0 – TOCNT[15:0]** Transmit Opportunity Count

This field maintains the lower 16 bits of the 32-bit count of the number of PLCA transmit opportunities the device may have utilized since the previous read.

**Note:** The contents of this register will be latched upon reading of the Transmit Opportunity Count (High) register.

**11.5.10 BEACON Count (High)**

**Name:** BCNCNTH  
**Address:** 0x0026

|        |               |    |    |    |    |    |    |    |
|--------|---------------|----|----|----|----|----|----|----|
| Bit    | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | BCNCNT[31:24] |    |    |    |    |    |    |    |
| Access | RC            | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | BCNCNT[23:16] |    |    |    |    |    |    |    |
| Access | RC            | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 15:0 – BCNCNT[31:16] Beacon Count**

This field maintains the upper 16 bits of the 32-bit counter of PLCA beacons received or transmitted since the previous read.

**Note:** When this register is read, the contents of the 32-bit beacon counter will be latched into the high and low counter register pair. The high counter register will be updated prior to be driven to the station management entity.

**Note:** The 32-bit beacon counter will be reset when the contents are latched into the high and low counter register pair.

### 11.5.11 BEACON Count (Low)

**Name:** BCNCNTL  
**Address:** 0x0027

|        |              |    |    |    |    |    |    |    |
|--------|--------------|----|----|----|----|----|----|----|
| Bit    | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | BCNCNT[15:8] |    |    |    |    |    |    |    |
| Access | RC           | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | BCNCNT[7:0]  |    |    |    |    |    |    |    |
| Access | RC           | RC | RC | RC | RC | RC | RC | RC |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

#### Bits 15:0 – BCNCNT[15:0] Beacon Count

This field maintains the lower 16 bits of the 32-bit counter of PLCA beacons received or transmitted since the previous read.

**Note:** The contents of this register will be latched upon reading of the BEACON Count (High) register.

**11.5.12 PLCA Multiple ID 0 Register****Name:** MULTID0**Address:** 0x0030

|        |          |     |     |     |     |     |     |     |
|--------|----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15       | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ID1[7:0] |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7        | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ID2[7:0] |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:8 – ID1[7:0]**

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

| Value      | Description                                                |
|------------|------------------------------------------------------------|
| 0x00, 0xFF | Value ignored                                              |
| 0x01-0xFE  | Additional LocalID (transmit opportunity) assigned to node |

**Bits 7:0 – ID2[7:0]**

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

| Value      | Description                                                |
|------------|------------------------------------------------------------|
| 0x00, 0xFF | Value ignored                                              |
| 0x01-0xFE  | Additional LocalID (transmit opportunity) assigned to node |

**11.5.13 PLCA Multiple ID 1 Register****Name:** MULTID1**Address:** 0x0031

|        |          |     |     |     |     |     |     |     |
|--------|----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15       | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ID3[7:0] |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7        | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ID4[7:0] |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:8 – ID3[7:0]**

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

| Value      | Description                                                |
|------------|------------------------------------------------------------|
| 0x00, 0xFF | Value ignored                                              |
| 0x01-0xFE  | Additional LocalID (transmit opportunity) assigned to node |

**Bits 7:0 – ID4[7:0]**

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

| Value      | Description                                                |
|------------|------------------------------------------------------------|
| 0x00, 0xFF | Value ignored                                              |
| 0x01-0xFE  | Additional LocalID (transmit opportunity) assigned to node |

**11.5.14 PLCA Multiple ID 2 Register****Name:** MULTID2**Address:** 0x0032

|        |          |     |     |     |     |     |     |     |
|--------|----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15       | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ID5[7:0] |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7        | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ID6[7:0] |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:8 – ID5[7:0]**

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

| Value      | Description                                                |
|------------|------------------------------------------------------------|
| 0x00, 0xFF | Value ignored                                              |
| 0x01-0xFE  | Additional LocalID (transmit opportunity) assigned to node |

**Bits 7:0 – ID6[7:0]**

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

| Value      | Description                                                |
|------------|------------------------------------------------------------|
| 0x00, 0xFF | Value ignored                                              |
| 0x01-0xFE  | Additional LocalID (transmit opportunity) assigned to node |

**11.5.15 PLCA Multiple ID 3 Register****Name:** MULTID3**Address:** 0x0033

|        |          |     |     |     |     |     |     |     |
|--------|----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15       | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | ID7[7:0] |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7        | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ID8[7:0] |     |     |     |     |     |     |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:8 – ID7[7:0]**

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

| Value      | Description                                                |
|------------|------------------------------------------------------------|
| 0x00, 0xFF | Value ignored                                              |
| 0x01-0xFE  | Additional LocalID (transmit opportunity) assigned to node |

**Bits 7:0 – ID8[7:0]**

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

| Value      | Description                                                |
|------------|------------------------------------------------------------|
| 0x00, 0xFF | Value ignored                                              |
| 0x01-0xFE  | Additional LocalID (transmit opportunity) assigned to node |



## 11.5.16 PLCA Reconciliation Sublayer Status

**Name:** PRSSTS

**Address:** 0x0036

|        |            |    |    |    |    |    |    |    |
|--------|------------|----|----|----|----|----|----|----|
| Bit    | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | MAXID[7:0] |    |    |    |    |    |    |    |
| Access | RO         | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

### Bits 15:8 – MAXID[7:0] Maximum ID

This field contains the maximum PLCA transmit opportunity ID count in the previous PLCA bus cycle. By monitoring this field, the PLCA follower station applications may detect the number of transmit opportunities the PLCA coordinator allows between BEACONS.

## 11.5.17 Port Management 2

**Name:** PRTMGMT2**Address:** 0x003D

|        |    |    |          |         |          |    |    |    |
|--------|----|----|----------|---------|----------|----|----|----|
| Bit    | 15 | 14 | 13       | 12      | 11       | 10 | 9  | 8  |
|        |    |    | MIRXWDEN | PRIWDEN | MITXWDEN |    |    |    |
| Access | RO | RO | R/W      | R/W     | R/W      | RO | RO | RO |
| Reset  | 0  | 0  | 1        | 0       | 1        | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bit 13 – MIRXWDEN** Media Interface Receive Watchdog Enable

When set, packets received from the network and output through the internal MII to the MAC and SPI will reset the inactivity watchdog timer.

| Value | Description                                          |
|-------|------------------------------------------------------|
| 0     | Media interface receive inactivity watchdog disabled |
| 1     | Media interface receive watchdog enabled             |

**Bit 12 – PRIWDEN** PHY Register Inactivity Watchdog Enable

When set, PHY register accesses by the SPI host will reset the inactivity watchdog timer.

| Value | Description                                      |
|-------|--------------------------------------------------|
| 0     | PHY register access inactivity watchdog disabled |
| 1     | PHY register access inactivity watchdog enabled  |

**Bit 11 – MITXWDEN** Media Interface Transmit Watchdog Enable

When set, packets received from the SPI and MAC through the internal MII and output on the network will reset the inactivity watchdog timer.

| Value | Description                                           |
|-------|-------------------------------------------------------|
| 0     | Media interface transmit inactivity watchdog disabled |
| 1     | Media interface transmit inactivity watchdog enabled  |

### 11.5.18 Inactivity Watchdog Timeout (High)

**Name:** IWDTOH

**Address:** 0x003E

|        |                |     |     |     |     |     |     |     |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15             | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TIMEOUT[31:24] |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7              | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TIMEOUT[23:16] |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1              | 0   | 0   | 1   | 1   | 0   | 0   | 0   |

**Bits 15:0 – TIMEOUT[31:16]** Inactivity Watchdog Timeout

This field configures the upper 16 bits of the 32-bit integrated PHY/MAC MII and PHY register access inactivity watchdog timeout in increments of 200 ns.

**Note:** The default value of 0x00989680 results in a timeout of 2 seconds.

### 11.5.19 Inactivity Watchdog Timeout (Low)

**Name:** IWDTOL

**Address:** 0x003F

|        |               |     |     |     |     |     |     |     |
|--------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15            | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TIMEOUT[15:8] |     |     |     |     |     |     |     |
| Access | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1             | 0   | 0   | 1   | 0   | 1   | 1   | 0   |
| Bit    | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TIMEOUT[7:0]  |     |     |     |     |     |     |     |
| Access | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:0 – TIMEOUT[15:0]** Inactivity Watchdog Timeout

This field configures the lower 16 bits of the 32-bit integrated PHY/MAC MII and PHY register access inactivity watchdog timeout in increments of 200 ns.

**Note:** The default value of 0x00989680 results in a timeout of 2 seconds.

## 11.5.20 Transmit Match Control Register

**Name:** TXMCTL**Address:** 0x0040

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |         |     |     |     |     |          |      |     |
|--------|---------|-----|-----|-----|-----|----------|------|-----|
| Bit    | 7       | 6   | 5   | 4   | 3   | 2        | 1    | 0   |
| Access | TXPMDET |     |     |     |     | MACTXTSE | TXME |     |
| Reset  | RC      | R/W | R/W | R/W | R/W | R/W      | R/W  | R/W |
|        | 0       | 0   | 0   | 0   | 0   | 0        | 0    | 0   |

### Bit 7 – TXPMDET Transmit Packet Match Detected

| Value | Description                                |
|-------|--------------------------------------------|
| 0     | A matching packet has not been transmitted |
| 1     | A matching packet has been transmitted     |

### Bit 2 – MACTXTSE MAC Transmit Time Stamp Enable

When enabled, transmitted packets will be compared. When a match is detected, a logical collision will be asserted to the MAC delaying transmission until the next PLCA transmit opportunity.

**Note:** This bit cannot be enabled at the same time as the [TXME](#) bit.

| Value | Description                                                                                                            |
|-------|------------------------------------------------------------------------------------------------------------------------|
| 0     | Transmit MAC gPTP disabled. Normal operation.                                                                          |
| 1     | Transmit MAC gPTP enabled. Matching transmit packets will delay transmission until the next PLCA transmit opportunity. |

### Bit 1 – TXME Transmit Match Enable

When enabled, transmit packets will be compared. When a match is detected, the TXPI pin will be asserted as configured.

**Note:** This bit cannot be enabled at the same time as the [MACTXTSE](#) bit.

| Value | Description                                                        |
|-------|--------------------------------------------------------------------|
| 0     | Transmitted packets are not compared. Normal operation.            |
| 1     | Transmitted packets will be compared and TXPI asserted on a match. |

## 11.5.21 Transmit Match Pattern (High) Register

**Name:** TXMPATH

**Address:** 0x0041

|        |               |     |     |     |     |     |     |     |
|--------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15            | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        |               |     |     |     |     |     |     |     |
| Access | RO            | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TXMPAT[23:16] |     |     |     |     |     |     |     |
| Access | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1             | 0   | 0   | 0   | 1   | 0   | 0   | 0   |

**Bits 7:0 – TXMPAT[23:16]** Transmit Match Pattern (High)  
Upper 8 bits of the 24-bit transmit match pattern.

## 11.5.22 Transmit Match Pattern (Low) Register

**Name:** TXMPATL  
**Address:** 0x0042

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TXMPAT[15:8] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1            | 1   | 1   | 1   | 0   | 1   | 1   | 1   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TXMPAT[7:0]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 1   | 0   | 0   | 0   | 0   |

**Bits 15:0 – TXMPAT[15:0]** Transmit Match Pattern (Low)  
Lower 16 bits of the 24-bit transmit match pattern.

**11.5.23 Transmit Match Mask (High) Register****Name:** TXMMSKH**Address:** 0x0043

|        |               |     |     |     |     |     |     |     |
|--------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15            | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| Access | RO            | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TXMMSK[23:16] |     |     |     |     |     |     |     |
| Access | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 7:0 – TXMMSK[23:16] Transmit Match Mask (High)**

Upper 8 bits of the 24-bit transmit match mask. A '1' in any bit will cause the corresponding bit in the Transmit Match Pattern field to be ignored. A '0' will cause the corresponding bit in the Transmit Match Pattern field to be compared.

**Note:** Triggering of transmit packets matching at the Start-of-Frame Delimiter (SFD) requires that all bits within the Transmit Match Pattern field be disabled from the compare by writing the Transmit Match Mask registers to 0xFFFFFFFF. Additionally, the Transmit Match Location must be configured to 0x0000.



**11.5.24 Transmit Match Mask (Low) Register****Name:** TXMMSKL**Address:** 0x0044

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TXMMSK[15:8] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TXMMSK[7:0]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:0 – TXMMSK[15:0] Transmit Match Mask (Low)**

Lower 16 bits of the 24-bit transmit match mask. A '1' in any bit will cause the corresponding bit in the Transmit Match Pattern field to be ignored. A '0' will cause the corresponding bit in the Transmit Match Pattern field to be compared.

**Note:** Triggering of transmit packets matching at the Start-of-Frame Delimiter (SFD) requires that all bits within the Transmit Match Pattern field be disabled from the compare by writing the Transmit Match Mask registers to 0xFFFFFFFF. Additionally, the Transmit Match Location must be configured to 0x0000.

### 11.5.25 Transmit Match Location Register

**Name:** TXMLOC**Address:** 0x0045

|        |     |     |     |     |     |     |     |     |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

|        |     |     |                 |     |     |     |     |     |
|--------|-----|-----|-----------------|-----|-----|-----|-----|-----|
| Bit    | 7   | 6   | 5               | 4   | 3   | 2   | 1   | 0   |
|        |     |     | TXLOCATION[5:0] |     |     |     |     |     |
| Access | R/W | R/W | R/W             | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0   | 0               | 1   | 1   | 1   | 1   | 0   |

**Bits 5:0 – TXLOCATION[5:0]** Transmit Match Location

Location in nibbles within the Ethernet packet relative to, but not including, the Start-of-Frame Delimiter (SFD) at which the pattern matcher will activate. The six previous transmitted nibbles relative to (but not including) the transmit match location nibble will be compared. Valid range is from 0x00 to 0x3D.

**Note:** Triggering of transmit packets matching at the Start-of-Frame Delimiter (SFD) requires that the Transmit Match Location be configured to 0x00. Additionally, all bits within the Transmit Match Pattern field must be disabled from the compare by writing the Transmit Match Mask registers to 0xFFFFFFFF.

## 11.5.26 Transmit Matched Packet Delay Register

**Name:** TXMDLY**Address:** 0x0049

|        |                |    |    |    |    |                 |    |    |
|--------|----------------|----|----|----|----|-----------------|----|----|
| Bit    | 15             | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
|        | TXMDLYEN       |    |    |    |    | TXMPKTDLY[10:8] |    |    |
| Access | R/W            | RO | RO | RO | RO | RO              | RO | RO |
| Reset  | 0              | 0  | 0  | 0  | 0  | 0               | 0  | 0  |
| Bit    | 7              | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
|        | TXMPKTDLY[7:0] |    |    |    |    |                 |    |    |
| Access | RO             | RO | RO | RO | RO | RO              | RO | RO |
| Reset  | 0              | 0  | 0  | 0  | 0  | 0               | 0  | 0  |

**Bit 15 – TXMDLYEN** Transmit Matched Packet Delay Measurement Enable

When set, this bit enables the measurement of matched transmit packet delays through the PHY.

| Value | Description                                   |
|-------|-----------------------------------------------|
| 0     | Transmit packet delay measurement is disabled |
| 1     | Transmit packet delay measurement is enabled  |

**Bits 10:0 – TXMPKTDLY[10:0]** Transmit Matched Packet Delay

This field contains the delay of the previously matched transmit packet through the PHY. The delay is measured from the assertion of TXEN to the end of the transmission of the first SSD symbol ('H') of the packet preamble onto the line units of 40 ns. When PLCA is enabled, the measured delay includes the delay of the packet through the PLCA elastic buffer.

| Value | Description    |
|-------|----------------|
| 0x000 | 0 ns           |
| 0x001 | 40 ns          |
| ...   | ...            |
| 0x7FF | 81.880 $\mu$ s |

### 11.5.27 Receive Match Control Register

**Name:** RXMCTL**Address:** 0x0050

|        |    |    |    |    |    |    |    |     |
|--------|----|----|----|----|----|----|----|-----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
|        |    |    |    |    |    |    |    |     |
| Access | RO | RO | RO | RO | RO | RO | RO | R/W |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0   |

|        |     |          |     |     |     |     |      |     |
|--------|-----|----------|-----|-----|-----|-----|------|-----|
| Bit    | 7   | 6        | 5   | 4   | 3   | 2   | 1    | 0   |
|        |     | RXPMDDET |     |     |     |     | RXME |     |
| Access | R/W | RC       | R/W | R/W | R/W | R/W | R/W  | R/W |
| Reset  | 0   | 0        | 0   | 0   | 0   | 0   | 0    | 0   |

**Bit 6 – RXPMDDET** Receive Packet Match Detected

| Value | Description                             |
|-------|-----------------------------------------|
| 0     | A matching packet has not been received |
| 1     | A matching packet has been received     |

**Bit 1 – RXME** Receive Packet Match Enable

When enabled, receive packets will be compared. When a match is detected, RXPI pin will be asserted as configured.

| Value | Description                                                     |
|-------|-----------------------------------------------------------------|
| 0     | Received packets are not compared. Normal operation.            |
| 1     | Received packets will be compared and RXPI asserted on a match. |

## 11.5.28 Receive Match Pattern (High) Register

**Name:** RXMPATH

**Address:** 0x0051

|        |               |     |     |     |     |     |     |     |
|--------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15            | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        |               |     |     |     |     |     |     |     |
| Access | RO            | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | RXMPAT[23:16] |     |     |     |     |     |     |     |
| Access | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1             | 0   | 0   | 0   | 1   | 0   | 0   | 0   |

**Bits 7:0 – RXMPAT[23:16]** Receive Match Pattern (High)  
Upper 8 bits of the 24-bit receive match pattern.

## 11.5.29 Receive Match Pattern (Low) Register

**Name:** RXMPATL  
**Address:** 0x0052

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | RXMPAT[15:8] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1            | 1   | 1   | 1   | 0   | 1   | 1   | 1   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | RXMPAT[7:0]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 1   | 0   | 0   | 0   | 0   |

**Bits 15:0 – RXMPAT[15:0]** Receive Match Pattern (Low)  
Lower 16 bits of the 24-bit receive match pattern.

**11.5.30 Receive Match Mask (High) Register****Name:** RXMMSKH**Address:** 0x0053

|        |               |     |     |     |     |     |     |     |
|--------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15            | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| Access | RO            | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | RXMMSK[23:16] |     |     |     |     |     |     |     |
| Access | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 7:0 – RXMMSK[23:16] Receive Match Mask (High)**

Upper 8 bits of the 24-bit receive match mask. A '1' in any bit will cause the corresponding bit in the Receive Match Pattern field to be ignored. A '0' will cause the corresponding bit in the Receive Match Pattern field to be compared.

**Note:** Triggering of receive packets matching at the Start-of-Frame Delimiter (SFD) requires that all bits within the Receive Match Pattern field be disabled from the compare by writing the Receive Match Mask registers to 0xFFFFFFFF. Additionally, the Receive Match Location must be configured to 0x0000.

**11.5.31 Receive Match Mask (Low) Register****Name:** RXMMSKL**Address:** 0x0054

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | RXMMSK[15:8] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | RXMMSK[7:0]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:0 – RXMMSK[15:0] Receive Match Mask (Low)**

Lower 16 bits of the 24-bit receive match mask. A '1' in any bit will cause the corresponding bit in the Receive Match Pattern field to be ignored. A '0' will cause the corresponding bit in the Receive Match Pattern field to be compared.

**Note:** Triggering of receive packets matching at the Start-of-Frame Delimiter (SFD) requires that all bits within the Receive Match Pattern field be disabled from the compare by writing the Receive Match Mask registers to 0xFFFFFFFF. Additionally, the Receive Match Location must be configured to 0x0000.



**11.5.32 Receive Match Location Register****Name:** RXMLOC**Address:** 0x0055

|        |     |     |     |     |     |     |     |     |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0   | 0   | 1   | 1   | 1   | 1   | 0   |

**Bits 5:0 – RXLOCATION[5:0] Receive Match Location**

Location in nibbles within the Ethernet packet relative to, but not including, the Start-of-Frame Delimiter (SFD) at which the pattern matcher will activate. The six previous received nibbles relative to (but not including) the receive match location nibble will be compared. Valid range is from 0x00 to 0x3D.

**Note:** Triggering of receive packets matching at the Start-of-Frame Delimiter (SFD) requires that the Receive Match Location be configured to 0x00. Additionally, all bits within the Receive Match Pattern field must be disabled from the compare by writing the Receive Match Mask registers to 0xFFFFF.

**11.5.33 Receive Matched Packet Delay Register****Name:** RXMDLY**Address:** 0x0059

|        |                |    |    |    |    |                 |    |    |
|--------|----------------|----|----|----|----|-----------------|----|----|
| Bit    | 15             | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
|        | RXMDLYEN       |    |    |    |    | RXMPKTDLY[10:8] |    |    |
| Access | R/W            | RO | RO | RO | RO | RO              | RO | RO |
| Reset  | 0              | 0  | 0  | 0  | 0  | 0               | 0  | 0  |
| Bit    | 7              | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
|        | RXMPKTDLY[7:0] |    |    |    |    |                 |    |    |
| Access | RO             | RO | RO | RO | RO | RO              | RO | RO |
| Reset  | 0              | 0  | 0  | 0  | 0  | 0               | 0  | 0  |

**Bit 15 – RXMDLYEN** Receive Matched Packet Delay Measurement Enable

When set, this bit enables the measurement of matched receive packet delays through the PHY.

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | Receive packet delay measurement is disabled |
| 1     | Receive packet delay measurement is enabled  |

**Bits 10:0 – RXMPKTDLY[10:0]** Receive Matched Packet Delay

This field contains the delay of the previously matched receive packet through the PHY. The delay is measured from detection of the first SSD symbol ("H") of the packet preamble on the line to the assertion of Receive Data Valid at the media interface. The delay in this field is represented in units of 10 ns with an uncertainty of 10 ns.

| Value | Description    |
|-------|----------------|
| 0x000 | 0 ns           |
| 0x001 | 10 ns          |
| 0x010 | 20 ns          |
| ...   | ...            |
| 0x7FF | 20.470 $\mu$ s |

### 11.5.34 Credit Based Shaper Stop Threshold (High) Register

**Name:** CBSSPTHH

**Address:** 0x0060

|        |    |    |    |    |                |     |     |     |
|--------|----|----|----|----|----------------|-----|-----|-----|
| Bit    | 15 | 14 | 13 | 12 | 11             | 10  | 9   | 8   |
|        |    |    |    |    |                |     |     |     |
| Access | RO | RO | RO | RO | RO             | RO  | RO  | RO  |
| Reset  | 0  | 0  | 0  | 0  | 0              | 0   | 0   | 0   |
| Bit    | 7  | 6  | 5  | 4  | 3              | 2   | 1   | 0   |
|        |    |    |    |    | STOPTHR[19:16] |     |     |     |
| Access | RO | RO | RO | RO | R/W            | R/W | R/W | R/W |
| Reset  | 0  | 0  | 0  | 0  | 0              | 0   | 0   | 0   |

**Bits 3:0 – STOPTHR[19:16] Stop Threshold (High)**

Upper 4 bits of the 20-bit credit stop threshold value. Once the credit counter drops below this threshold the device will assert CRS to hold off the MAC from transmitting.

### 11.5.35 Credit Based Shaper Stop Threshold (Low) Register

**Name:** CBSSPHTL

**Address:** 0x0061

|        |               |     |     |     |     |     |     |     |
|--------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15            | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STOPTHR[15:8] |     |     |     |     |     |     |     |
| Access | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1             | 0   | 1   | 1   | 0   | 0   | 1   | 1   |
| Bit    | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STOPTHR[7:0]  |     |     |     |     |     |     |     |
| Access | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1             | 0   | 0   | 0   | 1   | 0   | 0   | 0   |

**Bits 15:0 – STOPTHR[15:0] Stop Threshold (Low)**

Lower 16 bits of the 20-bit credit stop threshold value. Once the credit counter drops below this threshold the device will assert CRS to hold off the MAC from transmitting.

### 11.5.36 Credit Based Shaper Start Threshold (High) Register

**Name:** CBSSTTHH

**Address:** 0x0062

|        |    |    |    |    |                 |     |     |     |
|--------|----|----|----|----|-----------------|-----|-----|-----|
| Bit    | 15 | 14 | 13 | 12 | 11              | 10  | 9   | 8   |
|        |    |    |    |    |                 |     |     |     |
| Access | RO | RO | RO | RO | RO              | RO  | RO  | RO  |
| Reset  | 0  | 0  | 0  | 0  | 0               | 0   | 0   | 0   |
| Bit    | 7  | 6  | 5  | 4  | 3               | 2   | 1   | 0   |
|        |    |    |    |    | STARTTHR[19:16] |     |     |     |
| Access | RO | RO | RO | RO | R/W             | R/W | R/W | R/W |
| Reset  | 0  | 0  | 0  | 0  | 0               | 0   | 0   | 0   |

**Bits 3:0 – STARTTHR[19:16] Start Threshold (High)**

Upper 4 bits of the 20-bit credit start threshold value. Once the credit counter accumulates above this threshold the device will negate CRS to allow the MAC to transmit.

**11.5.37 Credit Based Shaper Start Threshold (Low) Register****Name:** CBSSTTHL**Address:** 0x0063

|        |                |     |     |     |     |     |     |     |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15             | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STARTTHR[15:8] |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1              | 0   | 1   | 1   | 0   | 0   | 1   | 1   |
| Bit    | 7              | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STARTTHR[7:0]  |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1              | 0   | 0   | 0   | 1   | 0   | 0   | 0   |

**Bits 15:0 – STARTTHR[15:0] Start Threshold (Low)**

Lower 16 bits of the 20-bit credit start threshold value. Once the credit counter accumulates above this threshold the device will negate CRS to allow the MAC to transmit.

**11.5.38 Credit Based Shaper Slope Control Register****Name:** CBSSLPCTL**Address:** 0x0064

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | FALLSLP[7:0] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 1   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | RISESLP[7:0] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 1   | 1   | 1   | 1   | 0   |

**Bits 15:8 – FALLSLP[7:0]** Falling Slope

Sets the rate at which credits are reduced when transmitting. Each time the PHY transmits the number of bytes configured by this parameter, the credit count will be decremented by one, until the bottom limit is reached.

**Bits 7:0 – RISESLP[7:0]** Rising Slope

Sets the rate at which credits are increased when receiving or idle. The PHY will count the number of received bytes or 800 ms periods of idle time. When the receive/idle byte count reaches the value in this parameter, the receive/idle byte count will be reset to 0 and the credit count will be incremented by one, until the top limit is reached.

### 11.5.39 Credit Based Shaper Top Limit (High) Register

**Name:**     CBSTPLMTH

**Address:**  0x0065

|        |    |    |    |    |                 |     |     |     |
|--------|----|----|----|----|-----------------|-----|-----|-----|
| Bit    | 15 | 14 | 13 | 12 | 11              | 10  | 9   | 8   |
|        |    |    |    |    |                 |     |     |     |
| Access | RO | RO | RO | RO | RO              | RO  | RO  | RO  |
| Reset  | 0  | 0  | 0  | 0  | 0               | 0   | 0   | 0   |
| Bit    | 7  | 6  | 5  | 4  | 3               | 2   | 1   | 0   |
|        |    |    |    |    | TOPLIMIT[19:16] |     |     |     |
| Access | RO | RO | RO | RO | R/W             | R/W | R/W | R/W |
| Reset  | 0  | 0  | 0  | 0  | 0               | 0   | 0   | 1   |

**Bits 3:0 – TOPLIMIT[19:16] Credit Top Limit (High)**

Upper 4 bits of the 20-bit credit top limit threshold value. The credit counter will saturate at this value once it has been incremented to this limit.



### 11.5.40 Credit Based Shaper Top Limit (Low) Register

**Name:**     CBSTPLMTL

**Address:**  0x0066

|        |                |     |     |     |     |     |     |     |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15             | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | TOPLIMIT[15:8] |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0              | 1   | 1   | 0   | 0   | 1   | 1   | 1   |
| Bit    | 7              | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TOPLIMIT[7:0]  |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0   | 0   | 1   | 0   | 0   | 0   | 0   |

**Bits 15:0 – TOPLIMIT[15:0] Credit Top Limit (Low)**

Lower 16 bits of the 20-bit credit top limit threshold value. The credit counter will saturate at this value once it has incremented to this limit.

### 11.5.41 Credit Based Shaper Bottom Limit (High) Register

**Name:** CBSBTLMT

**Address:** 0x0067

|        |    |    |    |    |                 |     |     |     |
|--------|----|----|----|----|-----------------|-----|-----|-----|
| Bit    | 15 | 14 | 13 | 12 | 11              | 10  | 9   | 8   |
|        |    |    |    |    |                 |     |     |     |
| Access | RO | RO | RO | RO | RO              | RO  | RO  | RO  |
| Reset  | 0  | 0  | 0  | 0  | 0               | 0   | 0   | 0   |
| Bit    | 7  | 6  | 5  | 4  | 3               | 2   | 1   | 0   |
|        |    |    |    |    | BOTLIMIT[19:16] |     |     |     |
| Access | RO | RO | RO | RO | R/W             | R/W | R/W | R/W |
| Reset  | 0  | 0  | 0  | 0  | 0               | 0   | 0   | 0   |

**Bits 3:0 – BOTLIMIT[19:16]** Credit Bottom Limit (High)

Upper 4 bits of the 20-bit credit bottom limit threshold value. The credit counter will saturate at this value once it has been decremented to this limit.

## 11.5.42 Credit Based Shaper Bottom Limit (Low) Register

**Name:** CBSBTLMTL

**Address:** 0x0068

|        |                |     |     |     |     |     |     |     |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15             | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | BOTLIMIT[15:8] |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7              | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | BOTLIMIT[7:0]  |     |     |     |     |     |     |     |
| Access | R/W            | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

### Bits 15:0 – BOTLIMIT[15:0] Credit Bottom Limit (Low)

Lower 16 bits of the 20-bit credit bottom limit threshold value. The credit counter will saturate at this value once it has been decremented to this limit.

### 11.5.43 Credit Based Shaper Credit Counter (High) Register

**Name:** CBSCRCTRH

**Address:** 0x0069

|        |    |    |    |    |                  |    |    |    |
|--------|----|----|----|----|------------------|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
|        |    |    |    |    |                  |    |    |    |
| Access | RO | RO | RO | RO | RO               | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0                | 0  | 0  | 0  |
| Bit    | 7  | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
|        |    |    |    |    | CREDITCTR[19:16] |    |    |    |
| Access | RO | RO | RO | RO | RO               | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0                | 0  | 0  | 0  |

**Bits 3:0 – CREDITCTR[19:16]** Credit Counter (High)  
Upper 4 bits of the 20-bit credit counter.

## 11.5.44 Credit Based Shaper Credit Counter (Low) Register

**Name:** CBSCRCTRL

**Address:** 0x006A

|        |                 |    |    |    |    |    |    |    |
|--------|-----------------|----|----|----|----|----|----|----|
| Bit    | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | CREDITCTR[15:8] |    |    |    |    |    |    |    |
| Access | RO              | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | CREDITCTR[7:0]  |    |    |    |    |    |    |    |
| Access | RO              | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 15:0 – CREDITCTR[15:0]** Credit Counter (Low)  
Lower 16 bits of the 20-bit credit counter.

### 11.5.45 Credit Based Shaper Control Register

**Name:** CBSCTRL**Address:** 0x006B

|        |    |    |    |    |    |    |     |           |
|--------|----|----|----|----|----|----|-----|-----------|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9   | 8         |
|        |    |    |    |    |    |    |     | ECCRDS[7] |
| Access | RO | RO | RO | RO | RO | RO | R/W | R/W       |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 1   | 0         |

|        |             |     |     |     |     |     |     |       |
|--------|-------------|-----|-----|-----|-----|-----|-----|-------|
| Bit    | 7           | 6   | 5   | 4   | 3   | 2   | 1   | 0     |
|        | ECCRDS[6:0] |     |     |     |     |     |     | CBSEN |
| Access | R/W         | R/W | R/W | R/W | R/W | R/W | R/W | R/W   |
| Reset  | 0           | 0   | 1   | 1   | 1   | 1   | 0   | 0     |

**Bits 8:1 – ECCRDS[7:0]** Empty Cycle Credits

Sets the number of additional credits added on detection of an empty PLCA bus cycle.

**Bit 0 – CBSEN** Credit Based Shaper Enable

| Value | Description                                       |
|-------|---------------------------------------------------|
| 0     | Hardware credit based traffic shaping is disabled |
| 1     | Hardware credit based traffic shaping is enabled  |

**11.5.46 PLCA Skip Control Register****Name:** PLCASKPCTL**Address:** 0x0070

|        |    |    |    |    |    |    |         |    |
|--------|----|----|----|----|----|----|---------|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9       | 8  |
| Access | RO | RO | RO | RO | RO | RO | RO      | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0  |
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1       | 0  |
| Access | RO | RO | RO | RO | RO | RO | TOSKPEN |    |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0  |

**Bit 1 – TOSKPEN** PLCA Transmit Opportunity Skip Enable

When enabled, the device will assert CRS for a number of its assigned PLCA transmit opportunities after transmitting a packet to delay the MAC from transmitting another packet. The number of transmit opportunities skipped before allowing the MAC to transmit is configured in the PLCA Cycle Skip register.

| Value | Description                                |
|-------|--------------------------------------------|
| 0     | Transmit opportunity skipping is disabled. |
| 1     | Transmit opportunity skipping is enabled.  |

## 11.5.47 PLCA Transmit Opportunity Skip Register

**Name:** PLCATOSKP

**Address:** 0x0071

|        |               |     |     |     |     |     |     |     |
|--------|---------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15            | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| Access | RO            | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TOSKPNUM[7:0] |     |     |     |     |     |     |     |
| Access | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 7:0 – TOSKPNUM[7:0]** Transmit Opportunity Skip Number

Configures the number of assigned transmit opportunities to skip after transmitting a packet.



## 11.5.48 Application Controlled Media Access Control Register

**Name:** ACMACTL  
**Address:** 0x0074

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |     |    |        |
|--------|----|----|----|----|----|-----|----|--------|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2   | 1  | 0      |
| Access | RO | RO | RO | RO | RO | R/W | RC | ACMAEN |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0   | 0  | 0      |

### Bit 0 – ACMAEN ACMA Enable

When enabled, the PHY will only allow the MAC to transmit a packet when the ACMA pin is asserted.

| Value | Description                 |
|-------|-----------------------------|
| 0     | ACMA operation is disabled. |
| 1     | ACMA operation is enabled.  |

**11.5.49 Sleep Control 0 Register****Name:** SLPCTL0**Address:** 0x0080

|        |       |        |         |                |     |     |     |     |
|--------|-------|--------|---------|----------------|-----|-----|-----|-----|
| Bit    | 15    | 14     | 13      | 12             | 11  | 10  | 9   | 8   |
|        | SLPEN | WKINEN | MDIWKEN | SLPINHDLY[1:0] |     |     |     |     |
| Access | R/W   | R/W    | R/W     | R/W            | R/W | R/W | R/W | R/W |
| Reset  | 0     | 0      | 0       | 0              | 0   | 0   | 0   | 1   |

|        |     |             |     |     |     |     |     |     |
|--------|-----|-------------|-----|-----|-----|-----|-----|-----|
| Bit    | 7   | 6           | 5   | 4   | 3   | 2   | 1   | 0   |
|        |     | SLPCAL[3:0] |     |     |     |     |     |     |
| Access | R/W | R/W         | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0           | 0   | 0   | 0   | 0   | 0   | 0   |

**Bit 15 – SLPEN** Sleep Enable

When set, the device stops driving the INH pin high, releasing it to high-impedance, and enters deep sleep mode. When released, if no other device is driving the INH electrical node, an external resistor will pull the node low disabling system switched power supplies.

| Value | Description      |
|-------|------------------|
| 0     | Normal operation |
| 1     | Sleep            |

**Bit 14 – WKINEN** WAKE\_IN Wake-up Enable

When set, enables wake-up from sleep mode upon detection of a pulse on the WAKE\_IN pin.

| Value | Description                               |
|-------|-------------------------------------------|
| 0     | Disable wake-up by input pulse on WAKE_IN |
| 1     | Enable wake-up by input pulse on WAKE_IN  |

**Bit 13 – MDIWKEN** MDI Wake-up Enable

When set, enables wake-up from sleep mode upon detection of activity at the MDI.

| Value | Description                                 |
|-------|---------------------------------------------|
| 0     | Disable wake-up from MDI activity detection |
| 1     | Enable wake-up from MDI activity detection  |

**Bits 12:11 – SLPINHDLY[1:0]** Sleep Inhibit Delay

This field configures the delay from when sleep is first commanded to when the power supply Inhibit (INH) pin becomes high-impedance and the sleep state is entered. This delay is used to allow all nodes on a mixing segment time to go quiet before powering down.

| Value | Description  |
|-------|--------------|
| 00    | 0 ms delay   |
| 01    | 50 ms delay  |
| 10    | 100 ms delay |
| 11    | 200 ms delay |

**Bits 6:3 – SLPCAL[3:0]** Sleep Calibration

Factory use only. Must always be written as 0000.

| Value  | Description                          |
|--------|--------------------------------------|
| 0000   | Only valid value for write           |
| Others | Invalid on write.<br>Ignore on read. |

### 11.5.50 Sleep Control 1 Register

**Name:** SLPCTL1**Address:** 0x0081

| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|--------|----|----|----|----|----|----|----|----|
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit    | 7     | 6   | 5     | 4       | 3      | 2      | 1        | 0        |
|--------|-------|-----|-------|---------|--------|--------|----------|----------|
|        | WOPOL |     | WIPOL | WAKEIND | CLRWKI | MWKFWD | WKOFWDEN | MDIFWDEN |
| Access | R/W   | R/W | R/W   | RO      | R/W    | R/W SC | R/W      | R/W      |
| Reset  | 0     | 0   | 0     | 0       | 0      | 0      | 0        | 0        |

**Bit 7 – WOPOL** WAKE\_OUT Polarity

This bit configures the polarity of the 90  $\mu$ s output wake pulse generated on the WAKE\_OUT pin.

**Note:** Only wake from HIGH pulses on WAKE\_OUT is supported.



**Restriction:** While this bit defaults to '0', it must always be written to '1' when writing to other bits in this register.

| Value | Description                                                  |
|-------|--------------------------------------------------------------|
| 0     | Reserved                                                     |
| 1     | Device will output an active HIGH pulse on the WAKE_OUT pin. |

**Bit 5 – WIPOL** WAKE\_IN Polarity

This bit configures the polarity of the pulse on the WAKE\_IN pin that will wake the device from sleep.

| Value | Description                                                |
|-------|------------------------------------------------------------|
| 0     | Device will wake from an active LOW pulse on WAKE_IN pin.  |
| 1     | Device will wake from an active HIGH pulse on WAKE_IN pin. |

**Bit 4 – WAKEIND** Wake Indication

This bit indicates a wake-up event when set.

**Note:** This bit is cleared by writing a '1' followed by a '0' to the Clear Wake Indication (CLRWKI) bit.

| Value | Description                         |
|-------|-------------------------------------|
| 0     | Wake-up from sleep has not occurred |
| 1     | Wake-up from sleep has occurred     |

**Bit 3 – CLRWKI** Clear Wake Indication

Writing a '1' to this bit will cause the Wake Indication (WAKEIND) status bit to be cleared.

**Note:** Once the device has been awoken, the station controller must write this bit to '1' then '0' to clear the wake activity status and re-enable the ability to be awoken again.

| Value | Description                  |
|-------|------------------------------|
| 0     | Normal operation             |
| 1     | Clear wake activity detector |

**Bit 2 – MWKFWD** Manual Wake Forward

When set, this bit will trigger a wake forwarding event. The device will generate a wake-up pulse on WAKE\_OUT if forwarding of wake events to WAKE\_OUT is enabled by WAKE\_OUT Forward Enable (WKOFWDEN) bit. Wake activity signaling will be generated to the MDI if forwarding of wake events to MDI is enabled by MDI Wake Forward Enable (MDIFWDEN) bit.

**Note:** This bit is self-cleared by hardware once the wake output events have completed.

| Value | Description                                        |
|-------|----------------------------------------------------|
| 0     | No wake out signaling (normal operation)           |
| 1     | Generate wake out signaling to WAKE_OUT and/or MDI |

**Bit 1 – WKOFWDEN** WAKE\_OUT Forward Enable

Enable the generation of a WAKE\_OUT pulse when a wake indication is detected by MDI activity or assertion of the WAKE\_IN pin.

| Value | Description                                          |
|-------|------------------------------------------------------|
| 0     | Disable generation of a pulse on WAKE_OUT on wake-up |
| 1     | Enable generation of a pulse on WAKE_OUT on wake-up  |

**Bit 0 – MDIFWDEN** MDI Forward Enable

This bit will enable the generation of activity signaling on the MDI when a wake indication is detected by the assertion of the WAKE\_IN pin.

| Value | Description                                                     |
|-------|-----------------------------------------------------------------|
| 0     | Disable generation MDI wake signaling upon wake-up from WAKE_IN |
| 1     | Enable generation MDI wake signaling upon wake-up from WAKE_IN  |

### 11.5.51 Collision Detector Control 0 Register

**Name:** CDCTL0

**Address:** 0x0087

|        |      |     |     |     |    |    |    |     |
|--------|------|-----|-----|-----|----|----|----|-----|
| Bit    | 15   | 14  | 13  | 12  | 11 | 10 | 9  | 8   |
|        | CDEN |     |     |     |    |    |    |     |
| Access | R/W  | R/W | R/W | R/W | RO | RO | RO | R/W |
| Reset  | 1    | 0   | 0   | 0   | 0  | 0  | 0  | 0   |

|        |     |     |     |     |     |     |     |     |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        |     |     |     |     |     |     |     |     |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1   | 0   | 0   | 0   | 0   | 0   | 1   | 1   |

#### Bit 15 – CDEN Collision Detect Enable

When set, this bit enables the detection of collisions on the physical medium when transmitting.



**Tip:** No physical collisions will occur when all nodes in a mixing segment are properly configured for PLCA operation. As a result, for improved performance in high noise environments where false collisions may be detected leading to dropped packets, it is recommended that the user write this bit to a '0' to disable collision detection when PLCA is enabled. When collision detection is disabled, the PLCA reconciliation sublayer will still assert *logical collisions* to the MAC as part of normal operation.



**CAUTION** When writing to this bit, use a read-modify-write operation to avoid accidental modifications to reserved fields.

| Value | Description                              |
|-------|------------------------------------------|
| 0     | Collision detection is disabled          |
| 1     | Collision detection is enabled (default) |

## 11.5.52 SQI Control Register

**Name:** SQICTL

**Address:** 0x00A0

| Bit    | 15     | 14    | 13  | 12  | 11  | 10  | 9   | 8   |
|--------|--------|-------|-----|-----|-----|-----|-----|-----|
|        | SQIRST | SQIEN |     |     |     |     |     |     |
| Access | R/W SC | R/W   | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0      | 0     | 0   | 1   | 0   | 1   | 0   | 0   |

| Bit    | 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|--------|-----|----|----|----|----|----|----|----|
|        |     |    |    |    |    |    |    |    |
| Access | R/W | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

### Bit 15 – SQIRST SQI Reset

Setting this bit will reset the SQI block. This bit is self-clearing.

| Value | Description        |
|-------|--------------------|
| 0     | Normal Operation   |
| 1     | SQI block is reset |

### Bit 14 – SQIEN SQI Enable

This bit enables the SQI measurement process when set.

| Value | Description     |
|-------|-----------------|
| 0     | SQI is disabled |
| 1     | SQI is enabled  |

**11.5.53 SQI Status 0 Register**

**Name:** SQISTS0  
**Address:** 0x00A1

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |        |        |             |    |    |              |    |    |
|--------|--------|--------|-------------|----|----|--------------|----|----|
| Bit    | 7      | 6      | 5           | 4  | 3  | 2            | 1  | 0  |
|        | SQIERR | SQIVLD | SQIVAL[2:0] |    |    | SQIERRC[2:0] |    |    |
| Access | RO     | RC     | RO          | RO | RO | RO           | RO | RO |
| Reset  | 0      | 0      | 0           | 0  | 0  | 0            | 0  | 0  |

**Bit 7 – SQIERR SQI ERR**

This bit will be set when an error has occurred during the SQI statistic accumulation period.

| Value | Description                                    |
|-------|------------------------------------------------|
| 0     | No error detected during SQI measurement       |
| 1     | Error has been detected during SQI measurement |

**Bit 6 – SQIVLD SQI Valid**

This bit is set when the SQI measurement is valid and may be read from [SQIVAL](#).

| Value | Description                             |
|-------|-----------------------------------------|
| 0     | SQI estimation is not complete or valid |
| 1     | SQI estimation is complete and valid    |

**Bits 5:3 – SQIVAL[2:0] SQI Value**

This field contains the measured SQI Value.

| Value | Description                                                            |
|-------|------------------------------------------------------------------------|
| 000   | SNR $\leq$ ~5 dB (Worst SQI)<br>BER $\geq$ ~3.8E-02                    |
| 001   | ~5 dB $\leq$ SNR $\leq$ ~10 dB<br>~3.8E-02 $\geq$ BER $\geq$ ~7.8E-4   |
| 010   | ~10 dB $\leq$ SNR $\leq$ ~12 dB<br>~7.8E-4 $\geq$ BER $\geq$ ~3.4E-5   |
| 011   | ~12 dB $\leq$ SNR $\leq$ ~14 dB<br>~3.4E-5 $\geq$ BER $\geq$ ~2.7E-7   |
| 100   | ~14 dB $\leq$ SNR $\leq$ ~16 dB<br>~2.7E-7 $\geq$ BER $\geq$ ~1.4E-10  |
| 101   | ~16 dB $\leq$ SNR $\leq$ ~17 dB<br>~1.4E-10 $\geq$ BER $\geq$ ~7.2E-13 |
| 110   | ~17 dB $\leq$ SNR $\leq$ ~18 dB<br>~7.2E-13 $\geq$ BER $\geq$ ~9.9E-16 |
| 111   | SNR $\geq$ ~18 dB (Best SQI)<br>BER $\leq$ ~9.9E-16                    |

**Bits 2:0 – SQIERRC[2:0] SQI Error Code**

This field returns the SQI Error code when the [SQIERR](#) bit is set indicating an error condition occurred during the SQI statistic accumulation period.

| Value | Description       |
|-------|-------------------|
| 000   | No error / events |

| Value  | Description                         |
|--------|-------------------------------------|
| 001    | Low threshold > Maximum limitation  |
| 010    | High threshold > Maximum limitation |
| 011    | Low threshold < Minimum limitation  |
| 100    | High threshold < Minimum limitation |
| 101    | Low threshold > High threshold      |
| Others | Undefined                           |



## 11.5.54 SQI Configuration 0 Register

**Name:** SQICFG0

**Address:** 0x00AA

|        |           |     |     |     |           |     |     |     |
|--------|-----------|-----|-----|-----|-----------|-----|-----|-----|
| Bit    | 15        | 14  | 13  | 12  | 11        | 10  | 9   | 8   |
|        |           |     |     |     | TOID[7:4] |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W       | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0         | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3         | 2   | 1   | 0   |
|        | TOID[3:0] |     |     |     |           |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W       | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 1         | 1   | 1   | 1   |

### Bits 11:4 – TOID[7:0] Transmit Opportunity ID

This field configures the PLCA transmit opportunity ID for which to measure the SQI. This is used to measure the SQI for a specific node on a PLCA enabled segment. A value of 0xFF will result in the SQI being measured over packets received from all nodes.

**11.5.55 Analog Control 5****Name:** ANALOG5**Address:** 0x00D5

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | UV33FTM[7:0] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 1   | 0   | 1   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        |              |     |     |     |     |     |     |     |
| Access | RO           | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:8 – UV33FTM[7:0] Voltage Ready Time**

This field configures the 3.3V VDDA and VDDAU supply under-voltage filter in increments of 10  $\mu$ s. The voltage must fall below the under-voltage threshold for longer than the time configured in this field before the 3.3V under-voltage condition will be triggered.

| Value | Description           |
|-------|-----------------------|
| 00h   | 0 $\mu$ s             |
| 01h   | 10 $\mu$ s            |
| 02h   | 20 $\mu$ s            |
| ...   | ...                   |
| 14h   | 200 $\mu$ s (default) |
| ...   | ...                   |
| FFh   | 2.55 ms               |

**11.5.56 OPEN Alliance Map ID and Version Register**

**Name:** MIDVER  
**Address:** 0xCA00

|        |          |    |    |    |    |    |    |    |
|--------|----------|----|----|----|----|----|----|----|
| Bit    | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | IDM[7:0] |    |    |    |    |    |    |    |
| Access | RO       | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0        | 0  | 0  | 0  | 1  | 0  | 1  | 0  |
| Bit    | 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | VER[7:0] |    |    |    |    |    |    |    |
| Access | RO       | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0        | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

**Bits 15:8 – IDM[7:0] Register Map ID**

This field uniquely identifies the OPEN Alliance address space for register mapping.

| Value | Description                |
|-------|----------------------------|
| 0x0A  | OPEN Alliance register map |

**Bits 7:0 – VER[7:0] Register Map Version**

This field specifies the register map version. The version number is represented in binary-coded-decimal.



**Tip:** This device conforms to the OPEN Alliance register map version 1.1 although this field indicates conformity to version 1.0. The only difference between the two register map specifications is the default value of the Transmit Opportunity Timer (TOTMR) bit field. Version 1.0 of the register map specifies a default TOTMR value of 24 whereas this device implements a default TOTMR value of 32 conforming to Clause 30 of the IEEE 802.3 specification. This discontinuity was resolved with OPEN Alliance register map version 1.1.

| Value | Description                            |
|-------|----------------------------------------|
| 0x10  | OPEN Alliance register map version 1.0 |

**11.5.57 PLCA Control 0 Register****Name:** PLCA\_CTRL0**Address:** 0xCA01

|        |     |        |    |    |    |    |    |    |
|--------|-----|--------|----|----|----|----|----|----|
| Bit    | 15  | 14     | 13 | 12 | 11 | 10 | 9  | 8  |
|        | EN  | RST    |    |    |    |    |    |    |
| Access | R/W | R/W SC | RO | RO | RO | RO | RO | RO |
| Reset  | 0   | 0      | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bit 15 – EN** PLCA Enable

Setting this bit will enable Physical Layer Collision Avoidance. When this bit is clear, the PHY will operate in pure CSMA/CD mode.

**Note:** When PLCA is enabled on a properly configured mixing segment, no collisions should occur on the physical layer. It is therefore recommended to disable physical layer collision detection to achieve a higher level of noise tolerance.

| Value | Description                                                                                                                            |
|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 0     | The PLCA reconciliation sublayer is disabled and the PHY operates in normal CSMA/CD mode without the performance enhancements of PLCA. |
| 1     | The Physical Layer Collision Avoidance (PLCA) reconciliation sublayer functionality is enabled.                                        |

**Bit 14 – RST** PLCA Reset

Writing '1' to this bit will result in a reset of the PLCA reconciliation sublayer.

**Note:** This bit is self-clearing. When setting this bit, do not set other bits in this register.

| Value | Description                           |
|-------|---------------------------------------|
| 0     | Normal operation                      |
| 1     | PLCA reconciliation sublayer is reset |

### 11.5.58 PLCA Control 1 Register

**Name:** PLCA\_CTRL1**Address:** 0xCA02

|        |           |     |     |     |     |     |     |     |
|--------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | NCNT[7:0] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 1   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | ID[7:0]   |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1         | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

**Bits 15:8 – NCNT[7:0] Node Count**

This field configures the maximum number of nodes supported on the multidrop network. Proper operation requires that this field be set to at least the number of nodes that may exist on the network. The number of transmit opportunities in a given PLCA cycle.

Valid range: 0x01-0xFF

**Note:** This field must be configured correctly on the node with ID=0.

**Bits 7:0 – ID[7:0] PLCA Local ID**

This field configures the node's PLCA Local ID and the transmit opportunity within the PLCA cycle which it will transmit. A value of zero configures the node as the PLCA coordinator responsible for the periodic transmission of the PLCA BEACON and the number of transmit opportunities available per PLCA bus cycle. When set to 0xFF, the PLCA operation will be disabled and the node will revert to CSMA/CD.

Up to eight additional transmit opportunities may be configured in the PLCA Multiple ID 0-3 (MULTID0-MULTID3) registers.

**Note:** This parameter shall be configured unique across the multidrop network to ensure proper collision-free operation.

| Value  | Description                    |
|--------|--------------------------------|
| 0      | PLCA Coordinator node Local ID |
| 1-0xFE | PLCA Follower node Local ID    |
| 0xFF   | PLCA Disabled                  |

**Related Links**

[11.5.12. MULTID0](#)

[11.5.13. MULTID1](#)

[11.5.14. MULTID2](#)

[11.5.15. MULTID3](#)

### 11.5.59 PLCA Status Register

**Name:** PLCA\_STS

**Address:** 0xCA03

|        |     |    |    |    |    |    |    |    |
|--------|-----|----|----|----|----|----|----|----|
| Bit    | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | PST |    |    |    |    |    |    |    |
| Access | RO  | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

#### Bit 15 – PST PLCA Status

This field indicates that the PLCA reconciliation sublayer is active and a BEACON is being regularly transmitted or received.

| Value | Description                                                                            |
|-------|----------------------------------------------------------------------------------------|
| 0     | The PLCA reconciliation sublayer is not regularly receiving or transmitting the BEACON |
| 1     | The PLCA reconciliation sublayer is regularly receiving or transmitting the BEACON     |

**11.5.60 PLCA Transmit Opportunity Timer Register****Name:** PLCA\_TOTMR**Address:** 0xCA04

|        |            |     |     |     |     |     |     |     |
|--------|------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15         | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| Access | RO         | RO  | RO  | RO  | RO  | RO  | RO  | RO  |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | TOTMR[7:0] |     |     |     |     |     |     |     |
| Access | R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 1   | 0   | 0   | 0   | 0   | 0   |

**Bits 7:0 – TOTMR[7:0] PLCA Transmit Opportunity Timer**

Configures the PLCA Transmit Opportunity time allowed for each node to begin transmitting and capture the carrier sense for all nodes on the network. The time is represented in increments of 100 ns (i.e., 1 BT). This field defaults to 32 bit times (3.2  $\mu$ s) according to the IEEE 802.3cg specification (Clause 30), and the *OPEN Alliance 10BASE-T1S PLCA Management Registers* specification Version 1.2.



**Important:** This field must be configured identically across all nodes on the multidrop mixing segment.



Improper configuration of Transmit Opportunity timer may result in reduced network performance or collisions. Determination of the optimal Transmit Opportunity time requires knowledge of various delays of each of the vendor PHYs on the mixing segment and various physical layer propagation delay. It is recommended to leave this field at its default value unless a full evaluation of delays has been performed.

**Note:** Due to discrepancies in the default value for this register between Version 1.0 of the OPEN Alliance register map specification for this field and Clause 30 of the IEEE 802.3cg specification, it is recommended that this field always be configured to the desired value for all Microchip and non-Microchip devices on the network.

**11.5.61 PLCA Burst Mode Register****Name:** PLCA\_BURST**Address:** 0xCA05

|        |            |     |     |     |     |     |     |     |
|--------|------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 15         | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | MAXBC[7:0] |     |     |     |     |     |     |     |
| Access | R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | BTMR[7:0]  |     |     |     |     |     |     |     |
| Access | R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 1          | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:8 – MAXBC[7:0] Maximum Burst Count**

This field configures the maximum number of additional frames that the node may transmit in a single transmit opportunity. When set to 0, the PLCA burst mode is disabled and only one frame will be transmitted per transmit opportunity.

| Value  | Description                                                                       |
|--------|-----------------------------------------------------------------------------------|
| 0      | Burst mode disabled. Only one frame will be transmitted per Transmit Opportunity. |
| 1-0xFF | Number of additional frames that may be transmitted in a burst.                   |

**Bits 7:0 – BTMR[7:0] Burst Timer**

When burst mode is enabled, this field configures the amount of time allowed following the transmission of a frame which the node will continue to transmit and hold the multidrop network waiting for the MAC to transmit an additional frame. Should the timer expire before the MAC transmits an additional frame, or if the maximum number of frames allowed to be transmitted in a single burst has been exceeded, the node will stop transmitting and yield the network to the next transmit opportunity.

The time is represented in increments of 100 ns (i.e., 1 BT).

**Note:** The minimum value should be equal to the MAC inter-frame gap (IFG) plus margin for the latency between the MAC and PHY.



## 11.6 Miscellaneous Register Descriptions

The section describes the various miscellaneous registers. These registers are located within Memory Map Selector 10 (MMS 10).



RESERVED address space must not be written except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Refer to the Register Bit Types section for details on register bit attribute notation.

| Address             | Name     | Bit Pos. | 7            | 6          | 5           | 4         | 3            | 2             | 1            | 0         |          |         |
|---------------------|----------|----------|--------------|------------|-------------|-----------|--------------|---------------|--------------|-----------|----------|---------|
| 0x00<br>...<br>0x80 | Reserved |          |              |            |             |           |              |               |              |           |          |         |
| 0x81                | QTXCFG   | 31:24    | CTTHR[1:0]   |            |             |           |              |               |              |           |          |         |
|                     |          | 23:16    |              | BUFSZ[2:0] |             | MACFCSDIS |              |               |              |           |          |         |
|                     |          | 15:8     |              |            |             |           |              |               |              |           |          |         |
|                     |          | 7:0      |              |            |             |           |              |               |              |           |          |         |
| 0x82                | QRXCFG   | 31:24    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 23:16    |              | BUFSZ[2:0] |             |           |              |               |              |           |          |         |
|                     |          | 15:8     |              |            |             |           |              |               |              |           |          |         |
|                     |          | 7:0      |              |            |             |           |              |               |              |           |          |         |
| 0x86<br>...<br>0x88 | Reserved |          |              |            |             |           |              |               |              |           |          |         |
| 0x89                | CLKOCTL  | 31:24    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 23:16    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 15:8     |              |            |             |           |              |               |              |           |          |         |
|                     |          | 7:0      |              |            |             | CLKOEN    |              |               | CLKOSEL[1:0] |           |          |         |
| 0x8C                | MISC     | 31:24    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 23:16    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 15:8     |              |            |             | UV18FEN   |              | UV18FTM[11:8] |              |           |          |         |
|                     |          | 7:0      | UV18FTM[7:0] |            |             |           |              |               |              |           |          |         |
| 0x90<br>...<br>0x93 | Reserved |          |              |            |             |           |              |               |              |           |          |         |
| 0x94                | DEVID    | 31:24    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 23:16    |              |            |             |           | MODEL[15:12] |               |              |           |          |         |
|                     |          | 15:8     | MODEL[11:4]  |            |             |           | MODEL[3:0]   |               |              |           |          |         |
|                     |          | 7:0      | MODEL[3:0]   |            |             |           | REV[3:0]     |               |              |           |          |         |
| 0x96                | BUSPCS   | 31:24    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 23:16    |              |            |             |           | MBMPER       |               | SPIPER       |           | CSRBPER  | SRAMPER |
|                     |          | 15:8     |              |            |             |           |              |               |              |           |          |         |
|                     |          | 7:0      |              |            |             | CSRBDPERG |              | SRAMDPERI     | MBMDPERI     | BMGRAPERI | PARGCEN  |         |
| 0x99                | CFGPRCTL | 31:24    | KEY2         | KEY1       |             |           |              |               |              |           |          |         |
|                     |          | 23:16    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 15:8     |              |            |             |           |              |               |              |           |          |         |
|                     |          | 7:0      |              |            |             |           |              |               |              |           | WREN     |         |
| 0x9D<br>...<br>0xFF | Reserved |          |              |            |             |           |              |               |              |           |          |         |
| 0x0100              | ECCCTRL  | 31:24    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 23:16    |              |            |             |           |              |               | DECDIS       |           | ENCDIS   |         |
|                     |          | 15:8     | SBERLMT[7:0] |            |             |           |              |               |              |           |          |         |
|                     |          | 7:0      |              |            |             |           |              | ERONESHT      |              | ERCLR     | BERCNTEN |         |
| 0x0101              | ECCSTS   | 31:24    |              |            |             |           |              |               |              |           |          |         |
|                     |          | 23:16    | ERSTS[1:0]   |            | ERRSYN[5:0] |           |              |               |              |           |          |         |
|                     |          | 15:8     | DBERCNT[7:0] |            |             |           |              |               |              |           |          |         |
|                     |          | 7:0      | SBERCNT[7:0] |            |             |           |              |               |              |           |          |         |

.....continued

| Address                 | Name       | Bit Pos. | 7               | 6          | 5               | 4               | 3     | 2           | 1  | 0       |
|-------------------------|------------|----------|-----------------|------------|-----------------|-----------------|-------|-------------|----|---------|
| 0x0102                  | ECCFLTCTRL | 31:24    |                 |            |                 | FLTINJADR[12:8] |       |             |    |         |
|                         |            | 23:16    | FLTINJADR[7:0]  |            |                 |                 |       |             |    |         |
|                         |            | 15:8     |                 | FLTINJONCE | FLTINJBIT2[5:0] |                 |       |             |    |         |
|                         |            | 7:0      | FLTINJAEQ       | FLTINJEN   | FLTINJBIT1[5:0] |                 |       |             |    |         |
| 0x0106<br>...<br>0x01FF | Reserved   |          |                 |            |                 |                 |       |             |    |         |
| 0x0200                  | EC0CTRL    | 31:24    |                 |            |                 |                 |       |             |    |         |
|                         |            | 23:16    |                 |            |                 |                 |       |             |    |         |
|                         |            | 15:8     |                 | MAX[3:0]   |                 |                 |       |             |    | EDGE[1] |
|                         |            | 7:0      | EDGE[0]         | SRC[2:0]   |                 |                 | CLR   |             | DA | EN      |
| 0x0201                  | EC1CTRL    | 31:24    |                 |            |                 |                 |       |             |    |         |
|                         |            | 23:16    |                 |            |                 |                 |       |             |    |         |
|                         |            | 15:8     |                 | MAX[3:0]   |                 |                 |       |             |    | EDGE[1] |
|                         |            | 7:0      | EDGE[0]         | SRC[2:0]   |                 |                 | CLR   |             | DA | EN      |
| 0x0202                  | EC2CTRL    | 31:24    |                 |            |                 |                 |       |             |    |         |
|                         |            | 23:16    |                 |            |                 |                 |       |             |    |         |
|                         |            | 15:8     |                 | MAX[3:0]   |                 |                 |       |             |    | EDGE[1] |
|                         |            | 7:0      | EDGE[0]         | SRC[2:0]   |                 |                 | CLR   |             | DA | EN      |
| 0x0203                  | EC3CTRL    | 31:24    |                 |            |                 |                 |       |             |    |         |
|                         |            | 23:16    |                 |            |                 |                 |       |             |    |         |
|                         |            | 15:8     |                 | MAX[3:0]   |                 |                 |       |             |    | EDGE[1] |
|                         |            | 7:0      | EDGE[0]         | SRC[2:0]   |                 |                 | CLR   |             | DA | EN      |
| 0x0204                  | ECRDSTS    | 31:24    |                 |            | EC3OV           | EC2OV           | EC1OV | EC0OV       |    |         |
|                         |            | 23:16    |                 |            |                 |                 |       |             |    |         |
|                         |            | 15:8     | EC3CT[3:0]      |            |                 |                 |       | EC2CT[3:0]  |    |         |
|                         |            | 7:0      | EC1CT[3:0]      |            |                 |                 |       | EC0CT[3:0]  |    |         |
| 0x0205                  | ECTOT      | 31:24    | EC3TOT[7:0]     |            |                 |                 |       | EC2TOT[7:0] |    |         |
|                         |            | 23:16    | EC2TOT[7:0]     |            |                 |                 |       | EC1TOT[7:0] |    |         |
|                         |            | 15:8     | EC1TOT[7:0]     |            |                 |                 |       | EC0TOT[7:0] |    |         |
|                         |            | 7:0      | EC0TOT[7:0]     |            |                 |                 |       |             |    |         |
| 0x0206                  | ECCLKSH    | 31:24    |                 |            |                 |                 |       |             |    |         |
|                         |            | 23:16    |                 |            |                 |                 |       |             |    |         |
|                         |            | 15:8     | CLKSEC[47:40]   |            |                 |                 |       |             |    |         |
|                         |            | 7:0      | CLKSEC[39:32]   |            |                 |                 |       |             |    |         |
| 0x0207                  | ECCLKSL    | 31:24    | CLKSEC[31:24]   |            |                 |                 |       |             |    |         |
|                         |            | 23:16    | CLKSEC[23:16]   |            |                 |                 |       |             |    |         |
|                         |            | 15:8     | CLKSEC[15:8]    |            |                 |                 |       |             |    |         |
|                         |            | 7:0      | CLKSEC[7:0]     |            |                 |                 |       |             |    |         |
| 0x0208                  | ECCLKNS    | 31:24    |                 |            |                 | CLOCK_NS[29:24] |       |             |    |         |
|                         |            | 23:16    | CLOCK_NS[23:16] |            |                 |                 |       |             |    |         |
|                         |            | 15:8     | CLOCK_NS[15:8]  |            |                 |                 |       |             |    |         |
|                         |            | 7:0      | CLOCK_NS[7:0]   |            |                 |                 |       |             |    |         |
| 0x0209                  | ECRDTS0    | 31:24    | TSSEC[1:0]      |            |                 | TSNS[29:24]     |       |             |    |         |
|                         |            | 23:16    | TSNS[23:16]     |            |                 |                 |       |             |    |         |
|                         |            | 15:8     | TSNS[15:8]      |            |                 |                 |       |             |    |         |
|                         |            | 7:0      | TSNS[7:0]       |            |                 |                 |       |             |    |         |
| 0x020A                  | ECRDTS1    | 31:24    | TSSEC[1:0]      |            |                 | TSNS[29:24]     |       |             |    |         |
|                         |            | 23:16    | TSNS[23:16]     |            |                 |                 |       |             |    |         |
|                         |            | 15:8     | TSNS[15:8]      |            |                 |                 |       |             |    |         |
|                         |            | 7:0      | TSNS[7:0]       |            |                 |                 |       |             |    |         |
| 0x020B                  | ECRDTS2    | 31:24    | TSSEC[1:0]      |            |                 | TSNS[29:24]     |       |             |    |         |
|                         |            | 23:16    | TSNS[23:16]     |            |                 |                 |       |             |    |         |
|                         |            | 15:8     | TSNS[15:8]      |            |                 |                 |       |             |    |         |
|                         |            | 7:0      | TSNS[7:0]       |            |                 |                 |       |             |    |         |
| 0x020C                  | ECRDTS3    | 31:24    | TSSEC[1:0]      |            |                 | TSNS[29:24]     |       |             |    |         |
|                         |            | 23:16    | TSNS[23:16]     |            |                 |                 |       |             |    |         |
|                         |            | 15:8     | TSNS[15:8]      |            |                 |                 |       |             |    |         |
|                         |            | 7:0      | TSNS[7:0]       |            |                 |                 |       |             |    |         |

.....continued

| Address | Name     | Bit Pos. | 7          | 6   | 5   | 4           | 3 | 2 | 1 | 0        |
|---------|----------|----------|------------|-----|-----|-------------|---|---|---|----------|
| 0x020D  | ECRDT54  | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x020E  | ECRDT55  | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x020F  | ECRDT56  | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x0210  | ECRDT57  | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x0211  | ECRDT58  | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x0212  | ECRDT59  | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x0213  | ECRDT510 | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x0214  | ECRDT511 | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x0215  | ECRDT512 | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x0216  | ECRDT513 | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x0217  | ECRDT514 | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x0218  | ECRDT515 | 31:24    | TSSEC[1:0] |     |     | TSNS[29:24] |   |   |   |          |
|         |          | 23:16    |            |     |     | TSNS[23:16] |   |   |   |          |
|         |          | 15:8     |            |     |     | TSNS[15:8]  |   |   |   |          |
|         |          | 7:0      |            |     |     | TSNS[7:0]   |   |   |   |          |
| 0x021C  | Reserved |          |            |     |     |             |   |   |   |          |
| ...     |          |          |            |     |     |             |   |   |   |          |
| 0x021E  |          |          |            |     |     |             |   |   |   |          |
| 0x021F  | PACYC    | 31:24    | CYC[29:24] |     |     |             |   |   |   |          |
|         |          | 23:16    | CYC[23:16] |     |     |             |   |   |   |          |
|         |          | 15:8     | CYC[15:8]  |     |     |             |   |   |   |          |
|         |          | 7:0      | CYC[7:0]   |     |     |             |   |   |   |          |
| 0x0220  | PACTRL   | 31:24    | ACT        | SEC | DEC |             |   |   |   |          |
|         |          | 23:16    |            |     |     |             |   |   |   |          |
|         |          | 15:8     |            |     |     |             |   |   |   | DIF[9:8] |
|         |          | 7:0      | DIF[7:0]   |     |     |             |   |   |   |          |

.....continued

| Address | Name      | Bit Pos. | 7 | 6 | 5 | 4     | 3   | 2  | 1    | 0            |
|---------|-----------|----------|---|---|---|-------|-----|----|------|--------------|
| 0x0221  | EG0STNS   | 31:24    |   |   |   |       |     |    |      | STNS[30:0]   |
|         |           | 23:16    |   |   |   |       |     |    |      | STNS[30:0]   |
|         |           | 15:8     |   |   |   |       |     |    |      | STNS[30:0]   |
|         |           | 7:0      |   |   |   |       |     |    |      | STNS[30:0]   |
| 0x0222  | EG0STSECL | 31:24    |   |   |   |       |     |    |      | STSEC[31:24] |
|         |           | 23:16    |   |   |   |       |     |    |      | STSEC[23:16] |
|         |           | 15:8     |   |   |   |       |     |    |      | STSEC[15:8]  |
|         |           | 7:0      |   |   |   |       |     |    |      | STSEC[7:0]   |
| 0x0223  | EG0STSECH | 31:24    |   |   |   |       |     |    |      |              |
|         |           | 23:16    |   |   |   |       |     |    |      |              |
|         |           | 15:8     |   |   |   |       |     |    |      | STSEC[47:40] |
|         |           | 7:0      |   |   |   |       |     |    |      | STSEC[39:32] |
| 0x0224  | EG0PW     | 31:24    |   |   |   |       |     |    |      | PW[29:24]    |
|         |           | 23:16    |   |   |   |       |     |    |      | PW[23:16]    |
|         |           | 15:8     |   |   |   |       |     |    |      | PW[15:8]     |
|         |           | 7:0      |   |   |   |       |     |    |      | PW[7:0]      |
| 0x0225  | EG0IT     | 31:24    |   |   |   |       |     |    |      | IT[29:24]    |
|         |           | 23:16    |   |   |   |       |     |    |      | IT[23:16]    |
|         |           | 15:8     |   |   |   |       |     |    |      | IT[15:8]     |
|         |           | 7:0      |   |   |   |       |     |    |      | IT[7:0]      |
| 0x0226  | EG0CTL    | 31:24    |   |   |   |       |     |    |      |              |
|         |           | 23:16    |   |   |   |       |     |    |      |              |
|         |           | 15:8     |   |   |   |       |     |    |      |              |
|         |           | 7:0      |   |   |   | ISREL | REP | AH | STOP | START        |
| 0x0227  | EG1STNS   | 31:24    |   |   |   |       |     |    |      | STNS[30:0]   |
|         |           | 23:16    |   |   |   |       |     |    |      | STNS[30:0]   |
|         |           | 15:8     |   |   |   |       |     |    |      | STNS[30:0]   |
|         |           | 7:0      |   |   |   |       |     |    |      | STNS[30:0]   |
| 0x0228  | EG1STSECL | 31:24    |   |   |   |       |     |    |      | STSEC[31:24] |
|         |           | 23:16    |   |   |   |       |     |    |      | STSEC[23:16] |
|         |           | 15:8     |   |   |   |       |     |    |      | STSEC[15:8]  |
|         |           | 7:0      |   |   |   |       |     |    |      | STSEC[7:0]   |
| 0x0229  | EG1STSECH | 31:24    |   |   |   |       |     |    |      |              |
|         |           | 23:16    |   |   |   |       |     |    |      |              |
|         |           | 15:8     |   |   |   |       |     |    |      | STSEC[47:40] |
|         |           | 7:0      |   |   |   |       |     |    |      | STSEC[39:32] |
| 0x022A  | EG1PW     | 31:24    |   |   |   |       |     |    |      | PW[29:24]    |
|         |           | 23:16    |   |   |   |       |     |    |      | PW[23:16]    |
|         |           | 15:8     |   |   |   |       |     |    |      | PW[15:8]     |
|         |           | 7:0      |   |   |   |       |     |    |      | PW[7:0]      |
| 0x022B  | EG1IT     | 31:24    |   |   |   |       |     |    |      | IT[29:24]    |
|         |           | 23:16    |   |   |   |       |     |    |      | IT[23:16]    |
|         |           | 15:8     |   |   |   |       |     |    |      | IT[15:8]     |
|         |           | 7:0      |   |   |   |       |     |    |      | IT[7:0]      |
| 0x022C  | EG1CTL    | 31:24    |   |   |   |       |     |    |      |              |
|         |           | 23:16    |   |   |   |       |     |    |      |              |
|         |           | 15:8     |   |   |   |       |     |    |      |              |
|         |           | 7:0      |   |   |   | ISREL | REP | AH | STOP | START        |
| 0x022D  | EG2STNS   | 31:24    |   |   |   |       |     |    |      | STNS[30:0]   |
|         |           | 23:16    |   |   |   |       |     |    |      | STNS[30:0]   |
|         |           | 15:8     |   |   |   |       |     |    |      | STNS[30:0]   |
|         |           | 7:0      |   |   |   |       |     |    |      | STNS[30:0]   |
| 0x022E  | EG2STSECL | 31:24    |   |   |   |       |     |    |      | STSEC[31:24] |
|         |           | 23:16    |   |   |   |       |     |    |      | STSEC[23:16] |
|         |           | 15:8     |   |   |   |       |     |    |      | STSEC[15:8]  |
|         |           | 7:0      |   |   |   |       |     |    |      | STSEC[7:0]   |
| 0x022F  | EG2STSECH | 31:24    |   |   |   |       |     |    |      |              |
|         |           | 23:16    |   |   |   |       |     |    |      |              |
|         |           | 15:8     |   |   |   |       |     |    |      | STSEC[47:40] |
|         |           | 7:0      |   |   |   |       |     |    |      | STSEC[39:32] |

.....continued

| Address | Name      | Bit Pos. | 7      | 6       | 5     | 4          | 3       | 2       | 1       | 0            |
|---------|-----------|----------|--------|---------|-------|------------|---------|---------|---------|--------------|
| 0x0230  | EG2PW     | 31:24    |        |         |       |            |         |         |         | PW[29:24]    |
|         |           | 23:16    |        |         |       |            |         |         |         | PW[23:16]    |
|         |           | 15:8     |        |         |       |            |         |         |         | PW[15:8]     |
|         |           | 7:0      |        |         |       |            |         |         |         | PW[7:0]      |
| 0x0231  | EG2IT     | 31:24    |        |         |       |            |         |         |         | IT[29:24]    |
|         |           | 23:16    |        |         |       |            |         |         |         | IT[23:16]    |
|         |           | 15:8     |        |         |       |            |         |         |         | IT[15:8]     |
|         |           | 7:0      |        |         |       |            |         |         |         | IT[7:0]      |
| 0x0232  | EG2CTL    | 31:24    |        |         |       |            |         |         |         |              |
|         |           | 23:16    |        |         |       |            |         |         |         |              |
|         |           | 15:8     |        |         |       |            |         |         |         |              |
|         |           | 7:0      |        |         |       | ISREL      | REP     | AH      | STOP    | START        |
| 0x0233  | EG3STNS   | 31:24    |        |         |       |            |         |         |         | STNS[30:0]   |
|         |           | 23:16    |        |         |       |            |         |         |         | STNS[30:0]   |
|         |           | 15:8     |        |         |       |            |         |         |         | STNS[30:0]   |
|         |           | 7:0      |        |         |       |            |         |         |         | STNS[30:0]   |
| 0x0234  | EG3STSECL | 31:24    |        |         |       |            |         |         |         | STSEC[31:24] |
|         |           | 23:16    |        |         |       |            |         |         |         | STSEC[23:16] |
|         |           | 15:8     |        |         |       |            |         |         |         | STSEC[15:8]  |
|         |           | 7:0      |        |         |       |            |         |         |         | STSEC[7:0]   |
| 0x0235  | EG3STSECH | 31:24    |        |         |       |            |         |         |         |              |
|         |           | 23:16    |        |         |       |            |         |         |         |              |
|         |           | 15:8     |        |         |       |            |         |         |         | STSEC[47:40] |
|         |           | 7:0      |        |         |       |            |         |         |         | STSEC[39:32] |
| 0x0236  | EG3PW     | 31:24    |        |         |       |            |         |         |         | PW[29:24]    |
|         |           | 23:16    |        |         |       |            |         |         |         | PW[23:16]    |
|         |           | 15:8     |        |         |       |            |         |         |         | PW[15:8]     |
|         |           | 7:0      |        |         |       |            |         |         |         | PW[7:0]      |
| 0x0237  | EG3IT     | 31:24    |        |         |       |            |         |         |         | IT[29:24]    |
|         |           | 23:16    |        |         |       |            |         |         |         | IT[23:16]    |
|         |           | 15:8     |        |         |       |            |         |         |         | IT[15:8]     |
|         |           | 7:0      |        |         |       |            |         |         |         | IT[7:0]      |
| 0x0238  | EG3CTL    | 31:24    |        |         |       |            |         |         |         |              |
|         |           | 23:16    |        |         |       |            |         |         |         |              |
|         |           | 15:8     |        |         |       |            |         |         |         |              |
|         |           | 7:0      |        |         |       | ISREL      | REP     | AH      | STOP    | START        |
| 0x0239  | PPSCTL    | 31:24    |        |         |       |            |         |         |         |              |
|         |           | 23:16    |        |         |       |            |         |         |         |              |
|         |           | 15:8     |        |         |       |            |         |         |         |              |
|         |           | 7:0      |        |         |       | PPSPW[4:0] |         |         | PPSDIS  | PPSEN        |
| 0x023A  | SEVINTEN  | 31:24    | PADONE | PPSDONE |       |            |         |         |         |              |
|         |           | 23:16    |        |         |       |            | EG3DONE | EG2DONE | EG1DONE | EG0DONE      |
|         |           | 15:8     |        |         |       |            |         |         |         |              |
|         |           | 7:0      | EC3DA  | EC3OF   | EC2DA | EC2OF      | EC1DA   | EC1OF   | EC0DA   | EC0OF        |
| 0x023B  | SEVINTDIS | 31:24    | PADONE | PPSDONE |       |            |         |         |         |              |
|         |           | 23:16    |        |         |       |            | EG3DONE | EG2DONE | EG1DONE | EG0DONE      |
|         |           | 15:8     |        |         |       |            |         |         |         |              |
|         |           | 7:0      | EC3DA  | EC3OF   | EC2DA | EC2OF      | EC1DA   | EC1OF   | EC0DA   | EC0OF        |
| 0x023C  | SEVIM     | 31:24    | PADONE | PPSDONE |       |            |         |         |         |              |
|         |           | 23:16    |        |         |       |            | EG3DONE | EG2DONE | EG1DONE | EG0DONE      |
|         |           | 15:8     |        |         |       |            |         |         |         |              |
|         |           | 7:0      | EC3DA  | EC3OF   | EC2DA | EC2OF      | EC1DA   | EC1OF   | EC0DA   | EC0OF        |
| 0x023D  | SEVSTS    | 31:24    | PADONE | PPSDONE |       |            |         |         |         |              |
|         |           | 23:16    |        |         |       |            | EG3DONE | EG2DONE | EG1DONE | EG0DONE      |
|         |           | 15:8     |        |         |       |            |         |         |         |              |
|         |           | 7:0      | EC3DA  | EC3OF   | EC2DA | EC2OF      | EC1DA   | EC1OF   | EC0DA   | EC0OF        |

## Related Links

### 1.3. Register Bit Types

### 11.6.1 Queue Transmit Configuration

**Name:** QTXCFG

**Address:** 0x0081



**Important:** When updating the fields of this register, the contents of reserved bits must not be changed. A read-modified-write process must be used when writing to this register.



**Important:** Fields in this register shall only be changed prior to setting the Configuration Synchronization (SYNC) bit in the OPEN Alliance Configuration 0 (OA\_CONFIG0) register enabling Ethernet packet transfer. Once the SYNC bit has been set, fields in this register must not be changed without resetting the MAC-PHY.

|        |            |            |     |     |           |     |     |     |
|--------|------------|------------|-----|-----|-----------|-----|-----|-----|
| Bit    | 31         | 30         | 29  | 28  | 27        | 26  | 25  | 24  |
|        | CTTHR[1:0] |            |     |     |           |     |     |     |
| Access | R/W        | R/W        | R/W | R/W | R/W       | R/W | R/W | R/W |
| Reset  | 0          | 1          | 0   | 1   | 1         | 0   | 0   | 0   |
| Bit    | 23         | 22         | 21  | 20  | 19        | 18  | 17  | 16  |
|        |            | BUFSZ[2:0] |     |     | MACFCSDIS |     |     |     |
| Access | R/W        | R/W        | R/W | R/W | R/W       | RO  | RO  | RO  |
| Reset  | 0          | 0          | 0   | 1   | 0         | 0   | 0   | 0   |
| Bit    | 15         | 14         | 13  | 12  | 11        | 10  | 9   | 8   |
|        |            |            |     |     |           |     |     |     |
| Access | RO         | RO         | RO  | RO  | RO        | RO  | RO  | RO  |
| Reset  | 0          | 0          | 0   | 0   | 0         | 0   | 0   | 0   |
| Bit    | 7          | 6          | 5   | 4   | 3         | 2   | 1   | 0   |
|        |            |            |     |     |           |     |     |     |
| Access | RO         | RO         | RO  | RO  | RO        | RO  | RO  | RO  |
| Reset  | 0          | 0          | 0   | 0   | 0         | 0   | 0   | 0   |

#### Bits 31:30 – CTTHR[1:0] Cut-through threshold

This field configures the minimum number of buffers / blocks of Ethernet frame data to fill from the SPI host before the MAC may begin to transmit to the network in cut-through mode.

| Value | Description       |
|-------|-------------------|
| 00    | 1 block           |
| 01    | 2 block (Default) |
| 10    | 3 block           |
| 11    | 4 block           |

#### Bits 22:20 – BUFSZ[2:0] Buffer Size

Number of bytes allocated to each buffer in the transmit queue.



**Important:** The buffer size configured in this field must match the Block Payload Size (BPS) configured in the OPEN Alliance Configuration 0 (OA\_CONFIG0) register.

| Value  | Description        |
|--------|--------------------|
| 000    | 32 Bytes           |
| 001    | 64 Bytes (default) |
| Others | Reserved           |

**Bit 19 – MACFCSDIS** MAC Frame Check Sequence Disable

By default, the device will accept transmit frames from the SPI host and the MAC will automatically pad the frames to the minimum 64 byte length with an appended calculated Frame Check Sequence (FCS). When set, this bit will disable the automatic padding and FCS insertion into transmitted frames, assuming that the SPI host has already performed padding and appending of the FCS. Additionally, when this bit is set, the MACPHY will validate the FCS of the frame received from the SPI host. If the FCS does not match, indicating a possible bit-error over the SPI link, the frame will not be transmitted to the network.

| Value | Description                                                                                                                                    |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | MAC will perform frame padding and insertion of the FCS                                                                                        |
| 1     | The MAC will not pad the frame or insert the FCS. The SPI host is responsible for padding the frame to the minimum size and appending the FCS. |

## 11.6.2 Queue Receive Configuration

**Name:** QRXCFG

**Address:** 0x0082



**Important:** When updating the fields of this register, the contents of reserved bits must not be changed. A read-modified-write process must be used when writing to this register.



**Important:** Fields in this register shall only be changed prior to setting the Configuration Synchronization (SYNC) bit in the OPEN Alliance Configuration 0 (OA\_CONFIG0) register enabling Ethernet packet transfer. Once the SYNC bit has been set, fields in this register must not be changed without resetting the MAC-PHY.

|        |     |            |     |     |     |     |     |     |
|--------|-----|------------|-----|-----|-----|-----|-----|-----|
| Bit    | 31  | 30         | 29  | 28  | 27  | 26  | 25  | 24  |
| Access | R/W | R/W        | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0          | 0   | 1   | 1   | 0   | 0   | 0   |
| Bit    | 23  | 22         | 21  | 20  | 19  | 18  | 17  | 16  |
|        |     | BUFSZ[2:0] |     |     |     |     |     |     |
| Access | R/W | R/W        | R/W | R/W | RO  | RO  | RO  | RO  |
| Reset  | 0   | 0          | 0   | 1   | 0   | 0   | 0   | 0   |
| Bit    | 15  | 14         | 13  | 12  | 11  | 10  | 9   | 8   |
| Access | RO  | RO         | RO  | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0          | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7   | 6          | 5   | 4   | 3   | 2   | 1   | 0   |
| Access | R/W | R/W        | R/W | R/W | R/W | R/W | RO  | RO  |
| Reset  | 0   | 0          | 0   | 0   | 1   | 1   | 0   | 0   |

### Bits 22:20 – BUFSZ[2:0] Buffer Size

Number of bytes allocated to each buffer in the receive queue.



**Important:** The buffer size configured in this field must match the Block Payload Size (BPS) configured in the OPEN Alliance Configuration 0 (OA\_CONFIG0) register.

| Value  | Description        |
|--------|--------------------|
| 000    | 32 Bytes           |
| 001    | 64 Bytes (default) |
| Others | Reserved           |





### 11.6.3 Pad Control Register

**Name:** PADCTRL  
**Address:** x0088

|        |            |     |            |     |            |     |              |     |
|--------|------------|-----|------------|-----|------------|-----|--------------|-----|
| Bit    | 31         | 30  | 29         | 28  | 27         | 26  | 25           | 24  |
|        | PDRV3[1:0] |     | PDRV2[1:0] |     | PDRV1[1:0] |     |              |     |
| Access | R/W        | R/W | R/W        | R/W | R/W        | R/W | R/W          | R/W |
| Reset  | 1          | 1   | 1          | 1   | 1          | 1   | 0            | 0   |
| Bit    | 23         | 22  | 21         | 20  | 19         | 18  | 17           | 16  |
|        | REFCLKSEL  |     |            |     |            |     | ACMASEL[1:0] |     |
| Access | R/W        | R/W | R/W        | R/W | R/W        | R/W | R/W          | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0          | 0   | 0            | 0   |
| Bit    | 15         | 14  | 13         | 12  | 11         | 10  | 9            | 8   |
|        |            |     |            |     | B0SEL[1:0] |     | A4SEL[1:0]   |     |
| Access | R/W        | R/W | R/W        | R/W | R/W        | R/W | R/W          | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0          | 1   | 0            | 0   |
| Bit    | 7          | 6   | 5          | 4   | 3          | 2   | 1            | 0   |
|        | A3SEL[1:0] |     | A2SEL[1:0] |     | A1SEL[1:0] |     | A0SEL[1:0]   |     |
| Access | R/W        | R/W | R/W        | R/W | R/W        | R/W | R/W          | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0          | 0   | 0            | 0   |

#### Bits 31:30 – PDRV3[1:0] Digital Output Pad Drive Strength

This field configures the output pad drive strength for pin group 3.

| Value | Description                  |
|-------|------------------------------|
| 00    | Low current drive            |
| 01    | Medium-low current drive     |
| 10    | Medium-high current drive    |
| 11    | High current drive (default) |

#### Bits 29:28 – PDRV2[1:0] Digital Output Pad Drive Strength

This field configures the output pad drive strength for pin group 2.

| Value | Description                  |
|-------|------------------------------|
| 00    | Low current drive            |
| 01    | Medium-low current drive     |
| 10    | Medium-high current drive    |
| 11    | High current drive (default) |

#### Bits 27:26 – PDRV1[1:0] Digital Output Pad Drive Strength

This field configures the output pad drive strength for pin group 1.

| Value | Description                  |
|-------|------------------------------|
| 00    | Low current drive            |
| 01    | Medium-low current drive     |
| 10    | Medium-high current drive    |
| 11    | High current drive (default) |

#### Bit 23 – REFCLKSEL Reference Clock Select

This bit selects the clock reference clock used for event capture, event generation and time stamping.

| Value | Description                                                                 |
|-------|-----------------------------------------------------------------------------|
| 0     | Reference clock is the internal 25 MHz clock derived from attached crystal. |

| Value | Description                                                                                                                                                  |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | Reference clock is an external clock on pin DIOB0. The DIOB0 Select (B0SEL) bit field below must also be configured to 00b (external reference clock input). |

#### Bits 17:16 – ACMASEL[1:0] ACMA Input Select

Selects the ACMA input pin.

| Value | Description                                                                                                                                                         |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00    | ACMA disabled                                                                                                                                                       |
| 01    | ACMA enabled with the control signal provided by event generator 0<br><b>Note:</b> If this value is selected, event generator 0 cannot be used as a DIO pin source. |
| 10    | ACMA enabled with the control signal on DIOA2                                                                                                                       |
| 11    | Reserved                                                                                                                                                            |

#### Bits 11:10 – B0SEL[1:0] DIOB0 Signal Select

This field configures the DIOB0 pin signal select.

**Note:** The DIOB0 pin is configured by default to be an output.

| Value | Description                                                                                                                                                                             |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00    | External 1588 reference clock (requires configuration in REFCLKSEL bit field above) (Input)                                                                                             |
| 01    | Clock output as configured in Clock Output Control Register, CLKOE (Output)<br>If this pin is not used, it may be connected to ground as long as the clock output is disabled in CLKOE. |
| 10    | Reserved (Input)                                                                                                                                                                        |
| 11    | Reserved (Input)                                                                                                                                                                        |

#### Bits 9:8 – A4SEL[1:0] DIOA4 Signal Select

This field configures the DIOA4 pin signal select

| Value | Description                                                                                    |
|-------|------------------------------------------------------------------------------------------------|
| 00    | Reserved (Input)                                                                               |
| 01    | 1PPS (Output)                                                                                  |
| 10    | Event Generator 2 (Output)<br><b>Note:</b> No signal will be provided to DIOA4 if ACMASEL = 2. |
| 11    | Event Generator 3 (Output)                                                                     |

#### Bits 7:6 – A3SEL[1:0] DIOA3 Signal Select

This field configures the DIOA3 pin signal select

| Value | Description                |
|-------|----------------------------|
| 00    | Event Capture (Input)      |
| 01    | Event Generator 3 (Output) |
| 10    | Reserved (Output)          |
| 11    | Reserved (Output)          |

#### Bits 5:4 – A2SEL[1:0] DIOA2 Signal Select

This field configures the DIOA2 pin signal select

| Value | Description                                                                                    |
|-------|------------------------------------------------------------------------------------------------|
| 00    | ACMA and/or Event Capture (Input)<br>ACMA is configured in the ACMASEL bits, above             |
| 01    | Event Generator 2 (Output)<br><b>Note:</b> No signal will be provided to DIOA2 if ACMASEL = 2. |
| 10    | Reserved (Output)                                                                              |
| 11    | Reserved (Input)                                                                               |

#### Bits 3:2 – A1SEL[1:0] DIO1 Signal Select

This field configures the DIO1 pin signal select

| Value | Description                |
|-------|----------------------------|
| 00    | Event Capture (Input)      |
| 01    | Event Generator 1 (Output) |
| 10    | Reserved (Output)          |

| Value | Description       |
|-------|-------------------|
| 11    | Reserved (Output) |

**Bits 1:0 – A0SEL[1:0] DIOA0 Signal Select**

This field configures the DIOA0 pin signal select

| Value | Description                |
|-------|----------------------------|
| 00    | Event Capture (Input)      |
| 01    | Event Generator 0 (Output) |
| 10    | Reserved (Output)          |
| 11    | Reserved (Output)          |

## 11.6.4 Clock Output Control

**Name:** CLKOCTL  
**Address:** 0x0089

|        |    |    |    |          |    |    |              |          |
|--------|----|----|----|----------|----|----|--------------|----------|
| Bit    | 31 | 30 | 29 | 28       | 27 | 26 | 25           | 24       |
| Access | RO | RO | RO | RO       | RO | RO | RO           | RO       |
| Reset  | 0  | 0  | 0  | 0        | 0  | 0  | 0            | 0        |
| Bit    | 23 | 22 | 21 | 20       | 19 | 18 | 17           | 16       |
| Access | RO | RO | RO | RO       | RO | RO | RO           | RO       |
| Reset  | 0  | 0  | 0  | 0        | 0  | 0  | 0            | 0        |
| Bit    | 15 | 14 | 13 | 12       | 11 | 10 | 9            | 8        |
| Access | RO | RO | RO | RO       | RO | RO | RO           | RO       |
| Reset  | 0  | 0  | 0  | 0        | 0  | 0  | 0            | 0        |
| Bit    | 7  | 6  | 5  | 4        | 3  | 2  | 1            | 0        |
| Access | RO | RO | RO | CLKOEN   | RO | RO | CLKOSEL[1:0] |          |
| Reset  | 0  | 0  | 0  | R/W NASR | 0  | 0  | R/W NASR     | R/W NASR |
|        |    |    |    | 0        |    |    | 0            | 1        |

### Bit 4 – CLKOEN Clock Output Enable

Setting this bit will enable the clock output to the CLKOUT pin.

**Note:** This bit is only reset by power-on. It is not affected by a soft reset or assertion of the RESET\_N pin.

| Value | Description                        |
|-------|------------------------------------|
| 0     | Clock output to CLKOUT is disabled |
| 1     | Clock output to CLKOUT is enabled  |

### Bits 1:0 – CLKOSEL[1:0] Clock Output Select

This field selects the clock for output onto the CLKOUT pin when enabled.

**Note:** This bit is only reset by power-on. It is not affected by a soft reset or assertion of the RESET\_N pin.

| Value | Description |
|-------|-------------|
| 00    | 8.33 MHz    |
| 01    | 12.5 MHz    |
| 10    | 6.25 MHz    |
| 11    | Reserved    |

## 11.6.5 Miscellaneous

**Name:** MISC  
**Address:** 0x008C

|        |              |    |    |         |               |    |    |    |
|--------|--------------|----|----|---------|---------------|----|----|----|
| Bit    | 31           | 30 | 29 | 28      | 27            | 26 | 25 | 24 |
| Access | RO           | RO | RO | RO      | RO            | RO | RO | RO |
| Reset  | 1            | 0  | 0  | 0       | 0             | 0  | 0  | 0  |
| Bit    | 23           | 22 | 21 | 20      | 19            | 18 | 17 | 16 |
| Access | RO           | RO | RO | RO      | RO            | RO | RO | RO |
| Reset  | 0            | 0  | 0  | 0       | 0             | 0  | 0  | 0  |
| Bit    | 15           | 14 | 13 | 12      | 11            | 10 | 9  | 8  |
| Access | RO           | RO | RO | UV18FEN | UV18FTM[11:8] |    |    |    |
| Reset  | 0            | 0  | 0  | 1       | 0             | 0  | 0  | 0  |
| Bit    | 7            | 6  | 5  | 4       | 3             | 2  | 1  | 0  |
| Access | UV18FTM[7:0] |    |    |         |               |    |    |    |
| Reset  | 0            | 0  | 0  | 0       | 0             | 0  | 0  | 1  |

### Bit 12 – UV18FEN 1.8V Supply Under-Voltage Filter Enable

Setting this bit enables the 1.8V supply under-voltage detector filter.

| Value | Description                                                 |
|-------|-------------------------------------------------------------|
| 0     | 1.8V supply under-voltage detector filter disabled          |
| 1     | 1.8V supply under-voltage detector filter enabled (default) |

### Bits 11:0 – UV18FTM[11:0] 1.8V supply Under-Voltage Filter Time

This field configures the 1.8V supply under-voltage filter in increments of 80 ns. The voltage must fall below the under-voltage threshold for longer than the time configured in this field before the under-voltage condition will be triggered.

| Value | Description            |
|-------|------------------------|
| 0x000 | 0 ns                   |
| 0x001 | 80 ns                  |
| ...   | ...                    |
| 0x010 | 1.28 $\mu$ s           |
| ...   | ...                    |
| 0x040 | 5.12 $\mu$ s (default) |
| ...   | ...                    |
| xFFFF | 327.8 ms               |

## 11.6.6 Device Identification

**Name:** DEVID  
**Address:** 0x0094

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  |
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 1  |
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | x  | 0  | 0  | 1  | 0  |

### Bits 19:4 – MODEL[15:0] Model Number

Device's model / product identification number

| Value | Description |
|-------|-------------|
| 8650h | LAN8650     |
| 8651h | LAN8651     |

### Bits 3:0 – REV[3:0] Revision Number

Device's silicon revision identification number

**Note:** The default value of the this field varies dependent on the silicon revision number.

| Value | Description        |
|-------|--------------------|
| 0001  | Silicon Revision 1 |
| 0010  | Silicon Revision 2 |

**11.6.7 Bus Parity Control and Status****Name:** BUSPCS**Address:** 0x96

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |        |        |         |         |
|--------|----|----|----|----|--------|--------|---------|---------|
| Bit    | 23 | 22 | 21 | 20 | 19     | 18     | 17      | 16      |
| Access | RO | RO | RO | RO | MBMPER | SPIPER | CSRBPER | SRAMPER |
| Reset  | 0  | 0  | 0  | 1  | 0      | 0      | 0       | 0       |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |           |           |          |           |         |
|--------|----|----|----|-----------|-----------|----------|-----------|---------|
| Bit    | 7  | 6  | 5  | 4         | 3         | 2        | 1         | 0       |
| Access | RO | RO | RO | CSRBDPERG | SRAMDPERI | MBMDPERI | BMGRAPERI | PARGCEN |
| Reset  | 0  | 0  | 1  | 0         | 0         | 0        | 0         | 0       |

**Bit 19 – MBMPER** MAC Buffer Manager Parity Error Status

This bit is set when the MAC buffer manager detects a bus parity error.

| Value | Description                                              |
|-------|----------------------------------------------------------|
| 0     | No bus parity error detected                             |
| 1     | Bus parity error has been detected by MAC buffer manager |

**Bit 18 – SPIPER** SPI Parity Error Status

This bit is set when the SPI block detects a bus parity error.

| Value | Description                                     |
|-------|-------------------------------------------------|
| 0     | No bus parity error detected                    |
| 1     | Bus parity error has been detected by SPI block |

**Bit 17 – CSRBPER** Control/Status Register Bridge Parity Error Status

This bit is set when the bridge to the control/status registers detects a bus parity error. If the parity error occurs during a read operation, the bridge will return a data value of zero. Write operations to the control/status register bridge will be blocked on detection of a parity error.

| Value | Description                                                              |
|-------|--------------------------------------------------------------------------|
| 0     | No bus parity error detected                                             |
| 1     | Bus parity error has been detected by the control/status register bridge |

**Bit 16 – SRAMPER** SRAM Controller Parity Error Status

This bit is set when the SRAM controller detects a bus parity error. If the parity occurs on a read from the SRAM, the controller will return data of zero. Write operations to the SRAM will be blocked on detection of a parity error.

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | No bus parity error detected                              |
| 1     | Bus parity error has been detected by the SRAM controller |



**Bit 4 – CSRBPERG** Bridge Parity Error Injection

When this bit is set, the bridge to the control/status register bus will inject a bus data parity error on read.

| Value | Description                                                                      |
|-------|----------------------------------------------------------------------------------|
| 0     | Normal operation                                                                 |
| 1     | Control/status register bridge will inject a data read parity error onto the bus |

**Bit 3 – SRAMDPERI** SRAM Controller Parity Error Injection

When this bit is set, the SRAM controller will inject a bus data parity error on read.

| Value | Description                                                           |
|-------|-----------------------------------------------------------------------|
| 0     | Normal operation                                                      |
| 1     | SRAM controller will inject a bus data read parity error onto the bus |

**Bit 2 – MBMDPERI** Buffer Manager Data Parity Error Injection

When this bit is set, the MAC buffer manager will inject a bus data parity error on write.

| Value | Description                                                              |
|-------|--------------------------------------------------------------------------|
| 0     | Normal operation                                                         |
| 1     | MAC buffer manager will inject a data parity error on write bus accesses |

**Bit 1 – BMGRAPERI** Buffer Manager Address Parity Error Injection

When this bit is set, the BMAC buffer manager will inject a bus address parity error on read and write.

| Value | Description                                                                       |
|-------|-----------------------------------------------------------------------------------|
| 0     | Normal operation                                                                  |
| 1     | MAC buffer manager will inject an address parity error on read/write bus accesses |

**Bit 0 – PARGCEN** Parity Generation and Check Enable

When set, this bit will enable the parity generation and checking on the internal bus.

| Value | Description                                                       |
|-------|-------------------------------------------------------------------|
| 0     | Internal bus parity generation and checking is disabled (default) |
| 1     | Internal bus parity generation and checking is enabled            |

### 11.6.8 Configuration Protection Control

**Name:** CFGPRTCTL

**Address:** 0x0099

This register is used to control the protection of various configuration registers and fields from accidental writing. When the Write Enable (WREN) field is '0', then writes to sensitive configuration registers and fields will be blocked.

|        |      |      |    |    |    |    |    |    |
|--------|------|------|----|----|----|----|----|----|
| Bit    | 31   | 30   | 29 | 28 | 27 | 26 | 25 | 24 |
|        | KEY2 | KEY1 |    |    |    |    |    |    |
| Access | RO   | RO   |    |    | RO | RO | RO | RO |
| Reset  | 0    | 0    |    |    | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        |    |    |    |    |    |    |    |    |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|        |    |    |    |    |    |    |    |      |
|--------|----|----|----|----|----|----|----|------|
| Bit    | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
|        |    |    |    |    |    |    |    | WREN |
| Access | RO | RO | RO | RO | RO | RO | RO | R/W  |
| Reset  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1    |

#### Bit 31 – KEY2 Key #2 Accepted

This bit is set when Key #2 (434F4E46h) has been successfully written to this register after Key #1.

**Note:** This bit is cleared on write to any other bit field in this register.

| Value | Description                                           |
|-------|-------------------------------------------------------|
| 0     | Key #2 has not been successfully written after Key #1 |
| 1     | Key #2 has been successfully written after Key #1     |

#### Bit 30 – KEY1 Key #1 Accepted

This bit is set when Key #1 (53464352h) has been successfully written to this register.

**Note:** This bit is cleared on write of any other value is to this register, except Key #2.

| Value | Description                              |
|-------|------------------------------------------|
| 0     | Key #1 has not been successfully written |
| 1     | Key #1 has been successfully written     |

#### Bit 0 – WREN Configuration Write Enable

When this bit is clear, writes to protected register bit fields are disabled to protect against accidental configuration changes. Writable bit fields may be written when this bit is set.

**Note:** This bit may only be written once both Key #1 and Key #2 have been successfully written in the correct sequence and fields **KEY1** and **KEY2** are both set.

| Value | Description                                              |
|-------|----------------------------------------------------------|
| 0     | Writes to register bit fields disabled (Protected mode)  |
| 1     | Writes to register bit fields enabled (Normal operation) |

**11.6.9 SRAM Error Correction Code Control****Name:** ECCCTRL**Address:** 0x0100

|        |              |    |    |    |    |          |              |          |
|--------|--------------|----|----|----|----|----------|--------------|----------|
| Bit    | 31           | 30 | 29 | 28 | 27 | 26       | 25           | 24       |
| Access | RO           | RO | RO | RO | RO | RO       | RO           | RO       |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0        | 0            | 0        |
| Bit    | 23           | 22 | 21 | 20 | 19 | 18       | 17           | 16       |
| Access | RO           | RO | RO | RO | RO | R/W      | DECDIS       | ENCDIS   |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0        | 0            | 0        |
| Bit    | 15           | 14 | 13 | 12 | 11 | 10       | 9            | 8        |
| Access | SBERLMT[7:0] |    |    |    |    |          |              |          |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0        | 0            | 1        |
| Bit    | 7            | 6  | 5  | 4  | 3  | 2        | 1            | 0        |
| Access | RO           | RO | RO | RO | RO | ERONESHT | ERCLR        | BERCNTEN |
| Reset  | 0            | 0  | 0  | 0  | 0  | 0        | R/W1 SC<br>0 | R/W<br>0 |

**Bit 17 – DECDIS** ECC Decoder Disable

When set, this bit will disable the ECC decoder.

| Value | Description          |
|-------|----------------------|
| 0     | ECC decoder enabled  |
| 1     | ECC decoder disabled |

**Bit 16 – ENCDIS** ECC Encoder Disable

When set, this bit will disable the ECC encoder.

| Value | Description          |
|-------|----------------------|
| 0     | ECC encoder enabled  |
| 1     | ECC encoder disabled |

**Bits 15:8 – SBERLMT[7:0]** Single Bit Error Limit

This field configures the limit for detected single bit errors.

**Bit 2 – ERONESHT** Error One Shot

This bit configures how errors are captured. When set, only the first error status and syndrome will be captured. When cleared, the latest error status and syndrome will be captured.

| Value | Description                    |
|-------|--------------------------------|
| 0     | Latest error/syndrome captured |
| 1     | First error/syndrome captured  |

**Bit 1 – ERCLR** Error Clear

Setting this bit will cause the ECC status register to clear.

**Note:** When set, the hardware will clear this bit automatically.

| Value | Description               |
|-------|---------------------------|
| 0     | Normal operation          |
| 1     | Clear ECC status register |

**Bit 0 – BERCNTEN** Bit Error Count Enable

When set, this bit will enable the error counters (single-bit, double-bit, etc.). When clear, the counters are frozen, but not cleared.

| Value | Description                    |
|-------|--------------------------------|
| 0     | Bit error counters are frozen  |
| 1     | Bit error counters are enabled |

**11.6.10 SRAM Error Correction Code Status****Name:** ECCSTS**Address:** 0x0101

|        |              |     |             |    |    |    |    |    |
|--------|--------------|-----|-------------|----|----|----|----|----|
| Bit    | 31           | 30  | 29          | 28 | 27 | 26 | 25 | 24 |
| Access | RO           | RO  | RO          | RO | RO | RO | RO | RO |
| Reset  | 0            | 0   | 0           | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23           | 22  | 21          | 20 | 19 | 18 | 17 | 16 |
|        | ERSTS[1:0]   |     | ERRSYN[5:0] |    |    |    |    |    |
| Access | R/W          | R/W | RC          | RC | RC | RC | RC | RC |
| Reset  | 0            | 0   | 0           | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15           | 14  | 13          | 12 | 11 | 10 | 9  | 8  |
|        | DBERCNT[7:0] |     |             |    |    |    |    |    |
| Access | RC           | RC  | RC          | RC | RC | RC | RC | RC |
| Reset  | 0            | 0   | 0           | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7            | 6   | 5           | 4  | 3  | 2  | 1  | 0  |
|        | SBERCNT[7:0] |     |             |    |    |    |    |    |
| Access | RC           | RC  | RC          | RC | RC | RC | RC | RC |
| Reset  | 0            | 0   | 0           | 0  | 0  | 0  | 0  | 0  |

**Bits 23:22 – ERSTS[1:0] Error Status**

| Value | Description                                 |
|-------|---------------------------------------------|
| 00    | No ECC error detected                       |
| 01    | Double bit error detected                   |
| 10    | Overall parity error detected (correctable) |
| 11    | Single bit error detected (correctable)     |

**Bits 21:16 – ERRSYN[5:0] Error Syndrome**

When a memory error is detected, this field contains the computed syndrome value. In the case of a single bit error, this syndrome will indicate which bit (0-38) contained the error (and was corrected).

| Value | Description                     |
|-------|---------------------------------|
| x00   | No single bit error detected    |
| x01   | SRAM bit 1, Parity bit 1 error  |
| x02   | SRAM bit 2, Parity bit 2 error  |
| x03   | SRAM bit 3, Data bit 0 error    |
| x04   | SRAM bit 4, Parity bit 3 error  |
| x05   | SRAM bit 5, Data bit 1 error    |
| x06   | SRAM bit 6, Data bit 2 error    |
| x07   | SRAM bit 7, Data bit 3 error    |
| x08   | SRAM bit 8, Parity bit 4 error  |
| x09   | SRAM bit 9, Data bit 4 error    |
| x0A   | SRAM bit 10, Data bit 5 error   |
| x0B   | SRAM bit 11, Data bit 6 error   |
| x0C   | SRAM bit 12, Data bit 7 error   |
| x0D   | SRAM bit 13, Data bit 8 error   |
| x0E   | SRAM bit 14, Data bit 9 error   |
| x0F   | SRAM bit 15, Data bit 10 error  |
| x10   | SRAM bit 16, Parity bit 5 error |
| x11   | SRAM bit 17, Data bit 11 error  |

| Value | Description                     |
|-------|---------------------------------|
| x12   | SRAM bit 18, Data bit 12 error  |
| x13   | SRAM bit 19, Data bit 13 error  |
| x14   | SRAM bit 20, Data bit 14 error  |
| x15   | SRAM bit 21, Data bit 15 error  |
| x16   | SRAM bit 22, Data bit 16 error  |
| x17   | SRAM bit 23, Data bit 17 error  |
| x18   | SRAM bit 24, Data bit 18 error  |
| x19   | SRAM bit 25, Data bit 19 error  |
| x1A   | SRAM bit 26, Data bit 20 error  |
| x1B   | SRAM bit 27, Data bit 21 error  |
| x1C   | SRAM bit 28, Data bit 22 error  |
| x1D   | SRAM bit 29, Data bit 23 error  |
| x1E   | SRAM bit 30, Data bit 24 error  |
| x1F   | SRAM bit 31, Data bit 25 error  |
| x20   | SRAM bit 32, Parity bit 6 error |
| x21   | SRAM bit 33, Data bit 26 error  |
| x22   | SRAM bit 34, Data bit 27 error  |
| x23   | SRAM bit 35, Data bit 28 error  |
| x24   | SRAM bit 36, Data bit 29 error  |
| x25   | SRAM bit 37, Data bit 30 error  |
| x26   | SRAM bit 38, Data bit 31 error  |

**Bits 15:8 – DBERCNT[7:0]** Double Bit Error Count

This field counts the number of double bit errors detected. The count will not saturate at 0xFF and will roll over to 0x00.

**Bits 7:0 – SBERCNT[7:0]** Single Bit Error Count

This field counts the number of single bit errors detected. The count will not saturate at the value configured in the Single Bit Error Limit (SBERLMT) and instead roll over to 0x00.

**11.6.11 SRAM Error Correction Code Fault Injection Control****Name:** ECCFLTCTRL**Address:** 0x0102

|        |                |            |     |                 |     |     |     |     |
|--------|----------------|------------|-----|-----------------|-----|-----|-----|-----|
| Bit    | 31             | 30         | 29  | 28              | 27  | 26  | 25  | 24  |
|        |                |            |     | FLTINJADR[12:8] |     |     |     |     |
| Access | RO             | RO         | RO  | R/W             | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0          | 0   | 0               | 0   | 0   | 0   | 0   |
| Bit    | 23             | 22         | 21  | 20              | 19  | 18  | 17  | 16  |
|        | FLTINJADR[7:0] |            |     |                 |     |     |     |     |
| Access | R/W            | R/W        | R/W | R/W             | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0          | 0   | 0               | 0   | 0   | 0   | 0   |
| Bit    | 15             | 14         | 13  | 12              | 11  | 10  | 9   | 8   |
|        |                | FLTINJONCE |     | FLTINJBIT2[5:0] |     |     |     |     |
| Access | RO             | R/W SC     | R/W | R/W             | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0          | 0   | 0               | 0   | 0   | 0   | 0   |
| Bit    | 7              | 6          | 5   | 4               | 3   | 2   | 1   | 0   |
|        | FLTINJAEQ      | FLTINJEN   |     | FLTINJBIT1[5:0] |     |     |     |     |
| Access | R/W            | R/W        | R/W | R/W             | R/W | R/W | R/W | R/W |
| Reset  | 0              | 0          | 0   | 0               | 0   | 0   | 0   | 0   |

**Bits 28:16 – FLTINJADR[12:0]** Fault Injection Address

only a READ from this address gets injected; Byte address, same as AHB. LSB 2 bits will be ignored.

**Bit 14 – FLTINJONCE** Fault Injection Once

When this bit is set, the fault will only be injected once upon next read of the SRAM, regardless of address.

**Note:** When set, this bit is self clearing upon injection of the fault.

| Value | Description                                                           |
|-------|-----------------------------------------------------------------------|
| 0     | Inject fault on every read of the Fault Injection Address             |
| 1     | Only inject the fault on the next read of the Fault Injection Address |

**Bits 13:8 – FLTINJBIT2[5:0]** Fault Injection Bit 2

This field configures which bit will be flipped on read of the SRAM. For single bit errors, configure this field to be the same as the Fault Injection Bit 1 (FLTINJBIT1) field. For double bit errors, configure this field to be different than the Fault Injection Bit 1 field.

| Value | Description                           |
|-------|---------------------------------------|
| x00   | Inject fault into read of SRAM bit 0  |
| x01   | Inject fault into read of SRAM bit 1  |
| ...   | ...                                   |
| x25   | Inject fault into read of SRAM bit 37 |
| x26   | Inject fault into read of SRAM bit 38 |
| x27   | Reserved                              |
| x28   | Reserved                              |
| ...   | ...                                   |
| x3F   | Reserved                              |

**Bit 7 – FLTINJAEQ** Fault Injection Address Equal

When set, the fault will only be injected when a SRAM read to the address specified by the Fault Injection Address field is performed.

| Value | Description                                                             |
|-------|-------------------------------------------------------------------------|
| 0     |                                                                         |
| 1     | Inject fault when SRAM address equals the Fault Injection Address field |

**Bit 6 – FLTINJEN** Fault Injection Enable

When this bit is set, bits will be flipped on the read of data from the SRAM address configured in the Fault Injection Address (FLTINJADR) field. The Fault Injection Address Equal (FLTINJAEQ) bit must also be set.

| Value | Description                 |
|-------|-----------------------------|
| 0     | Fault injection is disabled |
| 1     | Fault injection is enabled  |

**Bits 5:0 – FLTINJBIT1[5:0]** Fault Injection Bit 1

This field configures which bit will be flipped on read of the SRAM. For single bit errors, configure this field to be the same as the Fault Injection Bit 2 (FLTINJBIT2) field. For double bit errors, configure this field to be different than the Fault Injection Bit 2 field.

| Value | Description                           |
|-------|---------------------------------------|
| x00   | Inject fault into read of SRAM bit 0  |
| x01   | Inject fault into read of SRAM bit 1  |
| ...   | ...                                   |
| x25   | Inject fault into read of SRAM bit 37 |
| x26   | Inject fault into read of SRAM bit 38 |
| x27   | Reserved                              |
| x28   | Reserved                              |
| ...   | ...                                   |
| x3F   | Reserved                              |



**11.6.12 Event Capture 0 Control Register****Name:** ECOCTRL**Address:** 0x0200

|        |         |     |          |     |     |     |     |         |
|--------|---------|-----|----------|-----|-----|-----|-----|---------|
| Bit    | 31      | 30  | 29       | 28  | 27  | 26  | 25  | 24      |
| Access | R/W     | R/W | R/W      | R/W | R/W | R/W | R/W | R/W     |
| Reset  | 0       | 0   | 0        | 0   | 0   | 0   | 0   | 0       |
| Bit    | 23      | 22  | 21       | 20  | 19  | 18  | 17  | 16      |
| Access | R/W     | R/W | R/W      | R/W | R/W | R/W | R/W | R/W     |
| Reset  | 0       | 0   | 0        | 0   | 0   | 0   | 0   | 0       |
| Bit    | 15      | 14  | 13       | 12  | 11  | 10  | 9   | 8       |
|        |         |     | MAX[3:0] |     |     |     |     | EDGE[1] |
| Access | R/W     | R/W | R/W      | R/W | R/W | RO  | RO  | R/W     |
| Reset  | 0       | 0   | 0        | 0   | 0   | 0   | 0   | 0       |
| Bit    | 7       | 6   | 5        | 4   | 3   | 2   | 1   | 0       |
|        | EDGE[0] |     | SRC[2:0] |     | CLR |     | DA  | EN      |
| Access | R/W     | R/W | R/W      | R/W | W1S | R/W | RO  | R/W     |
| Reset  | 0       | 0   | 0        | 0   | 0   | 0   | 0   | 0       |

**Bits 14:11 – MAX[3:0]** Maximum number of captured timestamps

This is the maximum number of time stamps that can be captured by this event capture unit. When this unit is in use, this value must be greater than 0. Once this number is reached, timestamps must be read before any new timestamps will be captured; should another capture be triggered before a timestamp is read, an overflow condition will occur and the newest value will be lost.



**DANGER** This value shall not be changed if any of the timestamp units are enabled. Data corruption can occur.



**WARNING** The sum of all MAX values in all Timestamp control registers must not exceed 16.

| Value | Description                                                         |
|-------|---------------------------------------------------------------------|
| 0     | Only valid when this event capture unit is disabled.                |
| 1–F   | Maximum number of time stamps allocated to this event capture unit. |

**Bits 8:7 – EDGE[1:0]** Capture Edge Selection

**WARNING** This value can only be changed when disabled.

| Value | Description             |
|-------|-------------------------|
| 00    | Capture on rising edge  |
| 01    | Capture on falling edge |
| 10    | Capture on both edges   |
| 11    | Reserved                |

**Bits 6:4 – SRC[2:0]** Capture Signal Source

This value can only be changed when disabled.

| Value   | Description                     |
|---------|---------------------------------|
| 000     | Receive pattern match from PHY  |
| 001     | Transmit pattern match from PHY |
| 010     | DIOA0 input                     |
| 011     | DIOA1 input                     |
| 100     | DIOA2 input                     |
| 101     | DIOA3 input                     |
| 110–111 | Reserved                        |

**Bit 3 – CLR** Clear event capture unit

Writing a 1 to this bit will reset this event capture status and stored timestamps. Control settings will not change.

| Value | Description                    |
|-------|--------------------------------|
| 0     | No effect                      |
| 1     | Reset this event capture unit. |

**Bit 1 – DA** Data Available

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | This capture unit has no timestamps available to be read. |
| 1     | This capture unit has timestamps available to be read.    |

**Bit 0 – EN** Event Capture Unit Enable

| Value | Description                          |
|-------|--------------------------------------|
| 0     | This event capture unit is disabled. |
| 1     | This event capture unit is enabled.  |

**11.6.13 Event Capture 1 Control Register****Name:** EC1CTRL**Address:** 0x0201

|        |     |     |     |     |     |     |     |     |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| Access | R/W | R/W | R/W | R/W | R/W | RO  | RO  | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access | R/W | R/W | R/W | R/W | W1S | R/W | RO  | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 14:11 – MAX[3:0]** Maximum number of captured timestamps

This is the maximum number of time stamps that can be captured by this event capture unit. When this unit is in use, this value must be greater than 0. Once this number is reached, timestamps must be read before any new timestamps will be captured; should another capture be triggered before a timestamp is read, an overflow condition will occur and the newest value will be lost.



This value shall not be changed if any of the timestamp units are enabled. Data corruption can occur.



The sum of all MAX values in all Timestamp control registers must not exceed 16.

| Value | Description                                                         |
|-------|---------------------------------------------------------------------|
| 0     | Only valid when this event capture unit is disabled.                |
| 1–F   | Maximum number of time stamps allocated to this event capture unit. |

**Bits 8:7 – EDGE[1:0]** Capture Edge Selection

This value can only be changed when disabled.

| Value | Description             |
|-------|-------------------------|
| 00    | Capture on rising edge  |
| 01    | Capture on falling edge |
| 10    | Capture on both edges   |
| 11    | Reserved                |

**Bits 6:4 – SRC[2:0]** Capture Signal Source

This value can only be changed when disabled.

| Value   | Description                     |
|---------|---------------------------------|
| 000     | Receive pattern match from PHY  |
| 001     | Transmit pattern match from PHY |
| 010     | DIOA0 input                     |
| 011     | DIOA1 input                     |
| 100     | DIOA2 input                     |
| 101     | DIOA3 input                     |
| 110–111 | Reserved                        |

**Bit 3 – CLR** Clear event capture unit

Writing a 1 to this bit will reset this event capture status and stored timestamps. Control settings will not change.

| Value | Description                    |
|-------|--------------------------------|
| 0     | No effect                      |
| 1     | Reset this event capture unit. |

**Bit 1 – DA** Data Available

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | This capture unit has no timestamps available to be read. |
| 1     | This capture unit has timestamps available to be read.    |

**Bit 0 – EN** Event Capture Unit Enable

| Value | Description                          |
|-------|--------------------------------------|
| 0     | This event capture unit is disabled. |
| 1     | This event capture unit is enabled.  |

**11.6.14 Event Capture 2 Control Register****Name:** EC2CTRL**Address:** 0x0202

|        |         |     |          |     |     |     |     |         |
|--------|---------|-----|----------|-----|-----|-----|-----|---------|
| Bit    | 31      | 30  | 29       | 28  | 27  | 26  | 25  | 24      |
| Access | R/W     | R/W | R/W      | R/W | R/W | R/W | R/W | R/W     |
| Reset  | 0       | 0   | 0        | 0   | 0   | 0   | 0   | 0       |
| Bit    | 23      | 22  | 21       | 20  | 19  | 18  | 17  | 16      |
| Access | R/W     | R/W | R/W      | R/W | R/W | R/W | R/W | R/W     |
| Reset  | 0       | 0   | 0        | 0   | 0   | 0   | 0   | 0       |
| Bit    | 15      | 14  | 13       | 12  | 11  | 10  | 9   | 8       |
|        |         |     | MAX[3:0] |     |     |     |     | EDGE[1] |
| Access | R/W     | R/W | R/W      | R/W | R/W | RO  | RO  | R/W     |
| Reset  | 0       | 0   | 0        | 0   | 0   | 0   | 0   | 0       |
| Bit    | 7       | 6   | 5        | 4   | 3   | 2   | 1   | 0       |
|        | EDGE[0] |     | SRC[2:0] |     | CLR |     | DA  | EN      |
| Access | R/W     | R/W | R/W      | R/W | W1S | R/W | RO  | R/W     |
| Reset  | 0       | 0   | 0        | 0   | 0   | 0   | 0   | 0       |

**Bits 14:11 – MAX[3:0]** Maximum number of captured timestamps

This is the maximum number of time stamps that can be captured by this event capture unit. When this unit is in use, this value must be greater than 0. Once this number is reached, timestamps must be read before any new timestamps will be captured; should another capture be triggered before a timestamp is read, an overflow condition will occur and the newest value will be lost.

**DANGER**

This value shall not be changed if any of the timestamp units are enabled. Data corruption can occur.

**WARNING**

The sum of all MAX values in all Timestamp control registers must not exceed 16.

| Value | Description                                                         |
|-------|---------------------------------------------------------------------|
| 0     | Only valid when this event capture unit is disabled.                |
| 1–F   | Maximum number of time stamps allocated to this event capture unit. |

**Bits 8:7 – EDGE[1:0]** Capture Edge Selection**WARNING**

This value can only be changed when disabled.

| Value | Description             |
|-------|-------------------------|
| 00    | Capture on rising edge  |
| 01    | Capture on falling edge |
| 10    | Capture on both edges   |
| 11    | Reserved                |

**Bits 6:4 – SRC[2:0]** Capture Signal Source

This value can only be changed when disabled.

| Value   | Description                     |
|---------|---------------------------------|
| 000     | Receive pattern match from PHY  |
| 001     | Transmit pattern match from PHY |
| 010     | DIOA0 input                     |
| 011     | DIOA1 input                     |
| 100     | DIOA2 input                     |
| 101     | DIOA3 input                     |
| 110–111 | Reserved                        |

**Bit 3 – CLR** Clear capture unit

Writing a 1 to this bit will reset this event capture status and stored timestamps. Control settings will not change.

| Value | Description                    |
|-------|--------------------------------|
| 0     | No effect                      |
| 1     | Reset this event capture unit. |

**Bit 1 – DA** Data Available

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | This capture unit has no timestamps available to be read. |
| 1     | This capture unit has timestamps available to be read.    |

**Bit 0 – EN** Event Capture Unit Enable

| Value | Description                          |
|-------|--------------------------------------|
| 0     | This event capture unit is disabled. |
| 1     | This event capture unit is enabled.  |

**11.6.15 Event Capture 3 Control Register****Name:** EC3CTRL**Address:** 0x0203

|        |     |     |     |     |     |     |     |     |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| Access | R/W | R/W | R/W | R/W | R/W | RO  | RO  | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access | R/W | R/W | R/W | R/W | W1S | R/W | RO  | R/W |
| Reset  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 14:11 – MAX[3:0]** Maximum number of captured timestamps

This is the maximum number of time stamps that can be captured by this event capture unit. When this unit is in use, this value must be greater than 0. Once this number is reached, timestamps must be read before any new timestamps will be captured; should another capture be triggered before a timestamp is read, an overflow condition will occur and the newest value will be lost.

**DANGER**

This value shall not be changed if any of the timestamp units are enabled. Data corruption can occur.

**WARNING**

The sum of all MAX values in all Timestamp control registers must not exceed 16.

| Value | Description                                                         |
|-------|---------------------------------------------------------------------|
| 0     | Only valid when this event capture unit is disabled.                |
| 1–F   | Maximum number of time stamps allocated to this event capture unit. |

**Bits 8:7 – EDGE[1:0]** Capture Edge Selection**WARNING**

This value can only be changed when disabled.

| Value | Description             |
|-------|-------------------------|
| 00    | Capture on rising edge  |
| 01    | Capture on falling edge |
| 10    | Capture on both edges   |
| 11    | Reserved                |

**Bits 6:4 – SRC[2:0]** Capture Signal Source

This value can only be changed when disabled.

| Value   | Description                     |
|---------|---------------------------------|
| 000     | Receive pattern match from PHY  |
| 001     | Transmit pattern match from PHY |
| 010     | DIOA0 input                     |
| 011     | DIOA1 input                     |
| 100     | DIOA2 input                     |
| 101     | DIOA3 input                     |
| 110–111 | Reserved                        |

**Bit 3 – CLR** Clear event capture unit

Writing a 1 to this bit will reset this event capture status and stored timestamps. Control settings will not change.

| Value | Description                    |
|-------|--------------------------------|
| 0     | No effect                      |
| 1     | Reset this event capture unit. |

**Bit 1 – DA** Data Available

| Value | Description                                               |
|-------|-----------------------------------------------------------|
| 0     | This capture unit has no timestamps available to be read. |
| 1     | This capture unit has timestamps available to be read.    |

**Bit 0 – EN** Event Capture Unit Enable

| Value | Description                          |
|-------|--------------------------------------|
| 0     | This event capture unit is disabled. |
| 1     | This event capture unit is enabled.  |



### 11.6.16 Event Capture Read Status Register

**Name:** ECRDSTS**Address:** 0x0204

Contains the status of all of the event capture data registers since the last time this register was read. Any time that this register is read, the current state, including wall clock time, is saved and can be read from the following event capture registers.



**Important:** Since the event time stamps only have 2 bits representing seconds, this register must be read while the oldest time stamp can still be calculated from the captured wall clock.

|        |            |    |       |       |            |       |    |    |
|--------|------------|----|-------|-------|------------|-------|----|----|
| Bit    | 31         | 30 | 29    | 28    | 27         | 26    | 25 | 24 |
|        |            |    | EC3OV | EC2OV | EC1OV      | EC0OV |    |    |
| Access | RO         | RO | RO    | RO    | RO         | RO    | RO | RO |
| Reset  | 0          | 0  | 0     | 0     | 0          | 0     | 0  | 0  |
| Bit    | 23         | 22 | 21    | 20    | 19         | 18    | 17 | 16 |
|        |            |    |       |       |            |       |    |    |
| Access | RO         | RO | RO    | RO    | RO         | RO    | RO | RO |
| Reset  | 0          | 0  | 0     | 0     | 0          | 0     | 0  | 0  |
| Bit    | 15         | 14 | 13    | 12    | 11         | 10    | 9  | 8  |
|        | EC3CT[3:0] |    |       |       | EC2CT[3:0] |       |    |    |
| Access | RO         | RO | RO    | RO    | RO         | RO    | RO | RO |
| Reset  | 0          | 0  | 0     | 0     | 0          | 0     | 0  | 0  |
| Bit    | 7          | 6  | 5     | 4     | 3          | 2     | 1  | 0  |
|        | EC1CT[3:0] |    |       |       | EC0CT[3:0] |       |    |    |
| Access | RO         | RO | RO    | RO    | RO         | RO    | RO | RO |
| Reset  | 0          | 0  | 0     | 0     | 0          | 0     | 0  | 0  |

#### Bit 29 – EC3OV Event capture unit 3 overflow

| Value | Description                                                                      |
|-------|----------------------------------------------------------------------------------|
| 0     | Event capture unit 3 has not overflowed.                                         |
| 1     | Event capture unit 3 has overflowed and missed capturing at least one timestamp. |

#### Bit 28 – EC2OV Event capture unit 2 overflow

| Value | Description                                                                      |
|-------|----------------------------------------------------------------------------------|
| 0     | Event capture unit 2 has not overflowed.                                         |
| 1     | Event capture unit 2 has overflowed and missed capturing at least one timestamp. |

#### Bit 27 – EC1OV Event capture unit 1 overflow

| Value | Description                                                                      |
|-------|----------------------------------------------------------------------------------|
| 0     | Event capture unit 1 has not overflowed.                                         |
| 1     | Event capture unit 1 has overflowed and missed capturing at least one timestamp. |

#### Bit 26 – EC0OV Event capture unit 0 overflow

| Value | Description                                                                      |
|-------|----------------------------------------------------------------------------------|
| 0     | Event capture unit 0 has not overflowed.                                         |
| 1     | Event capture unit 0 has overflowed and missed capturing at least one timestamp. |

**Bits 15:12 – EC3CT[3:0]** Event capture unit 3 timestamp count

| Value | Description                                                                           |
|-------|---------------------------------------------------------------------------------------|
| 0 – F | Number of valid time stamps currently available for reading from event capture unit 3 |

**Bits 11:8 – EC2CT[3:0]** Event capture unit 2 timestamp count

| Value | Description                                                                           |
|-------|---------------------------------------------------------------------------------------|
| 0 – F | Number of valid time stamps currently available for reading from event capture unit 2 |

**Bits 7:4 – EC1CT[3:0]** Event capture unit 1 timestamp count

| Value | Description                                                                           |
|-------|---------------------------------------------------------------------------------------|
| 0 – F | Number of valid time stamps currently available for reading from event capture unit 1 |

**Bits 3:0 – EC0CT[3:0]** Event capture unit 0 timestamp count

| Value | Description                                                                           |
|-------|---------------------------------------------------------------------------------------|
| 0 – F | Number of valid time stamps currently available for reading from event capture unit 0 |

**11.6.17 Event Capture Total Counts Register**

**Name:** ECTOT  
**Address:** 0x0205

This register contains the total number of timestamps captured by each of the event capture units. The counts are reloaded every time ECRDSTS is read. The counts will roll over to 0 after 255. A count is cleared only when the timestamp is disabled or cleared.

|        |             |    |    |    |    |    |    |    |
|--------|-------------|----|----|----|----|----|----|----|
| Bit    | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | EC3TOT[7:0] |    |    |    |    |    |    |    |
| Access | RO          | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | EC2TOT[7:0] |    |    |    |    |    |    |    |
| Access | RO          | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | EC1TOT[7:0] |    |    |    |    |    |    |    |
| Access | RO          | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | EC0TOT[7:0] |    |    |    |    |    |    |    |
| Access | RO          | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:24 – EC3TOT[7:0] Event Capture 3 Total**  
 [bitFieldDescription]

| Value | Description                                                 |
|-------|-------------------------------------------------------------|
| 0–FF  | Total number of timestamps captured by event capture unit 3 |

**Bits 23:16 – EC2TOT[7:0] Event Capture 2 Total**

| Value | Description                                                 |
|-------|-------------------------------------------------------------|
| 0–FF  | Total number of timestamps captured by event capture unit 2 |

**Bits 15:8 – EC1TOT[7:0] Event Capture 1 Total**

| Value | Description                                                 |
|-------|-------------------------------------------------------------|
| 0–FF  | Total number of timestamps captured by event capture unit 1 |

**Bits 7:0 – EC0TOT[7:0] Event Capture 0 Total**

| Value | Description                                                 |
|-------|-------------------------------------------------------------|
| 0–FF  | Total number of timestamps captured by event capture unit 0 |

**11.6.18 Event Capture Clock Seconds High Register****Name:** ECCLKSH**Address:** 0x0206

|        |               |    |    |    |    |    |    |    |
|--------|---------------|----|----|----|----|----|----|----|
| Bit    | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        |               |    |    |    |    |    |    |    |
| Access | RO            | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        |               |    |    |    |    |    |    |    |
| Access | RO            | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | CLKSEC[47:40] |    |    |    |    |    |    |    |
| Access | RO            | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | CLKSEC[39:32] |    |    |    |    |    |    |    |
| Access | RO            | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 15:0 – CLKSEC[47:32]** Clock time in seconds

This field contains the upper 16 bits of the seconds portion of the clock time which was stored when the Event Capture Read Status Register (ECRDSTS) register was last read. These bits do not appear in the 64 bit format used in the SPI timestamp protocol. See 64-Bit Timestamp Format for more information.

**11.6.19 Event Capture Clock Seconds Low Register****Name:** ECCLKSL**Address:** 0x0207

|        |               |    |    |    |    |    |    |    |
|--------|---------------|----|----|----|----|----|----|----|
| Bit    | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|        | CLKSEC[31:24] |    |    |    |    |    |    |    |
| Access | RO            | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|        | CLKSEC[23:16] |    |    |    |    |    |    |    |
| Access | RO            | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
|        | CLKSEC[15:8]  |    |    |    |    |    |    |    |
| Access | RO            | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|        | CLKSEC[7:0]   |    |    |    |    |    |    |    |
| Access | RO            | RO | RO | RO | RO | RO | RO | RO |
| Reset  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Bits 31:0 – CLKSEC[31:0]** Clock time in seconds

This field contains the lower 32 bits of the seconds portion of the clock time which was stored when the Event Capture Read Status Register (ECRDSTS) register was last read. See 64-Bit Timestamp Format for more information

**11.6.20 Event Capture Clock Nanoseconds Register****Name:** ECCLKNS**Address:** 0x0208

|        |                 |     |     |     |     |     |     |     |
|--------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31              | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | CLOCK_NS[29:24] |     |     |     |     |     |     |     |
| Access | RO              | RO  | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0               | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23              | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | CLOCK_NS[23:16] |     |     |     |     |     |     |     |
| Access | R/W             | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0               | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15              | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | CLOCK_NS[15:8]  |     |     |     |     |     |     |     |
| Access | R/W             | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0               | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7               | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | CLOCK_NS[7:0]   |     |     |     |     |     |     |     |
| Access | R/W             | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0               | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – CLOCK\_NS[29:0]** Clock time in nanoseconds

This field contains the nanoseconds portion of the clock time which was stored when the Event Capture Read Status Register (ECDSTS) register was last read.

**11.6.21 Event Capture Read Timestamp Register n****Name:** ECRDTSn**Address:** 0x0209, 0x20A, 0x20B, 0x20C, 0x20D, 0x20E, 0x20F, 0x210, 0x211, 0x212, 0x213, 0x214, 0x215, 0x216, 0x217, 0x218

These registers are read to obtain the timestamps stored by the event capture units when the ECRDSTS register was last read. These values must be combined with the ECCLK registers to obtain the clock time of the timestamp. See the Event Capture section for a description of register allocation among the event capture units.

**Note:** When the register does not contain a valid timestamp it will read back as 0xFFFF\_FFFF.

|        |             |    |             |    |    |    |    |    |
|--------|-------------|----|-------------|----|----|----|----|----|
| Bit    | 31          | 30 | 29          | 28 | 27 | 26 | 25 | 24 |
|        | TSSEC[1:0]  |    | TSNS[29:24] |    |    |    |    |    |
| Access | RO          | RO | RO          | RO | RO | RO | RO | RO |
| Reset  | 0           | 0  | 0           | 0  | 0  | 0  | 0  | 0  |
| Bit    | 23          | 22 | 21          | 20 | 19 | 18 | 17 | 16 |
|        | TSNS[23:16] |    |             |    |    |    |    |    |
| Access | RO          | RO | RO          | RO | RO | RO | RO | RO |
| Reset  | 0           | 0  | 0           | 0  | 0  | 0  | 0  | 0  |
| Bit    | 15          | 14 | 13          | 12 | 11 | 10 | 9  | 8  |
|        | TSNS[15:8]  |    |             |    |    |    |    |    |
| Access | RO          | RO | RO          | RO | RO | RO | RO | RO |
| Reset  | 0           | 0  | 0           | 0  | 0  | 0  | 0  | 0  |
| Bit    | 7           | 6  | 5           | 4  | 3  | 2  | 1  | 0  |
|        | TSNS[7:0]   |    |             |    |    |    |    |    |
| Access | RO          | RO | RO          | RO | RO | RO | RO | RO |
| Reset  | 0           | 0  | 0           | 0  | 0  | 0  | 0  | 0  |

**Bits 31:30 – TSSEC[1:0]** Timestamp Seconds

This 2-bit field contains the seconds portion of the saved timestamp.

**Bits 29:0 – TSNS[29:0]** Timestamp Nanoseconds

This bitfield contains the nanosecond portion of the saved timestamp.

## 11.6.22 Phase Adjuster Cycles Register

**Name:** PACYC  
**Address:** 0x021F

|        |            |     |            |     |     |     |     |     |
|--------|------------|-----|------------|-----|-----|-----|-----|-----|
| Bit    | 31         | 30  | 29         | 28  | 27  | 26  | 25  | 24  |
|        |            |     | CYC[29:24] |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23         | 22  | 21         | 20  | 19  | 18  | 17  | 16  |
|        | CYC[23:16] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15         | 14  | 13         | 12  | 11  | 10  | 9   | 8   |
|        | CYC[15:8]  |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5          | 4   | 3   | 2   | 1   | 0   |
|        | CYC[7:0]   |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |

### Bits 29:0 – CYC[29:0]

| Value                  | Description                                       |
|------------------------|---------------------------------------------------|
| 0 –<br>0x3FFF_FF<br>FF | Number of clock cycles between phase adjustments. |



### 11.6.23 Phase Adjuster Control Register

**Name:** PACTRL**Address:** 0x0220

No bit in this register shall be modified while the phase adjust is active.

|        |          |     |     |     |     |     |          |     |
|--------|----------|-----|-----|-----|-----|-----|----------|-----|
| Bit    | 31       | 30  | 29  | 28  | 27  | 26  | 25       | 24  |
|        | ACT      | SEC | DEC |     |     |     |          |     |
| Access | W1S      | R/W | R/W | R/W | R/W | R/W | R/W      | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0        | 0   |
| Bit    | 23       | 22  | 21  | 20  | 19  | 18  | 17       | 16  |
|        |          |     |     |     |     |     |          |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W      | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0        | 0   |
| Bit    | 15       | 14  | 13  | 12  | 11  | 10  | 9        | 8   |
|        |          |     |     |     |     |     | DIF[9:8] |     |
| Access |          |     |     |     |     |     | R/W      | R/W |
| Reset  |          |     |     |     |     |     | 0        | 0   |
| Bit    | 7        | 6   | 5   | 4   | 3   | 2   | 1        | 0   |
|        | DIF[7:0] |     |     |     |     |     |          |     |
| Access | R/W      | R/W | R/W | R/W | R/W | R/W | R/W      | R/W |
| Reset  | 0        | 0   | 0   | 0   | 0   | 0   | 0        | 0   |

**Bit 31 – ACT** Phase adjust active

Writing a 1 to this bit will start the phase adjust. Once started, this bit will read back as 1 until the phase adjustment is complete. At completion, hardware will reset this bit to 0.

**Bit 30 – SEC** Units are seconds

| Value | Description                                                     |
|-------|-----------------------------------------------------------------|
| 0     | Increment or decrement the nanosecond portion of the wall clock |
| 1     | Increment the second portion of the wall clock.                 |

**Bit 29 – DEC** Decrement

| Value | Description                                                                               |
|-------|-------------------------------------------------------------------------------------------|
| 0     | Increment the wall clock nanosecond or second field.                                      |
| 1     | Decrement the wall clock nanosecond field. This value is not valid if the SEC field is 1. |

**Bits 9:0 – DIF[9:0]** Time difference

| Value   | Description                                                                                           |
|---------|-------------------------------------------------------------------------------------------------------|
| 0 – 3FF | The total number of reference clock cycles during which the wall clock is incremented or decremented. |

**11.6.24 Event 0 Start Time Nanoseconds Register****Name:** EG0STNS**Address:** 0x0221

|        |            |     |            |     |     |     |     |     |
|--------|------------|-----|------------|-----|-----|-----|-----|-----|
| Bit    | 31         | 30  | 29         | 28  | 27  | 26  | 25  | 24  |
|        |            |     | STNS[30:0] |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23         | 22  | 21         | 20  | 19  | 18  | 17  | 16  |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15         | 14  | 13         | 12  | 11  | 10  | 9   | 8   |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5          | 4   | 3   | 2   | 1   | 0   |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – STNS[30:0]** Pulse Start Time in Nanoseconds

This field contains the nanosecond portion of the start time.

**11.6.25 Event 0 Start Time Seconds Low Register****Name:** EG0STSECL**Address:** 0x0222

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31           | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | STSEC[31:24] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23           | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | STSEC[23:16] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STSEC[15:8]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STSEC[7:0]   |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – STSEC[31:0] Start Time in Seconds**

This field contains the lower 32 bits of the seconds portion of the pulse start time.

**11.6.26 Event 0 Start Time Seconds High Register****Name:** EG0STSECH**Address:** 0x0223

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31           | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23           | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STSEC[47:40] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STSEC[39:32] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:0 – STSEC[47:32] Start Time in Seconds**

This field contains upper 16 bits of the seconds portion of the pulse start time.

**Note:** These bits are not included in the 64 bit timestamp format used in the SPI timestamp protocol.

**11.6.27 Event 0 Pulse Width Register****Name:** EG0PW**Address:** 0x0224

|        |           |     |     |     |     |     |     |     |
|--------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | PW[29:24] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | PW[23:16] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | PW[15:8]  |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | PW[7:0]   |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – PW[29:0] Pulse Width in Nanoseconds**

This field contains duration (in nanoseconds) that the pulse is asserted. If this value is 0, the output is toggled at the start time and remains constant for the idle time.

**11.6.28 Event 0 Idle Time Register**

**Name:** EGOIT  
**Address:** 0x0225

|        |           |     |           |     |     |     |     |     |
|--------|-----------|-----|-----------|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29        | 28  | 27  | 26  | 25  | 24  |
|        |           |     | IT[29:24] |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21        | 20  | 19  | 18  | 17  | 16  |
|        | IT[23:16] |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13        | 12  | 11  | 10  | 9   | 8   |
|        | IT[15:8]  |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5         | 4   | 3   | 2   | 1   | 0   |
|        | IT[7:0]   |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – IT[29:0] Idle Time in Nanoseconds**

This field contains the time that the pulse is deasserted. If the pulse is configured as repeating, the signal will be reasserted at the completion of this time. A reasserting pulse with pulse width of 0 will toggle again at the end of the idle time. The event is always marked as done at the end of the last idle time.

**11.6.29 Event Generator 0 Control Register**

**Name:** EGOCTL  
**Address:** 0x0226

|        |    |    |     |       |     |    |      |       |
|--------|----|----|-----|-------|-----|----|------|-------|
| Bit    | 31 | 30 | 29  | 28    | 27  | 26 | 25   | 24    |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 23 | 22 | 21  | 20    | 19  | 18 | 17   | 16    |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 15 | 14 | 13  | 12    | 11  | 10 | 9    | 8     |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 7  | 6  | 5   | 4     | 3   | 2  | 1    | 0     |
| Access | RO | RO | R/W | ISREL | REP | AH | STOP | START |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |

**Bit 4 – ISREL** Event Uses Relative Timing

| Value | Description                                                                        |
|-------|------------------------------------------------------------------------------------|
| 0     | Event start time is an absolute time.                                              |
| 1     | Event start time is relative to the wall clock time when the START bit is written. |

**Bit 3 – REP** Event Repeats Periodically

| Value | Description                                                               |
|-------|---------------------------------------------------------------------------|
| 0     | Event occurs once.                                                        |
| 1     | Event repeats periodically. The period equals pulse width plus idle time. |

**Bit 2 – AH** Event Output is Active High

**Note:** This bit has no effect if pulse width = 0 (toggle mode).

| Value | Description                                                                                                                                                     |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Event is active low - signal will be driven low at event start for the duration of the pulse width, then will transition to and remain low for the idle time.   |
| 1     | Event is active high - signal will be driven high at event start for the duration of the pulse width, then will transition to and remain low for the idle time. |

**Bit 1 – STOP** Stop Event

**Note:** Only events with REPEAT=1 need to be stopped.

| Value | Description                                                                                                                             |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0     | No effect                                                                                                                               |
| 1     | Stop repeating pulses at the end of the next idle time. The output will remain at the idle value and event done status bit will be set. |

**Bit 0 – START** Start Event

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | No effect                                    |
| 1     | Start the event configured in this register. |

**11.6.30 Event 1 Start Time Nanoseconds Register****Name:** EG1STNS**Address:** 0x0227

|        |            |     |            |     |     |     |     |     |
|--------|------------|-----|------------|-----|-----|-----|-----|-----|
| Bit    | 31         | 30  | 29         | 28  | 27  | 26  | 25  | 24  |
|        |            |     | STNS[30:0] |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23         | 22  | 21         | 20  | 19  | 18  | 17  | 16  |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15         | 14  | 13         | 12  | 11  | 10  | 9   | 8   |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5          | 4   | 3   | 2   | 1   | 0   |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – STNS[30:0]** Pulse Start Time in Nanoseconds

This field contains the nanosecond portion of the start time.



**11.6.31 Event 1 Start Time Seconds Low Register****Name:** EG1STSECL**Address:** 0x0228

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31           | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | STSEC[31:24] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23           | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | STSEC[23:16] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STSEC[15:8]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STSEC[7:0]   |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – STSEC[31:0] Start Time in Seconds**

This field contains the lower 32 bits of the seconds portion of the pulse start time.

## 11.6.32 Event 1 Start Time Seconds High Register

**Name:** EG1STSECH

**Address:** 0x0229

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31           | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23           | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STSEC[47:40] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STSEC[39:32] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

### Bits 15:0 – STSEC[47:32] Start Time in Seconds

This field contains upper 16 bits of the seconds portion of the pulse start time.

**Note:** These bits are not included in the 64 bit timestamp format used in the SPI timestamp protocol.

**11.6.33 Event 1 Pulse Width Register****Name:** EG1PW**Address:** 0x022A

|        |           |     |     |     |     |     |     |     |
|--------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | PW[29:24] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | PW[23:16] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | PW[15:8]  |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | PW[7:0]   |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – PW[29:0] Pulse Width in Nanoseconds**

This field contains duration (in nanoseconds) that the pulse is asserted. If this value is 0, the output is toggled at the start time and remains constant for the idle time.

**11.6.34 Event 1 Idle Time Register**

**Name:** EG1IT  
**Address:** 0x022B

|        |           |     |           |     |     |     |     |     |
|--------|-----------|-----|-----------|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29        | 28  | 27  | 26  | 25  | 24  |
|        |           |     | IT[29:24] |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21        | 20  | 19  | 18  | 17  | 16  |
|        | IT[23:16] |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13        | 12  | 11  | 10  | 9   | 8   |
|        | IT[15:8]  |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5         | 4   | 3   | 2   | 1   | 0   |
|        | IT[7:0]   |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – IT[29:0] Idle Time in Nanoseconds**

This field contains the time that the pulse is deasserted. If the pulse is configured as repeating, the signal will be reasserted at the completion of this time. A reasserting pulse with pulse width of 0 will toggle again at the end of the idle time. The event is always marked as done at the end of the last idle time.

**11.6.35 Event Generator 1 Control Register****Name:** EG1CTL**Address:** 0x022C

|        |    |    |     |       |     |    |      |       |
|--------|----|----|-----|-------|-----|----|------|-------|
| Bit    | 31 | 30 | 29  | 28    | 27  | 26 | 25   | 24    |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 23 | 22 | 21  | 20    | 19  | 18 | 17   | 16    |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 15 | 14 | 13  | 12    | 11  | 10 | 9    | 8     |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 7  | 6  | 5   | 4     | 3   | 2  | 1    | 0     |
| Access | RO | RO | R/W | ISREL | REP | AH | STOP | START |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |

**Bit 4 – ISREL** Event Uses Relative Timing

| Value | Description                                                                        |
|-------|------------------------------------------------------------------------------------|
| 0     | Event start time is an absolute time.                                              |
| 1     | Event start time is relative to the wall clock time when the START bit is written. |

**Bit 3 – REP** Event Repeats Periodically

| Value | Description                                                               |
|-------|---------------------------------------------------------------------------|
| 0     | Event occurs once.                                                        |
| 1     | Event repeats periodically. The period equals pulse width plus idle time. |

**Bit 2 – AH** Event Output is Active High**Note:** This bit has no effect if pulse width = 0 (toggle mode).

| Value | Description                                                                                                                                                     |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Event is active low - signal will be driven low at event start for the duration of the pulse width, then will transition to and remain low for the idle time.   |
| 1     | Event is active high - signal will be driven high at event start for the duration of the pulse width, then will transition to and remain low for the idle time. |

**Bit 1 – STOP** Stop Event**Note:** Only events with REPEAT=1 need to be stopped.

| Value | Description                                                                                                                             |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0     | No effect                                                                                                                               |
| 1     | Stop repeating pulses at the end of the next idle time. The output will remain at the idle value and event done status bit will be set. |

**Bit 0 – START** Start Event

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | No effect                                    |
| 1     | Start the event configured in this register. |

### 11.6.36 Event 2 Start Time Nanoseconds Register

**Name:** EG2STNS

**Address:** 0x022D

|        |            |     |            |     |     |     |     |     |
|--------|------------|-----|------------|-----|-----|-----|-----|-----|
| Bit    | 31         | 30  | 29         | 28  | 27  | 26  | 25  | 24  |
|        |            |     | STNS[30:0] |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23         | 22  | 21         | 20  | 19  | 18  | 17  | 16  |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15         | 14  | 13         | 12  | 11  | 10  | 9   | 8   |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5          | 4   | 3   | 2   | 1   | 0   |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – STNS[30:0]** Pulse Start Time in Nanoseconds

This field contains the nanosecond portion of the start time.

**11.6.37 Event 2 Start Time Seconds Low Register****Name:** EG2STSECL**Address:** 0x022E

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31           | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | STSEC[31:24] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23           | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | STSEC[23:16] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STSEC[15:8]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STSEC[7:0]   |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – STSEC[31:0] Start Time in Seconds**

This field contains the lower 32 bits of the seconds portion of the pulse start time.

**11.6.38 Event 2 Start Time Seconds High Register****Name:** EG2STSECH**Address:** 0x022F

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31           | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23           | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STSEC[47:40] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STSEC[39:32] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:0 – STSEC[47:32] Start Time in Seconds**

This field contains upper 16 bits of the seconds portion of the pulse start time.

**Note:** These bits are not included in the 64 bit timestamp format used in the SPI timestamp protocol.



**11.6.39 Event 2 Pulse Width Register****Name:** EG2PW**Address:** 0x0230

|        |           |     |     |     |     |     |     |     |
|--------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | PW[29:24] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | PW[23:16] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | PW[15:8]  |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | PW[7:0]   |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – PW[29:0] Pulse Width in Nanoseconds**

This field contains duration (in nanoseconds) that the pulse is asserted. If this value is 0, the output is toggled at the start time and remains constant for the idle time.

**11.6.40 Event 2 Idle Time Register**

**Name:** EG2IT  
**Address:** 0x0231

|        |           |     |           |     |     |     |     |     |
|--------|-----------|-----|-----------|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29        | 28  | 27  | 26  | 25  | 24  |
|        |           |     | IT[29:24] |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21        | 20  | 19  | 18  | 17  | 16  |
|        | IT[23:16] |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13        | 12  | 11  | 10  | 9   | 8   |
|        | IT[15:8]  |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5         | 4   | 3   | 2   | 1   | 0   |
|        | IT[7:0]   |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – IT[29:0] Idle Time in Nanoseconds**

This field contains the time that the pulse is deasserted. If the pulse is configured as repeating, the signal will be reasserted at the completion of this time. A reasserting pulse with pulse width of 0 will toggle again at the end of the idle time. The event is always marked as done at the end of the last idle time.

**11.6.41 Event Generator 2 Control Register****Name:** EG2CTL**Address:** 0x0232

|        |    |    |     |       |     |    |      |       |
|--------|----|----|-----|-------|-----|----|------|-------|
| Bit    | 31 | 30 | 29  | 28    | 27  | 26 | 25   | 24    |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 23 | 22 | 21  | 20    | 19  | 18 | 17   | 16    |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 15 | 14 | 13  | 12    | 11  | 10 | 9    | 8     |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 7  | 6  | 5   | 4     | 3   | 2  | 1    | 0     |
| Access | RO | RO | R/W | ISREL | REP | AH | STOP | START |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |

**Bit 4 – ISREL** Event Uses Relative Timing

| Value | Description                                                                        |
|-------|------------------------------------------------------------------------------------|
| 0     | Event start time is an absolute time.                                              |
| 1     | Event start time is relative to the wall clock time when the START bit is written. |

**Bit 3 – REP** Event Repeats Periodically

| Value | Description                                                               |
|-------|---------------------------------------------------------------------------|
| 0     | Event occurs once.                                                        |
| 1     | Event repeats periodically. The period equals pulse width plus idle time. |

**Bit 2 – AH** Event Output is Active High**Note:** This bit has no effect if pulse width = 0 (toggle mode).

| Value | Description                                                                                                                                                     |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Event is active low - signal will be driven low at event start for the duration of the pulse width, then will transition to and remain low for the idle time.   |
| 1     | Event is active high - signal will be driven high at event start for the duration of the pulse width, then will transition to and remain low for the idle time. |

**Bit 1 – STOP** Stop Event**Note:** Only events with REPEAT=1 need to be stopped.

| Value | Description                                                                                                                             |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0     | No effect                                                                                                                               |
| 1     | Stop repeating pulses at the end of the next idle time. The output will remain at the idle value and event done status bit will be set. |

**Bit 0 – START** Start Event

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | No effect                                    |
| 1     | Start the event configured in this register. |

## 11.6.42 Event 3 Start Time Nanoseconds Register

**Name:** EG3STNS

**Address:** 0x0233

|        |            |     |            |     |     |     |     |     |
|--------|------------|-----|------------|-----|-----|-----|-----|-----|
| Bit    | 31         | 30  | 29         | 28  | 27  | 26  | 25  | 24  |
|        |            |     | STNS[30:0] |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23         | 22  | 21         | 20  | 19  | 18  | 17  | 16  |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15         | 14  | 13         | 12  | 11  | 10  | 9   | 8   |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7          | 6   | 5          | 4   | 3   | 2   | 1   | 0   |
|        | STNS[30:0] |     |            |     |     |     |     |     |
| Access | R/W        | R/W | R/W        | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0          | 0   | 0          | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – STNS[30:0]** Pulse Start Time in Nanoseconds

This field contains the nanosecond portion of the start time.

**11.6.43 Event 3 Start Time Seconds Low Register****Name:** EG3STSECL**Address:** 0x0234

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31           | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | STSEC[31:24] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23           | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | STSEC[23:16] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STSEC[15:8]  |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STSEC[7:0]   |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 31:0 – STSEC[31:0] Start Time in Seconds**

This field contains the lower 32 bits of the seconds portion of the pulse start time.

**11.6.44 Event 3 Start Time Seconds High Register****Name:** EG3STSECH**Address:** 0x0235

|        |              |     |     |     |     |     |     |     |
|--------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31           | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23           | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15           | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | STSEC[47:40] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7            | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | STSEC[39:32] |     |     |     |     |     |     |     |
| Access | R/W          | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 15:0 – STSEC[47:32] Start Time in Seconds**

This field contains upper 16 bits of the seconds portion of the pulse start time.

**Note:** These bits are not included in the 64 bit timestamp format used in the SPI timestamp protocol.

**11.6.45 Event 3 Pulse Width Register****Name:** EG3PW**Address:** 0x0236

|        |           |     |     |     |     |     |     |     |
|--------|-----------|-----|-----|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|        | PW[29:24] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
|        | PW[23:16] |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|        | PW[15:8]  |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|        | PW[7:0]   |     |     |     |     |     |     |     |
| Access | R/W       | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – PW[29:0]** Pulse Width in Nanoseconds

This field contains duration (in nanoseconds) that the pulse is asserted. If this value is 0, the output is toggled at the start time and remains constant for the idle time.

**11.6.46 Event 3 Idle Time Register**

**Name:** EG3IT  
**Address:** 0x0237

|        |           |     |           |     |     |     |     |     |
|--------|-----------|-----|-----------|-----|-----|-----|-----|-----|
| Bit    | 31        | 30  | 29        | 28  | 27  | 26  | 25  | 24  |
|        |           |     | IT[29:24] |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 23        | 22  | 21        | 20  | 19  | 18  | 17  | 16  |
|        | IT[23:16] |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 15        | 14  | 13        | 12  | 11  | 10  | 9   | 8   |
|        | IT[15:8]  |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |
| Bit    | 7         | 6   | 5         | 4   | 3   | 2   | 1   | 0   |
|        | IT[7:0]   |     |           |     |     |     |     |     |
| Access | R/W       | R/W | R/W       | R/W | R/W | R/W | R/W | R/W |
| Reset  | 0         | 0   | 0         | 0   | 0   | 0   | 0   | 0   |

**Bits 29:0 – IT[29:0] Idle Time in Nanoseconds**

This field contains the time that the pulse is deasserted. If the pulse is configured as repeating, the signal will be reasserted at the completion of this time. A reasserting pulse with pulse width of 0 will toggle again at the end of the idle time. The event is always marked as done at the end of the last idle time.



**11.6.47 Event Generator 3 Control Register****Name:** EG3CTL**Address:** 0x0238

|        |    |    |     |       |     |    |      |       |
|--------|----|----|-----|-------|-----|----|------|-------|
| Bit    | 31 | 30 | 29  | 28    | 27  | 26 | 25   | 24    |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 23 | 22 | 21  | 20    | 19  | 18 | 17   | 16    |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 15 | 14 | 13  | 12    | 11  | 10 | 9    | 8     |
| Access | RO | RO | RO  | RO    | RO  | RO | RO   | RO    |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |
| Bit    | 7  | 6  | 5   | 4     | 3   | 2  | 1    | 0     |
| Access | RO | RO | R/W | ISREL | REP | AH | STOP | START |
| Reset  | 0  | 0  | 0   | 0     | 0   | 0  | 0    | 0     |

**Bit 4 – ISREL** Event Uses Relative Timing

| Value | Description                                                                        |
|-------|------------------------------------------------------------------------------------|
| 0     | Event start time is an absolute time.                                              |
| 1     | Event start time is relative to the wall clock time when the START bit is written. |

**Bit 3 – REP** Event Repeats Periodically

| Value | Description                                                               |
|-------|---------------------------------------------------------------------------|
| 0     | Event occurs once.                                                        |
| 1     | Event repeats periodically. The period equals pulse width plus idle time. |

**Bit 2 – AH** Event Output is Active High**Note:** This bit has no effect if pulse width = 0 (toggle mode).

| Value | Description                                                                                                                                                     |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Event is active low - signal will be driven low at event start for the duration of the pulse width, then will transition to and remain low for the idle time.   |
| 1     | Event is active high - signal will be driven high at event start for the duration of the pulse width, then will transition to and remain low for the idle time. |

**Bit 1 – STOP** Stop Event**Note:** Only events with REPEAT=1 need to be stopped.

| Value | Description                                                                                                                             |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0     | No effect                                                                                                                               |
| 1     | Stop repeating pulses at the end of the next idle time. The output will remain at the idle value and event done status bit will be set. |

**Bit 0 – START** Start Event

| Value | Description                                  |
|-------|----------------------------------------------|
| 0     | No effect                                    |
| 1     | Start the event configured in this register. |

**11.6.48 One Pulse-per-Second Control Register****Name:** PPSCTL**Address:** 0x0239

|        |    |            |    |    |    |    |        |       |
|--------|----|------------|----|----|----|----|--------|-------|
| Bit    | 31 | 30         | 29 | 28 | 27 | 26 | 25     | 24    |
|        |    |            |    |    |    |    |        |       |
| Access |    |            |    |    |    |    |        |       |
| Reset  |    |            |    |    |    |    |        |       |
| Bit    | 23 | 22         | 21 | 20 | 19 | 18 | 17     | 16    |
|        |    |            |    |    |    |    |        |       |
| Access |    |            |    |    |    |    |        |       |
| Reset  |    |            |    |    |    |    |        |       |
| Bit    | 15 | 14         | 13 | 12 | 11 | 10 | 9      | 8     |
|        |    |            |    |    |    |    |        |       |
| Access |    |            |    |    |    |    |        |       |
| Reset  |    |            |    |    |    |    |        |       |
| Bit    | 7  | 6          | 5  | 4  | 3  | 2  | 1      | 0     |
|        |    | PPSPW[4:0] |    |    |    |    | PPSDIS | PPSEN |
| Access |    | RW         | RW | RW | RW | RW | W1S    | W1S   |
| Reset  |    | 0          | 0  | 0  | 0  | 1  | 0      | 0     |

**Bits 6:2 – PPSPW[4:0]** Pulse-per-second pulse width

This field sets the 1PPS pulse width based on the 40 nanosecond period of the time stamp clock.

**Equation 11-1.** 1PPS Pulse Width

$$Pulse\_width = 16 \times (PPS\_WIDTH + 1) \times 40\ ns$$

The default value of 0 corresponds a pulse width of 640ns.

**Bit 1 – PPSDIS** 1 pulse-per-second signal disable

Writing 1 to this bit field will cause generation of 1 pulse-per-second to stop at the end of the active one second period. The PPSDONE bit in the SEVSTS register will also be set when the signal generation stops.

**Bit 0 – PPSEN** 1 pulse-per-second signal enable

Writing a 1 starts generation of 1 pulse-per-second signal

**11.6.49 Synchronization Event Interrupt Enable Register****Name:** SEVINTEN**Address:** 0x023A**Note:** All bits of this register are W1S.

|        |        |         |    |    |    |    |    |    |
|--------|--------|---------|----|----|----|----|----|----|
| Bit    | 31     | 30      | 29 | 28 | 27 | 26 | 25 | 24 |
|        | PADONE | PPSDONE |    |    |    |    |    |    |
| Access | W1S    | W1S     |    |    |    |    |    |    |
| Reset  | 0      | 0       |    |    |    |    |    |    |

|        |    |    |    |    |         |         |         |         |
|--------|----|----|----|----|---------|---------|---------|---------|
| Bit    | 23 | 22 | 21 | 20 | 19      | 18      | 17      | 16      |
|        |    |    |    |    | EG3DONE | EG2DONE | EG1DONE | EG0DONE |
| Access |    |    |    |    | W1S     | W1S     | W1S     | W1S     |
| Reset  |    |    |    |    | 0       | 0       | 0       | 0       |

|        |    |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|----|---|---|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|        |    |    |    |    |    |    |   |   |
| Access |    |    |    |    |    |    |   |   |
| Reset  |    |    |    |    |    |    |   |   |

|        |       |       |       |       |       |       |       |       |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|        | EC3DA | EC3OF | EC2DA | EC2OF | EC1DA | EC1OF | EC0DA | EC0OF |
| Access | W1S   | W1S   | W1S   | W1S   | W1S   | W1S   | W1S   | W1S   |
| Reset  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**Bit 31 – PADONE** Phase Adjust Done

Setting this bit will set the SEV bit of the OA\_STATUS1 register when phase adjust is done.

**Bit 30 – PPSDONE** One pulse-per-second signal generation done

Setting this bit will set the SEV bit of the OA\_STATUS1 register when the 1PPS signal generation is done.

**Bit 30 – PAER** Phase adjust error

Setting this bit will set the SEV bit of the OA\_STATUS1 register when an error is detected by the phase adjuster.

**Bit 19 – EG3DONE** Event generator 3 done

Setting this bit will set the SEV bit of the OA\_STATUS1 register when the pulse sequence configured on event generator 3 is done.

**Bit 18 – EG2DONE** Event generator 2 done completed.

Setting this bit will set the SEV bit of the OA\_STATUS1 register when the pulse sequence configured on event generator 2 is done.

**Bit 17 – EG1DONE** Event generator 1 done

Setting this bit will set the SEV bit of the OA\_STATUS1 register when the pulse sequence configured on event generator 1 is done.

**Bit 16 – EG0DONE** Event generator 0 done

Setting this bit will set the SEV bit of the OA\_STATUS1 register when the pulse sequence configured on event generator 0 is done.

**Bit 7 – EC3DA** Event capture unit 3 data available

Setting this bit will set the SEV bit of the OA\_STATUS1 register when timestamps are available to be read from event capture unit 3.

**Bit 6 – EC3OF** Event capture unit 3 overflow

Setting this bit will set the SEV bit of the OA\_STATUS1 register when event capture unit 3 has failed to capture a timestamp because no more storage was available.

**Bit 5 – EC2DA** Event capture unit 2 data available.

Setting this bit will set the SEV bit of the OA\_STATUS1 register when timestamps are available to be read from event capture unit 2.

**Bit 4 – EC2OF** Event capture unit 2 overflow

Setting this bit will set the SEV bit of the OA\_STATUS1 register when event capture unit 2 has failed to capture a timestamp because no more storage was available.

**Bit 3 – EC1DA** Event capture unit 1 data available

Setting this bit will set the SEV bit of the OA\_STATUS1 register when timestamps are available to be read from event capture unit 2.

**Bit 2 – EC1OF** Event capture unit 1 overflow

Setting this bit will set the SEV bit of the OA\_STATUS1 register event capture unit 1 has failed to capture a timestamp because no more storage was available.

**Bit 1 – EC0DA** Event capture unit 0 data available

Setting this bit will set the SEV bit of the OA\_STATUS1 register when timestamps are available to be read from event capture unit 0.

**Bit 0 – EC0OF** Event capture unit 0 overflow

Setting this bit will set the SEV bit of the OA\_STATUS1 register when event capture unit 0 has failed to capture a timestamp because no more storage was available.

**11.6.50 Synchronization Event Interrupt Disable Register****Name:** SEVINTDIS**Address:** 0x023B**Note:** The bits of this register are W1S.

|        |        |         |    |    |    |    |    |    |
|--------|--------|---------|----|----|----|----|----|----|
| Bit    | 31     | 30      | 29 | 28 | 27 | 26 | 25 | 24 |
|        | PADONE | PPSDONE |    |    |    |    |    |    |
| Access | W1S    | W1S     |    |    |    |    |    |    |
| Reset  | 0      | 0       |    |    |    |    |    |    |

|        |    |    |    |    |         |         |         |         |
|--------|----|----|----|----|---------|---------|---------|---------|
| Bit    | 23 | 22 | 21 | 20 | 19      | 18      | 17      | 16      |
|        |    |    |    |    | EG3DONE | EG2DONE | EG1DONE | EG0DONE |
| Access |    |    |    |    | W1S     | W1S     | W1S     | W1S     |
| Reset  |    |    |    |    | 0       | 0       | 0       | 0       |

|        |    |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|----|---|---|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|        |    |    |    |    |    |    |   |   |
| Access |    |    |    |    |    |    |   |   |
| Reset  |    |    |    |    |    |    |   |   |

|        |       |       |       |       |       |       |       |       |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|        | EC3DA | EC3OF | EC2DA | EC2OF | EC1DA | EC1OF | EC0DA | EC0OF |
| Access | W1S   | W1S   | W1S   | W1S   | W1S   | W1S   | W1S   | W1S   |
| Reset  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**Bit 31 – PADONE** Phase Adjust Done

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when phase adjust is done.

**Bit 30 – PPSDONE** One pulse-per-second signal generation done

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when one pulse-per-second signal generation has completed.

**Bit 30 – PAER** Phase adjust error

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when an error was detected by the phase adjuster.

**Bit 19 – EG3DONE** Event generator 3 done

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when the pulse sequence configured on event generator 3 is done.

**Bit 18 – EG2DONE** Event generator 2 done

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when the pulse sequence configured on event generator 2 is done.

**Bit 17 – EG1DONE** Event generator 1 done

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when the pulse sequence configured on event generator 1 is done.

**Bit 16 – EG0DONE** Event generator 0 done

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when the pulse sequence configured on event generator 0 is done.

**Bit 7 – EC3DA** Event capture unit 3 data available

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when timestamps are available to be read from event capture unit 3.

**Bit 6 – EC3OF** Event capture unit 3 overflow

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when event capture unit 3 has failed to capture a timestamp because no more storage was available.

**Bit 5 – EC2DA** Event capture unit 2 data available.

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when timestamps are available to be read from event capture unit 2.

**Bit 4 – EC2OF** Event capture unit 2 overflow

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when event capture unit 2 has failed to capture a timestamp because no more storage was available.

**Bit 3 – EC1DA** Event capture unit 1 data available

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when timestamps are available to be read from event capture unit 2.

**Bit 2 – EC1OF** Event capture unit 1 overflow

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when event capture unit 1 has failed to capture a timestamp because no more storage was available.

**Bit 1 – EC0DA** Event capture unit 0 data available

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when timestamps are available to be read from event capture unit 0.

**Bit 0 – EC0OF** Event capture unit 0 overflow

Setting this bit will prevent any effect on the SEV bit of OA\_STATUS1 when event capture unit 0 has failed to capture a timestamp because no more storage was available.

**11.6.51 Synchronization Event Interrupt Mask Status Register**

**Name:** SEVIM  
**Address:** 0x023C

**Note:** This register is read only.

|        |        |         |    |    |    |    |    |    |
|--------|--------|---------|----|----|----|----|----|----|
| Bit    | 31     | 30      | 29 | 28 | 27 | 26 | 25 | 24 |
|        | PADONE | PPSDONE |    |    |    |    |    |    |
| Access | RO     | RO      |    |    |    |    |    |    |
| Reset  | 0      | 0       |    |    |    |    |    |    |

|        |    |    |    |    |         |         |         |         |
|--------|----|----|----|----|---------|---------|---------|---------|
| Bit    | 23 | 22 | 21 | 20 | 19      | 18      | 17      | 16      |
|        |    |    |    |    | EG3DONE | EG2DONE | EG1DONE | EG0DONE |
| Access |    |    |    |    | RO      | RO      | RO      | RO      |
| Reset  |    |    |    |    | 0       | 0       | 0       | 0       |

|        |    |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|----|---|---|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|        |    |    |    |    |    |    |   |   |
| Access |    |    |    |    |    |    |   |   |
| Reset  |    |    |    |    |    |    |   |   |

|        |       |       |       |       |       |       |       |       |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|        | EC3DA | EC3OF | EC2DA | EC2OF | EC1DA | EC1OF | EC0DA | EC0OF |
| Access | RO    | RO    | RO    | RO    | RO    | RO    | RO    | RO    |
| Reset  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**Bit 31 – PADONE** Phase Adjust Done

| Value | Description                                                                                   |
|-------|-----------------------------------------------------------------------------------------------|
| 0     | When the PADONE bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The PADONE bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 30 – PPSDONE** One pulse-per-second signal generation done

| Value | Description                                                                                    |
|-------|------------------------------------------------------------------------------------------------|
| 0     | When the PPSDONE bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The PPSDONE bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 30 – PAER** Phase adjust error

| Value | Description                                                                                 |
|-------|---------------------------------------------------------------------------------------------|
| 0     | When the PAER bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The PAER bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 19 – EG3DONE** Event generator 3 done

| Value | Description                                                                                    |
|-------|------------------------------------------------------------------------------------------------|
| 0     | When the EG3DONE bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EG3DONE bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 18 – EG2DONE** Event generator 2 done

| Value | Description                                                                                    |
|-------|------------------------------------------------------------------------------------------------|
| 0     | When the EG2DONE bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EG2DONE bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 17 – EG1DONE** Event generator 1 done

| Value | Description                                                                                    |
|-------|------------------------------------------------------------------------------------------------|
| 0     | When the EG1DONE bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |

| Value | Description                                                             |
|-------|-------------------------------------------------------------------------|
| 1     | The EG1DONE bit of the SEVSTS has no effect on the OA_STATUS1 register. |

**Bit 16 – EG0DONE** Event generator 0 done

| Value | Description                                                                                    |
|-------|------------------------------------------------------------------------------------------------|
| 0     | When the EG0DONE bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EG0DONE bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 7 – EC3DA** Event capture unit 3 data available

| Value | Description                                                                                  |
|-------|----------------------------------------------------------------------------------------------|
| 0     | When the EC3DA bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EC3DA bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 6 – EC3OF** Event capture unit 3 overflow

| Value | Description                                                                                  |
|-------|----------------------------------------------------------------------------------------------|
| 0     | When the EC3OF bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EC3OF bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 5 – EC2DA** Event capture unit 2 data available

| Value | Description                                                                                  |
|-------|----------------------------------------------------------------------------------------------|
| 0     | When the EC2DA bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EC2DA bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 4 – EC2OF** Event capture unit 2 overflow

| Value | Description                                                                                  |
|-------|----------------------------------------------------------------------------------------------|
| 0     | When the EC2OF bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EC2OF bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 3 – EC1DA** Event capture unit 1 data available

| Value | Description                                                                                  |
|-------|----------------------------------------------------------------------------------------------|
| 0     | When the EC1DA bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EC1DA bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 2 – EC1OF** Event capture unit 1 overflow

| Value | Description                                                                                  |
|-------|----------------------------------------------------------------------------------------------|
| 0     | When the EC1OF bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EC1OF bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 1 – EC0DA** Event capture unit 0 data available

| Value | Description                                                                                  |
|-------|----------------------------------------------------------------------------------------------|
| 0     | When the EC0DA bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EC0DA bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |

**Bit 0 – EC0OF** Event capture unit 0 overflow

| Value | Description                                                                                  |
|-------|----------------------------------------------------------------------------------------------|
| 0     | When the EC0OF bit of the SEVSTS is set, the SEV bit of the OA_STATUS1 register will be set. |
| 1     | The EC0OF bit of the SEVSTS has no effect on the OA_STATUS1 register.                        |



## 11.6.52 Synchronization Event Status Register

**Name:** SEVSTS

**Address:** 0x023D

This register indicates all event status bits set since this register was last read.



**Important:** All bits are cleared upon read.

|        |        |         |    |    |    |    |    |    |
|--------|--------|---------|----|----|----|----|----|----|
| Bit    | 31     | 30      | 29 | 28 | 27 | 26 | 25 | 24 |
|        | PADONE | PPSDONE |    |    |    |    |    |    |
| Access | RC     | RC      |    |    |    |    |    |    |
| Reset  | 0      | 0       |    |    |    |    |    |    |

|        |    |    |    |    |         |         |         |         |
|--------|----|----|----|----|---------|---------|---------|---------|
| Bit    | 23 | 22 | 21 | 20 | 19      | 18      | 17      | 16      |
|        |    |    |    |    | EG3DONE | EG2DONE | EG1DONE | EG0DONE |
| Access |    |    |    |    | RC      | RC      | RC      | RC      |
| Reset  |    |    |    |    | 0       | 0       | 0       | 0       |

|        |    |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|----|---|---|
| Bit    | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|        |    |    |    |    |    |    |   |   |
| Access |    |    |    |    |    |    |   |   |
| Reset  |    |    |    |    |    |    |   |   |

|        |       |       |       |       |       |       |       |       |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|        | EC3DA | EC3OF | EC2DA | EC2OF | EC1DA | EC1OF | EC0DA | EC0OF |
| Access | RC    | RC    | RC    | RC    | RC    | RC    | RC    | RC    |
| Reset  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**Bit 31 – PADONE** Phase Adjust done

This bit is set to indicate that phase adjust has completed. This bit will be cleared on read.

**Bit 30 – PPSDONE** One pulse-per-second signal generation done

This bit is set to indicate that the pulse per second signal generation has completed. This bit will be cleared on read.

**Bit 30 – PAER** Phase adjust error

This bit is set to indicate that an error was detected by the phase adjuster. This bit will be cleared on read.

**Bit 19 – EG3DONE** Event generator 3 done

This bit is set to indicate when event generator 3 has completed generation of a pulse or pulse sequence. This bit will be cleared on read.

**Bit 18 – EG2DONE** Event generator 2 done

This bit is set to indicate when event generator 2 has completed generation of a pulse or pulse sequence. This bit will be cleared on read.

**Bit 17 – EG1DONE** Event generator 1 done

This bit is set to indicate when event generator 1 has completed generation of a pulse or pulse sequence. This bit will be cleared on read.

**Bit 16 – EG0DONE** Event generator 0 done

This bit is set to indicate when event generator 0 has completed generation of a pulse or pulse sequence. This bit will be cleared on read.

**Bit 7 – EC3DA** Event capture unit 3 data available

This bit is set to indicate that timestamps are available to be read from event capture unit 3. This bit will be cleared on read.

**Bit 6 – EC3OF** Event capture unit 3 overflow

This bit is set to indicate that event capture unit 3 has failed to capture a timestamp because no more storage was available. This bit will be cleared on read.

**Bit 5 – EC2DA** Event capture unit 2 data available

This bit is set to indicate that timestamps are available to be read from event capture unit 2. This bit will be cleared on read.

**Bit 4 – EC2OF** Event capture unit 2 overflow

This bit is set to indicate that event capture unit 2 has failed to capture a timestamp because no more storage was available. This bit will be cleared on read.

**Bit 3 – EC1DA** Event capture unit 1 data available

This bit is set to indicate that timestamps are available to be read from event capture unit 1. This bit will be cleared on read.

**Bit 2 – EC1OF** Event capture unit 1 overflow

This bit is set to indicate that event capture unit 1 has failed to capture a timestamp because no more storage was available. This bit will be cleared on read.

**Bit 1 – EC0DA** Event capture unit 0 data available

This bit is set to indicate that timestamps are available to be read from event capture unit 0. This bit will be cleared on read.

**Bit 0 – EC0OF** Event capture unit 0 overflow

This bit is set to indicate that event capture unit 0 has failed to capture a timestamp because no more storage was available. This bit will be cleared on read.

## 12. Data Sheet Revision History

**Table 12-1.** Data Sheet Revision History

| Revision Level & Date  | Section/Figure/Entry | Correction                                           |
|------------------------|----------------------|------------------------------------------------------|
| DS60001734D (Aug-2023) | All                  | Update for silicon revision 2 (product revision B1)  |
| DS60001734C (Feb-2023) | Table 9.4            | Updated Power Consumption for LAN8651.               |
| DS60001734B (Feb-2023) | All                  | Update for silicon revision 1 (product revision B0)  |
| DS60001734A (Nov-2021) | All                  | Initial for silicon revision 0 (product revision A0) |

## Microchip Information

### The Microchip Website

Microchip provides online support via our website at [www.microchip.com/](http://www.microchip.com/). This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

### Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to [www.microchip.com/pcn](http://www.microchip.com/pcn) and follow the registration instructions.

### Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: [www.microchip.com/support](http://www.microchip.com/support)

## Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u>       | <u>XX</u>                                                                                                                               | <u>[X]<sup>(1)</sup></u>                                                    | - | <u>X</u>          | / | <u>XXX</u>   | <u>[XXX]</u>    |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|---|-------------------|---|--------------|-----------------|
| Device                | Product Revision                                                                                                                        | Tape and Reel Option                                                        |   | Temperature Grade |   | Package Type | Automotive Code |
| Device:               | LAN8650 10BASE-T1S MAC-PHY Ethernet Controller, 3.3/1.8V supplies<br>LAN8651 10BASE-T1S MAC-PHY Ethernet Controller, single 3.3V supply |                                                                             |   |                   |   |              |                 |
| Product Revision:     | xx                                                                                                                                      | Two character code specifying product revision                              |   |                   |   |              |                 |
| Tape and Reel Option: | Blank                                                                                                                                   | Standard packaging (tray)                                                   |   |                   |   |              |                 |
|                       | T                                                                                                                                       | Tape and Reel <sup>(1)</sup>                                                |   |                   |   |              |                 |
| Temperature Grade:    | E                                                                                                                                       | -40°C to +125°C Extended range                                              |   |                   |   |              |                 |
| Package Type:         | LMX                                                                                                                                     | 32-pin VQFN                                                                 |   |                   |   |              |                 |
| Automotive Code:      | Vxx                                                                                                                                     | Optional three character code with "V" prefix specifying automotive product |   |                   |   |              |                 |

- LAN8650B1-E/LMXVAO - 10BASE-T1S MAC-PHY Ethernet Controller, 3.3/1.8V supply, Revision B1, Standard tray packaging, 32-VQFN package, -40°C to +125°C, automotive
- LAN8650B1T-E/LMX - 10BASE-T1S MAC-PHY Ethernet Controller, 3.3/1.8V supply, Revision B1, Tape and Reel packaging, 32-VQFN package, -40°C to +125°C
- LAN8651B1T-E/LMXVAO - 10BASE-T1S MAC-PHY Ethernet Controller, 3.3V supply, Revision B1, Tape and Reel packaging, 32-VQFN package, -40°C to +125°C, automotive
- LAN8651B1-E/LMX - 10BASE-T1S MAC-PHY Ethernet Controller, 3.3V supply, Revision B1, Standard tray packaging, 32-VQFN package, -40°C to +125°C

### Note:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

## Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

## Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at [www.microchip.com/en-us/support/design-help/client-support-services](http://www.microchip.com/en-us/support/design-help/client-support-services).

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

## Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, EyeOpen, GridTime, IdealBridge, IGaT, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, MarginLink, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mSiC, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, Power MOS IV, Power MOS 7, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, Turing, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2023, Microchip Technology Incorporated and its subsidiaries. All Rights Reserved.

ISBN: 978-1-6683-3007-4

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro,  $\mu$ Vision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

## Quality Management System

For information regarding Microchip's Quality Management Systems, please visit [www.microchip.com/quality](http://www.microchip.com/quality).

## Worldwide Sales and Service

| AMERICAS                                                                                                                                                                                                                                                                                               | ASIA/PACIFIC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | ASIA/PACIFIC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | EUROPE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Corporate Office</b><br>2355 West Chandler Blvd.<br>Chandler, AZ 85224-6199<br>Tel: 480-792-7200<br>Fax: 480-792-7277<br>Technical Support:<br><a href="http://www.microchip.com/support">www.microchip.com/support</a><br>Web Address:<br><a href="http://www.microchip.com">www.microchip.com</a> | <b>Australia - Sydney</b><br>Tel: 61-2-9868-6733<br><b>China - Beijing</b><br>Tel: 86-10-8569-7000<br><b>China - Chengdu</b><br>Tel: 86-28-8665-5511<br><b>China - Chongqing</b><br>Tel: 86-23-8980-9588<br><b>China - Dongguan</b><br>Tel: 86-769-8702-9880<br><b>China - Guangzhou</b><br>Tel: 86-20-8755-8029<br><b>China - Hangzhou</b><br>Tel: 86-571-8792-8115<br><b>China - Hong Kong SAR</b><br>Tel: 852-2943-5100<br><b>China - Nanjing</b><br>Tel: 86-25-8473-2460<br><b>China - Qingdao</b><br>Tel: 86-532-8502-7355<br><b>China - Shanghai</b><br>Tel: 86-21-3326-8000<br><b>China - Shenyang</b><br>Tel: 86-24-2334-2829<br><b>China - Shenzhen</b><br>Tel: 86-755-8864-2200<br><b>China - Suzhou</b><br>Tel: 86-186-6233-1526<br><b>China - Wuhan</b><br>Tel: 86-27-5980-5300<br><b>China - Xian</b><br>Tel: 86-29-8833-7252<br><b>China - Xiamen</b><br>Tel: 86-592-2388138<br><b>China - Zhuhai</b><br>Tel: 86-756-3210040 | <b>India - Bangalore</b><br>Tel: 91-80-3090-4444<br><b>India - New Delhi</b><br>Tel: 91-11-4160-8631<br><b>India - Pune</b><br>Tel: 91-20-4121-0141<br><b>Japan - Osaka</b><br>Tel: 81-6-6152-7160<br><b>Japan - Tokyo</b><br>Tel: 81-3-6880-3770<br><b>Korea - Daegu</b><br>Tel: 82-53-744-4301<br><b>Korea - Seoul</b><br>Tel: 82-2-554-7200<br><b>Malaysia - Kuala Lumpur</b><br>Tel: 60-3-7651-7906<br><b>Malaysia - Penang</b><br>Tel: 60-4-227-8870<br><b>Philippines - Manila</b><br>Tel: 63-2-634-9065<br><b>Singapore</b><br>Tel: 65-6334-8870<br><b>Taiwan - Hsin Chu</b><br>Tel: 886-3-577-8366<br><b>Taiwan - Kaohsiung</b><br>Tel: 886-7-213-7830<br><b>Taiwan - Taipei</b><br>Tel: 886-2-2508-8600<br><b>Thailand - Bangkok</b><br>Tel: 66-2-694-1351<br><b>Vietnam - Ho Chi Minh</b><br>Tel: 84-28-5448-2100 | <b>Austria - Wels</b><br>Tel: 43-7242-2244-39<br>Fax: 43-7242-2244-393<br><b>Denmark - Copenhagen</b><br>Tel: 45-4485-5910<br>Fax: 45-4485-2829<br><b>Finland - Espoo</b><br>Tel: 358-9-4520-820<br><b>France - Paris</b><br>Tel: 33-1-69-53-63-20<br>Fax: 33-1-69-30-90-79<br><b>Germany - Garching</b><br>Tel: 49-8931-9700<br><b>Germany - Haan</b><br>Tel: 49-2129-3766400<br><b>Germany - Heilbronn</b><br>Tel: 49-7131-72400<br><b>Germany - Karlsruhe</b><br>Tel: 49-721-625370<br><b>Germany - Munich</b><br>Tel: 49-89-627-144-0<br>Fax: 49-89-627-144-44<br><b>Germany - Rosenheim</b><br>Tel: 49-8031-354-560<br><b>Israel - Ra'anana</b><br>Tel: 972-9-744-7705<br><b>Italy - Milan</b><br>Tel: 39-0331-742611<br>Fax: 39-0331-466781<br><b>Italy - Padova</b><br>Tel: 39-049-7625286<br><b>Netherlands - Drunen</b><br>Tel: 31-416-690399<br>Fax: 31-416-690340<br><b>Norway - Trondheim</b><br>Tel: 47-72884388<br><b>Poland - Warsaw</b><br>Tel: 48-22-3325737<br><b>Romania - Bucharest</b><br>Tel: 40-21-407-87-50<br><b>Spain - Madrid</b><br>Tel: 34-91-708-08-90<br>Fax: 34-91-708-08-91<br><b>Sweden - Gothenberg</b><br>Tel: 46-31-704-60-40<br><b>Sweden - Stockholm</b><br>Tel: 46-8-5090-4654<br><b>UK - Wokingham</b><br>Tel: 44-118-921-5800<br>Fax: 44-118-921-5820 |