



CMOS 12-Bit Monolithic Multiplying DAC

AD7541A

1.1 Scope.

T-51-09-12

This specification covers the detail requirements for a 12-bit monolithic CMOS multiplying digital-to-analog converter. The AD7541A is a direct replacement for the industry standard AD7541, offering improved performance in the areas of latch-up, lower gain error and gain temperature coefficient.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD7541AS(X)/883B
-2	AD7541AT(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted. Pin numbers refer to DIP package.)

V_{DD} (Pin 16) to GND	+	17V
V_{REF} (Pin 17) to GND	±	25V
V_{RFB} (Pin 18) to GND	±	25V
Digital Input Voltage (Pin 4–Pin 15) to GND	–	0.3V, V_{DD}
V_{PIN1}, V_{PIN2} to GND	–	0.3V to V_{DD}
Power Dissipation		
Up to $+75^\circ\text{C}$		450mW
Derates above $+75^\circ\text{C}$		6mW/ $^\circ\text{C}$
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature Range		-65°C to $+150^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-18 and E-20A

$\theta_{JA} = 120^\circ\text{C/W}$ for Q-18 and E-20A

AD7541A—SPECIFICATIONS

T-51-09-12

Test	Symbol	Device	Design Limit @ +125°C	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2	12					Bits
Relative Accuracy	RA	-1	1	1	1		All Grades Guaranteed Monotonic to 12 Bits, T_{min} to T_{max}	\pm LSB max
		-2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	-1	1	1	1		All Grades Guaranteed Monotonic to 12 Bits, T_{min} to T_{max}	\pm LSB
		-2	1/2	1	1/2	1/2		
Gain Error ²	AE	-1	8	6	8			\pm LSB max
		-2	5	6	5	3		
Gain Tempco	TC _{AE}	-1, 2	5					\pm ppm/ $^{\circ}$ C max
Power Supply Rejection	PSRR	-1, 2	0.02	0.01	0.02		$\Delta V_{DD} = \pm 5\%$	\pm % per % max
Output Leakage Current Pin 1 Pin 2	I _{OUT1}	-1, 2	200	5	200		Digital Inputs = 0V	\pm nA max
	I _{OUT2}	-1, 2	200	5	200		Digital Inputs = V_{DD}	\pm nA max
Output Current Settling Time		-1, 2	0.6				To $\pm 1/2$ LSB, $R_{OUT} = 100\Omega$, $C_{OUT1} = 13pF$ Digital Inputs = V_{IH} to V_{IL} or V_{IL} to V_{IH}	μ s typ
Feedthrough Error ³	FT	-1, 2	1				$V_{REF} = \pm 10V$ 10kHz Sinewave $T_A = +25^{\circ}C$	mV p-p typ
Reference Input Resistance	R _{IN}	-1, 2	7	7	7			k Ω min
		-1, 2	18	18	18			k Ω max
Digital Input High Voltage	V _{IH}	-1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	-1, 2	1	1	1		$V_{IN} = 0V$ or V_{DD}	\pm μ A max
Digital Input Capacitance	C _{IN}	-1, 2	8					pF max
Output Capacitance Pin 1 Pin 2 Pin 1 Pin 2	C _{OUT1}	-1, 2	200				Digital Inputs = V_{IH}	pF max
		-1, 2	70				Digital Inputs = V_{IL}	pF max
	C _{OUT2}	-1, 2	70				Digital Inputs = V_{IL}	pF max
		-1, 2	200				Digital Inputs = V_{IL}	pF max
Supply Current from V_{DD}	I _{DD}	-1, 2	2 500	2 100	2 500		Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	mA max μ A max

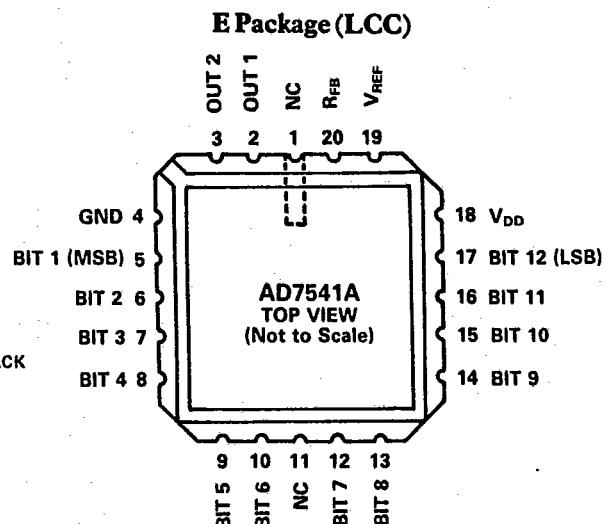
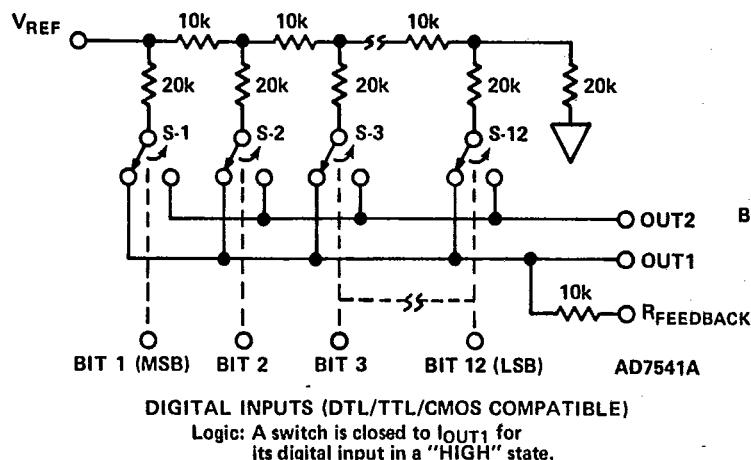
NOTES

¹ $V_{DD} = +15V$; $V_{OUT1} = V_{OUT2} = 0V$; $V_{REF} = +10V$ unless otherwise stated.²Measured using internal feedback resistor and includes effect of leakage current and gain TC.³Feedthrough error can be reduced by connecting the lid of the ceramic package to ground.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

T-51-09-12



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

