40V, 9A, Low I_Q Synchronous Step-Up Silent Switcher with Input Disconnect and PassThru

FEATURES

- **Silent Switcher**™ Architecture
  - Ultralow EMI Emissions
  - Optional Spread Spectrum Frequency Modulation
- Integrated 40V, 9A Power Switches
- Output Short Protection/Inrush Current Reduction
- Wide Input Voltage Range: 2.8V to 40V
- Output Voltage Programmable up to 36V
  - Optional 2 Pins select 21 output voltages
- Low V_{IN} Pin Quiescent Current:
  - 350nA In Shutdown; 9µA In Burst Mode; 12µA In PassThru™ ($V_{IN} \geq V_{OUT}$)
- 100% Duty Cycle Capability
- Adjustable and Synchronizable: 300kHz to 3MHz
- Pulse-Skipping or Burst Mode at Light Load
- Output Soft-Start and Power Good Monitoring
- Small 24-Lead (4mm × 4mm) LQFN Package

APPLICATIONS

- Automotive and Industrial Power Supplies
- General Purpose Step-Up

GENERAL DESCRIPTION

The **LT®8342** is a low I_Q, synchronous step-up DC/DC converter. It features a Silent Switcher architecture and optional spread spectrum frequency modulation to minimize electromagnetic interference (EMI) emissions while delivering high efficiencies at high switching frequencies. Output short circuit protection and inrush current reduction are optional.

The wide input/output voltage range, low V_{IN} pin quiescent current in Burst Mode operation, and 100% duty cycle capability for the synchronous MOSFET in PassThru operation ($V_{IN} \geq V_{OUT}$) make the LT8342 ideally suited for general-purpose step-up and automotive Pre-Boost applications.

To reduce V_{OUT} quiescent current in the feedback loop, an optional internal resistor divider (≥10MΩ) and two pins select 21 output voltage levels.

The LT8342 integrates 40V, 9A power switches, operating at a switching frequency programmable between 300kHz and 3MHz and synchronizable to an external clock.

The LT8342 features a programmable output soft-start, output power good flag, and output overvoltage lockout.

TYPICAL APPLICATION

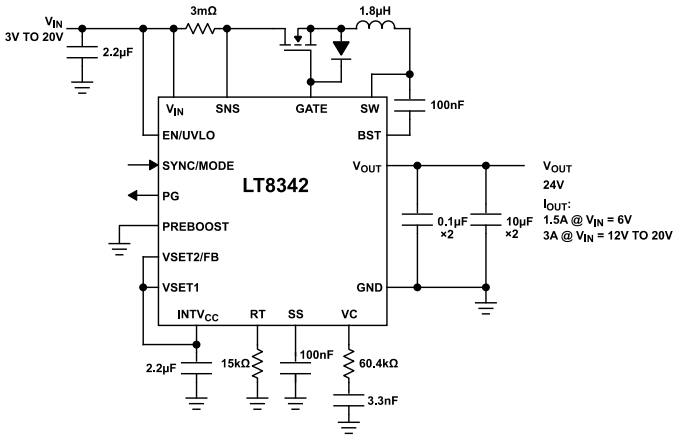

Figure 1. 2MHz, 24V, Step-Up Converter with Output Short Circuit Protection

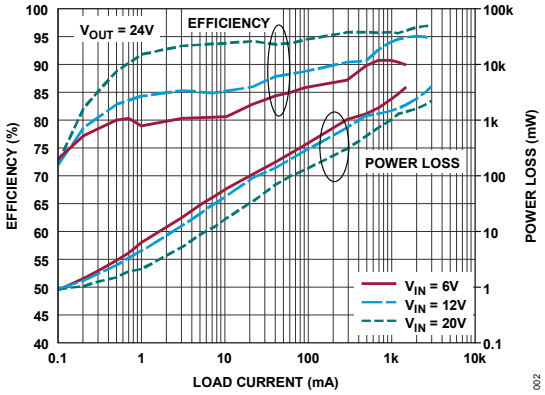

Figure 2. Efficiency and Power Loss vs Load Current in Burst Mode (SYNC/MODE = 0V)

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/24	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are for T_J = 25°C, V_{IN} = SNS = EN/UVLO = 5V unless otherwise noted[1].)

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
V_{IN} SUPPLY						
V_{IN} Operating Range		−40°C ≤ T_J ≤ 150°C	2.8		40	V
V_{IN} Quiescent Current in Shutdown	EN/UVLO < 0.15V	−40°C ≤ T_J ≤ 150°C		0.35	1.2	µA
V_{IN} Quiescent Current During Zero Load Conditions (No Switching), without external N-Channel FET (GATE = 0V)	SYNC/MODE = 0V (Burst Mode)			9	15	µA
		−40°C ≤ T_J ≤ 150°C			20	µA
	SYNC/MODE = $INTV_{CC}$ (Pulse-Skipping Mode)			1.9	2.5	mA
		−40°C ≤ T_J ≤ 150°C			3	mA
	V_{IN} = 10.1V, V_{OUT} ≤ 10V (PassThru), FB = 1.2V			12	20	µA
		−40°C ≤ T_J ≤ 150°C			30	µA
V_{IN} Quiescent Current During Zero Load Conditions (No Switching), with external N-Channel FET	SYNC/MODE = 0V (Burst Mode)			28	40	µA
		−40°C ≤ T_J ≤ 150°C			50	µA
	SYNC/MODE = $INTV_{CC}$ (Pulse-Skipping Mode)			1.9	2.5	mA
		−40°C ≤ T_J ≤ 150°C			3	mA
	V_{IN} = 10.1V, V_{OUT} ≤ 10V (PassThru), FB = 1.2V			26.5	40	µA
		−40°C ≤ T_J ≤ 150°C			55	µA
ENABLE/UNDERVOLTAGE LOCKOUT (UVLO)						
UVLO Threshold Voltage	EN/UVLO Falling	−40°C ≤ T_J ≤ 150°C	0.96	1.02	1.08	V
	Hysteresis			62		mV
EN/UVLO Pin Bias Current	EN/UVLO = 1V	−40°C ≤ T_J ≤ 150°C	−10		10	nA
ERROR AMPLIFIER, SOFT START, AND INTERNAL FEEDBACK						
Feedback Reference Voltage		−40°C ≤ T_J ≤ 150°C	0.99	1	1.01	V
Reference Voltage Line Regulation	$\Delta V_{FB}/\Delta V_{IN}$, 2.8V ≤ V_{IN} ≤ 40V			0	10	µV/V
VSET2/FB Pin Bias Current	VSET1 Pin is connected to $INTV_{CC}$ through 100kΩ		−10		10	nA

(Specifications are for T_J = 25°C, V_{IN} = SNS = EN/UVLO = 5V unless otherwise noted[1].)

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Error Amplifier Transconductance (gm_{EA})				160		µS
Error Amplifier Voltage Gain				600		V/V
Power Stage Transconductance (gmp)				14.7		S
Error Amplifier Source/Sink Current				36		µA
Soft-Start Pin Current	SS = 0.5V	−40°C ≤ T_J ≤ 150°C	9.1	10	10.5	µA
V_{OUT} Accuracy with Internal Feedback		−40°C ≤ T_J ≤ 150°C	−2		2	%
OSCILLATOR AND SPREAD SPECTRUM FREQUENCY MODULATION (SSFM)						
Switching Frequency Range		−40°C ≤ T_J ≤ 150°C	0.3		3.0	MHz
Switching Frequency (f_{OSC})	RT = 110kΩ	−40°C ≤ T_J ≤ 150°C	270	300	330	kHz
	RT = 31.6kΩ	−40°C ≤ T_J ≤ 150°C	0.95	1	1.05	MHz
	RT = 15kΩ	−40°C ≤ T_J ≤ 150°C	1.9	2	2.1	MHz
SSFM Mode Frequency Deviation	$\Delta f/f_{OSC}$ × 100%	RT = 15kΩ		13	20	%
SYNC/MODE						
SYNC Logic Level	SYNC Logic High	−40°C ≤ T_J ≤ 150°C	1.7			V
	SYNC Logic Low	−40°C ≤ T_J ≤ 150°C			0.4	V
f_{SYNC}/f_{OSC} allowed ratio			0.9	1	1.25	
INTERNAL NMOS POWER SWITCHES						
Bottom Switch On-Resistance	I_{SW} = 2A			25		mΩ
Bottom Switch Peak Current Limit		−40°C ≤ T_J ≤ 150°C	9	10.3	11	A
Bottom Switch Minimum Off-Time		−40°C ≤ T_J ≤ 150°C	20	35	50	ns

(Specifications are for T_J = 25°C, V_{IN} = SNS = EN/UVLO = 5V unless otherwise noted[1].)

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Bottom Switch Minimum On-Time	V_{IN} = 9.5V, V_{OUT} = 10V			60		ns
Top Switch On-Resistance	BST – SW = 4V, I_{SW} = 2A			30		mΩ
OUTPUT POWER GOOD AND OVERVOLTAGE LOCKOUT						
Power Not Good High (Outside this Window)[2]	FB Rising	−40°C ≤ T_J ≤ 150°C	7	11	15	%
	Hysteresis			3		%
Power Not Good Low (Outside this Window)	FB Falling	−40°C ≤ T_J ≤ 150°C	-13	-9	-5	%
	Hysteresis			3		%
PG Leakage Current	PG = 20V				1	µA
PG Pull-Down Voltage	1mA current (into the pin)		200	400	600	mV
V_{OUT} Over-Voltage Lockout (Rising)	Normalized to target or 36V	−40°C ≤ T_J ≤ 150°C	107	111	115	%
INPUT DISCONNECT						
GATE Drive Voltage (GATE − V_{IN})	V_{IN} = 3V, 1µA out of GATE pin	−40°C ≤ T_J ≤ 150°C	3.2	5	7	V
	V_{IN} ≥ 5V, 1µA out of GATE pin	−40°C ≤ T_J ≤ 150°C	4.5	6.5	8.5	V
GATE to V_{IN} Clamp Voltage	GATE−V_{IN}, 5mA into GATE pin		13	15	17	V
GATE Turn-On Pull-Up Current	GATE = 0V		5	9	13	µA
Over-Current Trip Voltage (ΔV_{SNS})	ΔV_{SNS} = V_{IN} − SNS	−40°C ≤ T_J ≤ 150°C	37.5	45	52.5	mV
Over-Current Event to GATE Turn-Off Propagation Delay				450		ns
GATE Turn-Off Pull-Down Current	GATE = 5V	During Over-Current Condition	80	135	190	mA
		During Time-Out Period		20		mA
GATE Retry Hiccup Time				40		ms

[1] LT8342R is specified over the −40°C ≤ T_J ≤ 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note that the maximum ambient temperature consistent with this specification is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

[2] If PreBoost is connected to $INTV_{CC}$, PG only pulls down if outside the lower window.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, SNS, EN/UVLO, V_{OUT}, SW, PG, VSET2/FB	−0.3V to 40V
GATE	−0.3V to Note[1]
BST	−0.3V to SW + 4V
V_{IN} to SNS	−1V to 1V
SYNC/MODE	−0.3V to 6V
PreBoost, VSET1, SS	−0.3V to 4V
VC, RT	−0.3V to 2V
Operating Junction Temperature Range: LT8342R[2,3]	−40°C to 150°C
Storage Temperature Range	−65°C to 150°C
Peak Solder Reflow Package Body Temperature	260°C

[1] Do not force with an external voltage source. If the function of input disconnect is not used, tie the GATE pin to ground.

[2] LT8342R is specified over the −40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

[3] LT8342R includes over-temperature protection that is intended to protect the device during momentary overload conditions. The junction temperature will exceed the maximum operating junction temperature when over-temperature is active. Continuous operating above the specified maximum operating junction temperature may impair device reliability.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to the Printed circuit board (PCB) design and the operating environment. Close attention to PCB thermal design is required.

Table 3. Thermal Resistance

BOARD TYPE	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOT}	UNIT
JEDEC BOARD	38	44	7	°C/W
DEMO BOARD	22	—	—	°C/W

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001, and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

Table 4. LT8342, 24-Lead (4mm × 4mm) LQFN

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
CDM	±1250	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

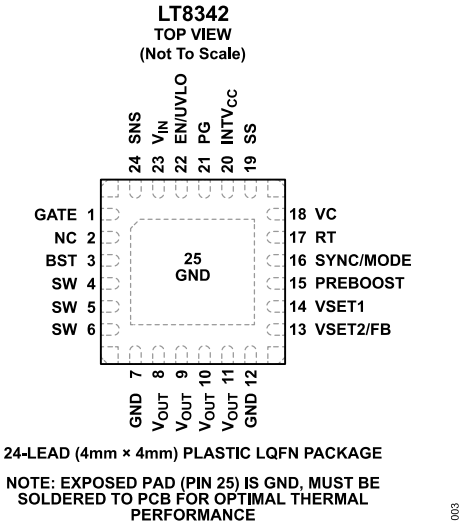


Figure 3. Pin Configuration

Table 5. Pin Descriptions

PIN	NAME	DESCRIPTION
1	GATE	Gate Driver Pin for External N-channel input-disconnect Field-effect transistor (FET). Connect this pin to the gate of the external FET, and a diode is needed to clamp between the gate and the source of the external FET. An internal 9µA current source charges the pin to V_{IN} + 6.5V. Do not drive or load this pin directly. Also, do not put the capacitor from the source of the Input Disconnect FET to ground. If external FET is not used, connect the GATE Pin to ground.
2	NC	No internal connection.
3	BST	Top Switch Driver Supply Pin. Place a 100nF, low Equivalent series resistance (ESR), ceramic capacitor between (and in close proximity to) BST and SW pins.
4, 5, 6	SW	Internal Power Switch Output Pin. This is the drain/source of the internal low-side/high-side NMOS power switches, respectively. To minimize EMI, minimize the metal trace area connected to this pin.
7, 12, Exposed Pad 25	GND	Ground Pin. The package has an exposed pad underneath the IC, which is the best path for heat and current out of the package. The pins should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT8342. See the *Recommended PCB Layout Guidelines* in the *Applications Information* Section to optimize GND returns for the best Silent Switcher performance.
8, 9, 10, 11	V_{OUT}	Converter Output Pin. A large, low ESR, ceramic capacitor (≥ 4.7µF) to GND is required to adequately filter the voltage ripple on the V_{OUT} pin. Two small ceramic capacitors (0.1µF), placed locally from V_{OUT} to GND, are recommended for optimal Silent Switcher

<table>
<tr><td></td><td></td><td>performance. See the Recommended PCB Layout Guidelines in the Applications Information Section. If external feedback is used (VSET1 tied to $INTV_{CC}$ through 100kΩ), set V_{OUT} with a resistor divider network from V_{OUT} to GND, with mid-point of resistor divider connected to VSET2/FB Pin (regulated to 1V).</td></tr>
<tr><td>13</td><td>VSET2/FB</td><td>Output Voltage Set 2 / External Feedback Pin. If internal feedback is used, program VSET2/FB Pin as shown in Table 6. If external feedback is used (VSET1 tied to $INTV_{CC}$ through 100kΩ), connect this pin to a resistor divider network from V_{OUT} to GND to set the desired V_{OUT} voltage. The LT8342 regulates the VSET2/FB pin to 1V (typical).

Table 6. Target V_{OUT} Configurations
<table>
<tr><th>VSET1</th><th>VSET2/FB</th><th>Target V_{OUT}</th></tr>
<tr><td>GND</td><td>GND</td><td>4V</td></tr>
<tr><td>GND</td><td>100kΩ to GND</td><td>6V</td></tr>
<tr><td>GND</td><td>Open</td><td>5V</td></tr>
<tr><td>GND</td><td>100kΩ to $INTV_{CC}$</td><td>7V</td></tr>
<tr><td>GND</td><td>$INTV_{CC}$</td><td>8V</td></tr>
<tr><td>Open</td><td>GND</td><td>9V</td></tr>
<tr><td>Open</td><td>100kΩ to GND</td><td>14V</td></tr>
<tr><td>Open</td><td>Open</td><td>10V</td></tr>
<tr><td>Open</td><td>100kΩ to $INTV_{CC}$</td><td>16V</td></tr>
<tr><td>Open</td><td>$INTV_{CC}$</td><td>12V</td></tr>
<tr><td>$INTV_{CC}$</td><td>GND</td><td>18V</td></tr>
<tr><td>$INTV_{CC}$</td><td>100kΩ to GND</td><td>22V</td></tr>
<tr><td>$INTV_{CC}$</td><td>Open</td><td>20V</td></tr>
<tr><td>$INTV_{CC}$</td><td>100kΩ to $INTV_{CC}$</td><td>26V</td></tr>
<tr><td>$INTV_{CC}$</td><td>$INTV_{CC}$</td><td>24V</td></tr>
<tr><td>100kΩ to GND</td><td>GND</td><td>28V</td></tr>
<tr><td>100kΩ to GND</td><td>100kΩ to GND</td><td>32V</td></tr>
<tr><td>100kΩ to GND</td><td>Open</td><td>30V</td></tr>
<tr><td>100kΩ to GND</td><td>100kΩ to $INTV_{CC}$</td><td>34V</td></tr>
<tr><td>100kΩ to GND</td><td>$INTV_{CC}$</td><td>36V</td></tr>
<tr><td>100kΩ to $INTV_{CC}$</td><td>GND</td><td>19V</td></tr>
<tr><td>100kΩ to $INTV_{CC}$</td><td>FB</td><td>External Feedback</td></tr>
</table></td></tr>
<tr><td>14</td><td>VSET1</td><td>Output Voltage Set 1 Pin. If internal feedback is used, program this pin as shown in Table 6. If external feedback is used, connect this pin to $INTV_{CC}$ through a 100kΩ resistor.</td></tr>
<tr><td>15</td><td>PREBOOST</td><td>PG mode Pin for PreBoost applications. When this pin is connected to GND, the PG Pin is pulled down when V_{OUT} is outside a ±10% window of its target voltage. When this pin is connected to $INTV_{CC}$, the PG Pin is only pulled low when V_{OUT} is lower than −10% of its target voltage. PG stays high in PassThru and saves quiescent current for PreBoost applications.</td></tr>
</table>

<table>
<tr><td>16</td><td>SYNC/MODE</td><td>This pin allows five selectable modes for optimization of performance.
<table><tr><th>SYNC / MODE Pin Input</th><th>Capable Mode(s) of Operation</th></tr><tr><td>GND or < 0.1V</td><td>Burst</td></tr><tr><td>External Clock</td><td>Pulse-skip/Sync</td></tr><tr><td>100k Resistor to GND</td><td>Burst/SSFM</td></tr><tr><td>Float (pin open)</td><td>Pulse-skip</td></tr><tr><td>$INTV_{CC}$</td><td>Pulse-skip/SSFM</td></tr></table>Where the selectable modes of operation are:
Burst = Low I_Q, low output ripple operation at light loads.
Pulse-skip = Skipped pulse(s) at light load (aligned to the clock).
Sync = Switching frequency synchronized to an external clock.
SSFM = Spread Spectrum Frequency Modulation for low EMI.</td></tr>
<tr><td>17</td><td>RT</td><td>Timing Resistor Pin. Connect a resistor from this pin to GND to set the LT8342's switching frequency internally. Do not float this pin. When clocking the IC externally with the SYNC pin, the external clock frequency can be no lower than 90% of the switching frequency programmed by the RT pin resistor.</td></tr>
<tr><td>18</td><td>VC</td><td>Error Amplifier Compensation Pin. Place the external RC compensation network from the VC pin to GND to stabilize the voltage loop.</td></tr>
<tr><td>19</td><td>SS</td><td>Soft-Start Pin. Place a soft-start capacitor C_{SS} between this pin and GND to program the output soft-start time.</td></tr>
<tr><td>20</td><td>$INTV_{CC}$</td><td>Internal 3.6V Regulator Bypass Pin. Connect a 2.2µF (or larger), low ESR, ceramic bypass capacitor from this pin to GND, placing the capacitor in close proximity to the pin. Do not drive this pin directly, nor load it with any other external circuitry. This pin powers the IC's internal switch drivers. $INTV_{CC}$ must exceed 2.75V to commence switching.</td></tr>
<tr><td>21</td><td>PG</td><td>Output Power Good Indicator Pin. The PG Pin is the open-drain output of an internal comparator. The PG pin is pulled low by the LT8342 when V_{OUT} is outside a ±10% window of its target voltage. An external pull-up resistor or current source pulls the PG pin high when the V_{OUT} enters a ±7% window around its target voltage. For a PreBoost application, the PREBOOST Pin can be connected to $INTV_{CC}$, so that the PG pin stays high at PassThru, and does not draw current.</td></tr>
<tr><td>22</td><td>EN/UVLO</td><td>Enable/Input Undervoltage Lockout Pin. The LT8342 is shut down when the EN/UVLO pin is driven below a 1.02V accurate threshold. The LT8342 is enabled when the EN/UVLO pin is driven above 1.08V.
The EN/UVLO pin can be connected to a resistor divider network from V_{IN} to GND to set a V_{IN} undervoltage lockout threshold below which the IC is disabled/shut down. See the Applications Information section for further details. Connect the pin directly to V_{IN} if the shutdown feature is not used.</td></tr>
<tr><td>23</td><td>V_{IN}</td><td>Input Supply Pin. Connect a 2.2µF (or larger) low ESR ceramic bypass capacitor from this pin to GND, placing the capacitor near the pin. The V_{IN} pin is also the positive input of the current sensing comparator for the input-disconnect FET.</td></tr>
</table>

24	SNS	Negative input of the current sensing comparator for the input-disconnect FET. Kelvin connect this pin to the external current sense resistor placed between the V_{IN} and the drain of the input-disconnect FET. The maximum V_{IN} to SNS voltage is limited to 45mV during over-current conditions, such as an output short circuit fault. Either connect this pin to V_{IN} or float this pin if the input-disconnect FET is not used.

TYPICAL PERFORMANCE CHARACTERISTICS

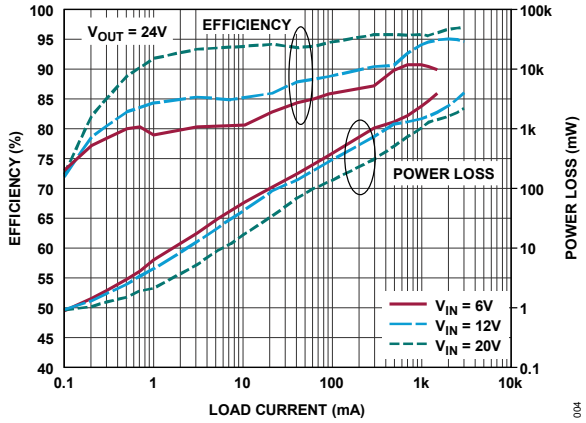


Figure 4. Burst Mode Efficiency and Power Loss vs Output Current. See Figure 1 with SYNC/MODE = 0V.

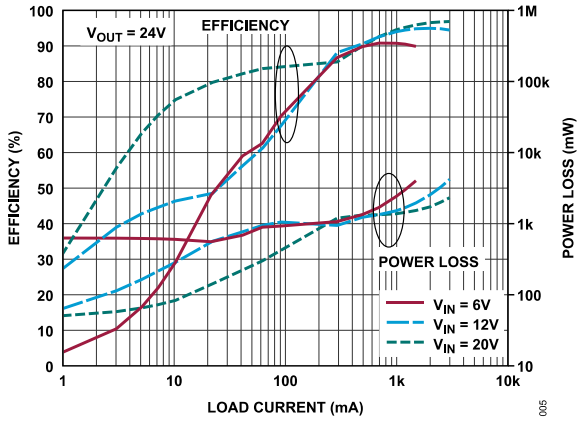


Figure 5. Pulse-Skip Mode Efficiency and Power Loss vs Output Current. See Figure 1 with SYNC/MODE open.

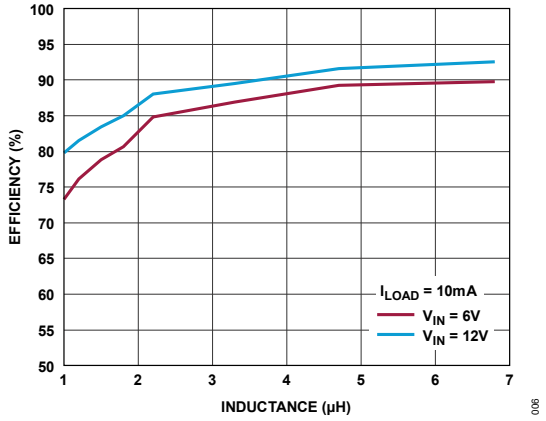


Figure 6. Burst Mode Efficiency vs Inductor Value. See Figure 1. V_{OUT} = 24V.

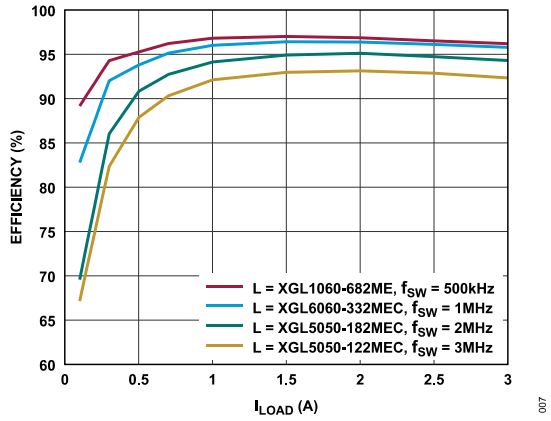


Figure 7. Efficiency vs Output Current at Different Switching Frequencies. See Figure 1. V_{IN} = 12V, V_{OUT} = 24V.

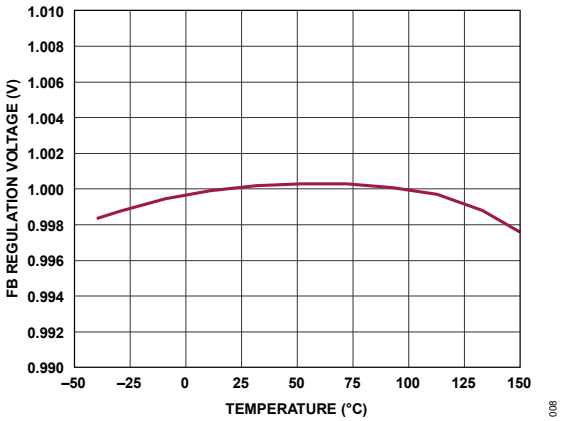


Figure 8. FB Regulation Voltage vs Temperature

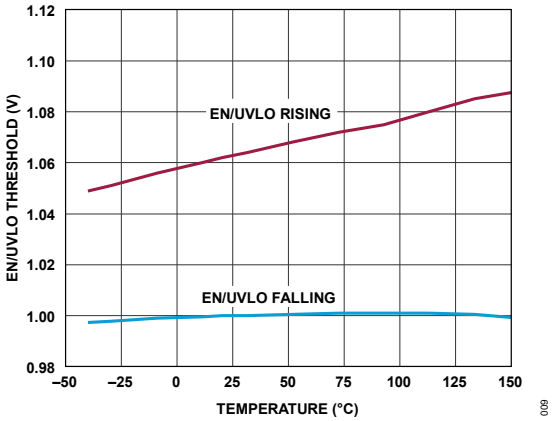


Figure 9. EN/UVLO Threshold vs Temperature

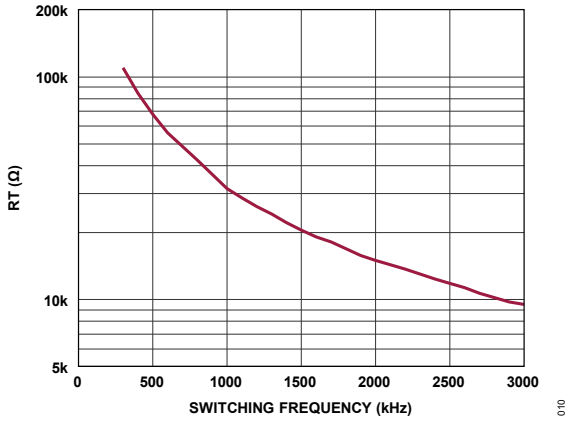


Figure 10. RT Value vs Switching Frequency

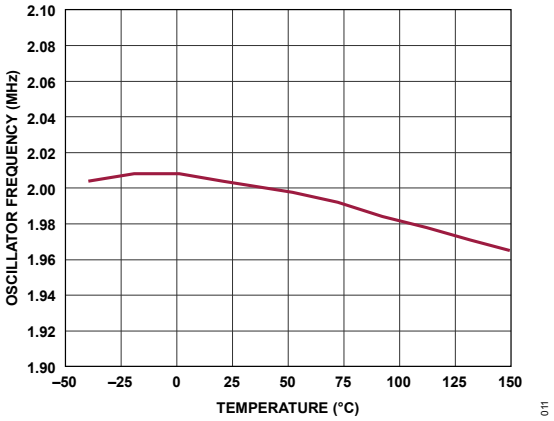


Figure 11. Oscillator Frequency vs Temperature

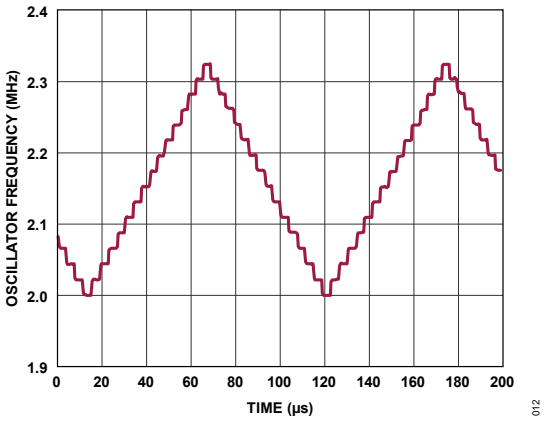


Figure 12. Oscillator Frequency with Spread Spectrum Modulation

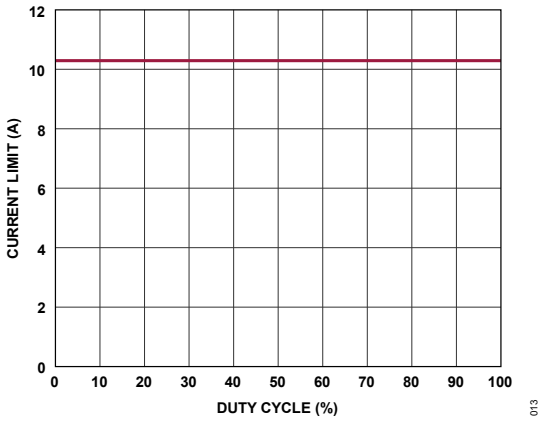


Figure 13. Bottom Switch Current Limit vs Duty Cycle

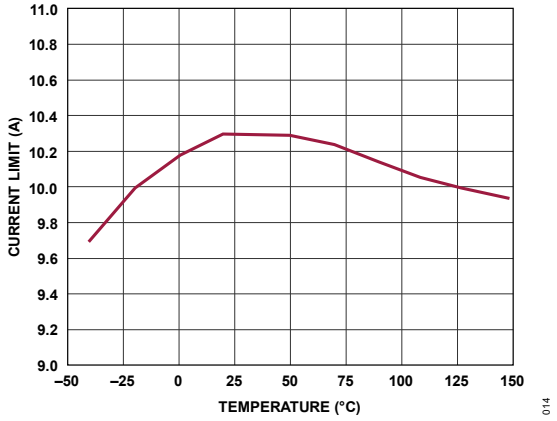


Figure 14. Bottom Switch Current Limit vs Temperature

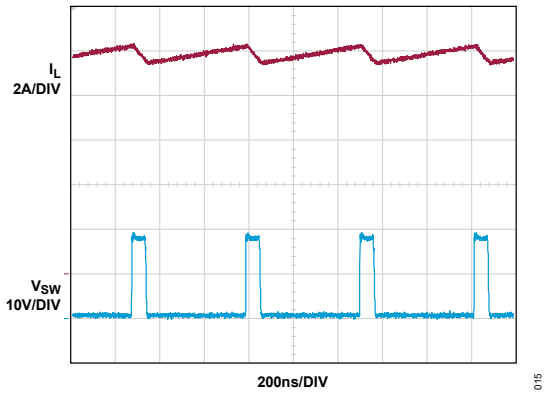


Figure 15. Switching Waveforms, Current Limit at 87% Duty Cycle. See Figure 1 at V_{IN} = 3V and Overload to V_{OUT} = 19V

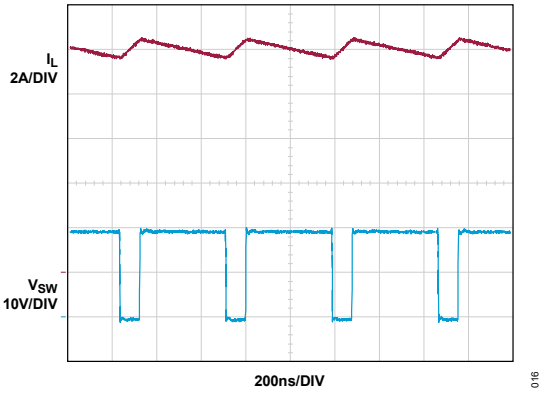


Figure 16. Switching Waveforms, Current Limit at 18% Duty Cycle. See Figure 1 at V_{IN} = 15V and Overload to V_{OUT} = 19V.

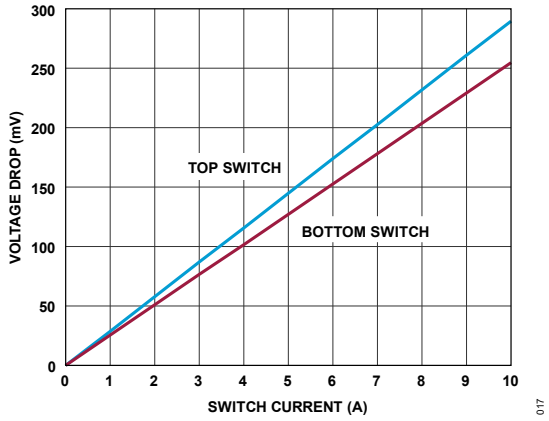


Figure 17. Power Switch Voltage Drop vs Switch Current

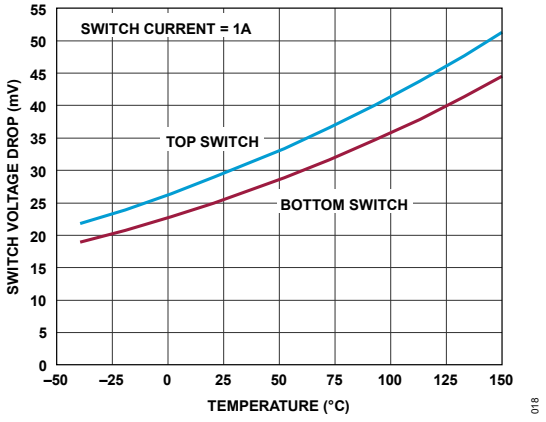


Figure 18. Power Switch Voltage Drop vs Temperature

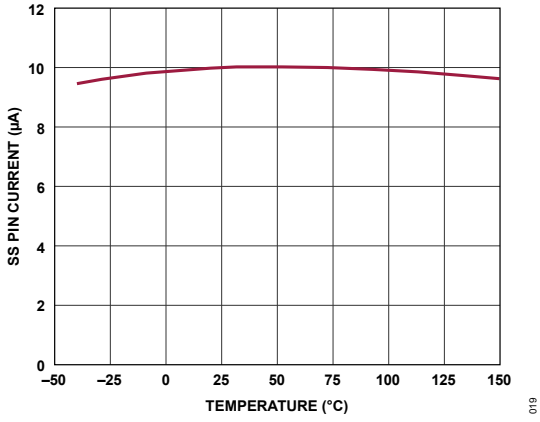


Figure 19. SS Pin Current vs Temperature

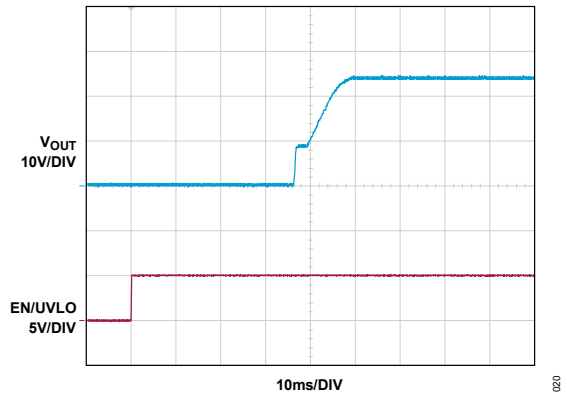


Figure 20. Soft Start, with Input Disconnect. See Figure 1, V_{IN} = 9V, V_{OUT} = 24V

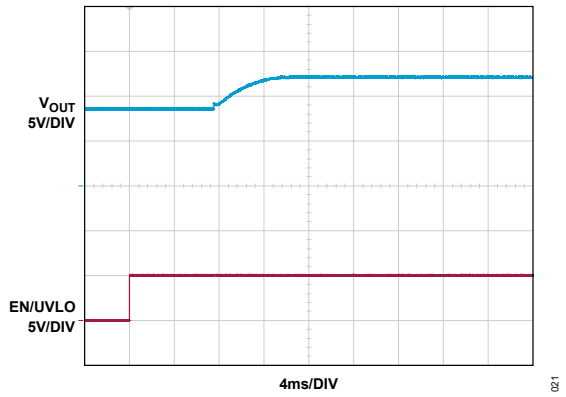


Figure 21. Soft Start, without Input Disconnect. See Circuit in Figure 45, V_{IN} = 9V, V_{OUT} = 12V

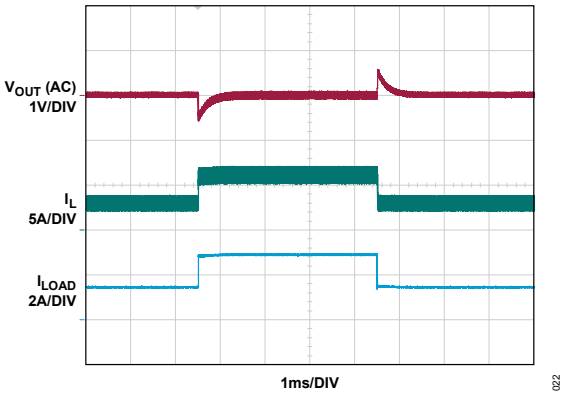


Figure 22. Load Transient Response: 1.5A to 3A. See Figure 1. V_{IN} = 12V, V_{OUT} = 24V

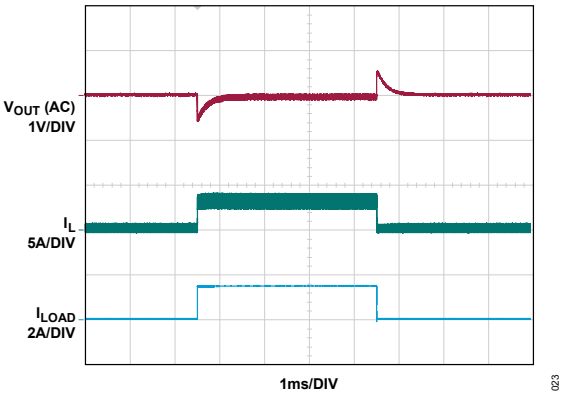


Figure 23. Load Transient Response: 50mA to 1.5A. See Figure 1, Pulse-Skip Mode. V_{IN} = 12V, V_{OUT} = 24V

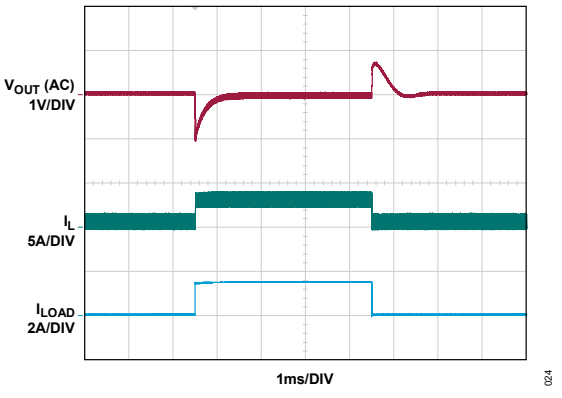


Figure 24. Load Transient Response: 50mA to 1.5A. See Figure 1, Burst Mode. V_{IN} = 12V, V_{OUT} = 24V

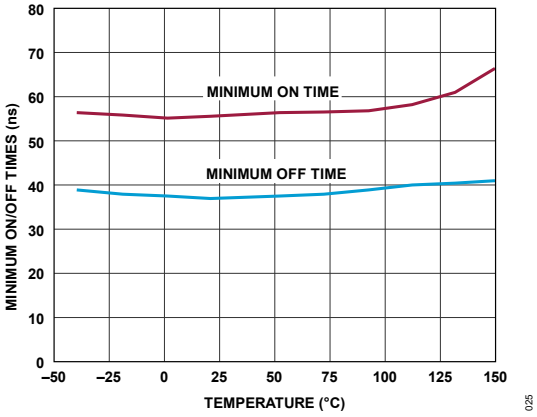


Figure 25. Bottom Switch Minimum On/Off Times vs Temperature

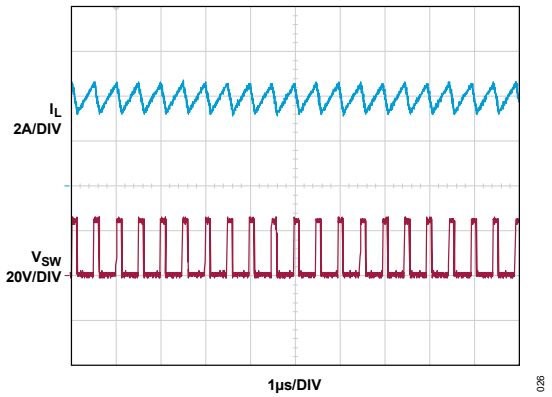


Figure 26. Full Frequency PWM Operation. See Figure 1, V_{IN} = 6V, V_{OUT} = 24V, I_{LOAD} = 900mA

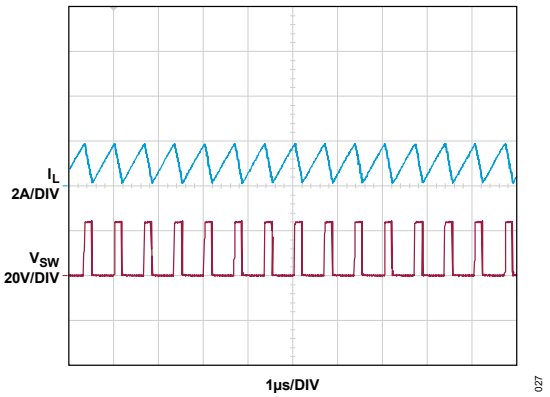


Figure 27. Continuous Burst Mode Operation. See Figure 1, SYNC/MODE = 0V, V_{IN} = 6V, I_{LOAD} = 230mA

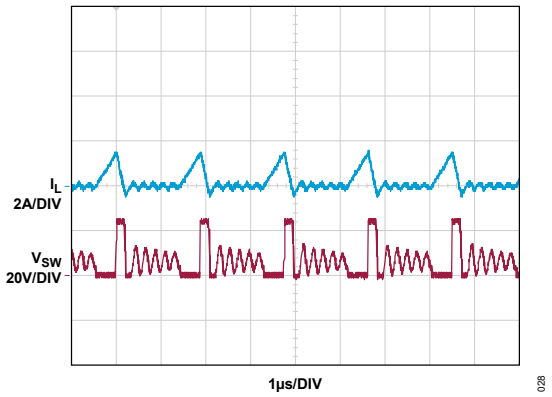


Figure 28. Discontinuous Burst Mode Operation. See Figure 1, SYNC/MODE = 0V, V_{IN} = 6V, I_{LOAD} = 50mA

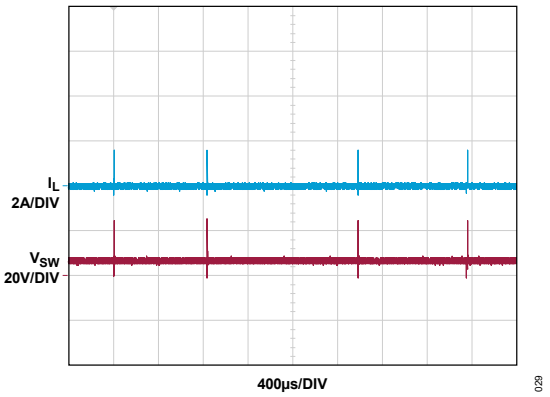


Figure 29. Light Load Low I_Q Burst Mode Operation. See Figure 1, SYNC/MODE = 0V, V_{IN} = 6V, I_{LOAD} = 0A

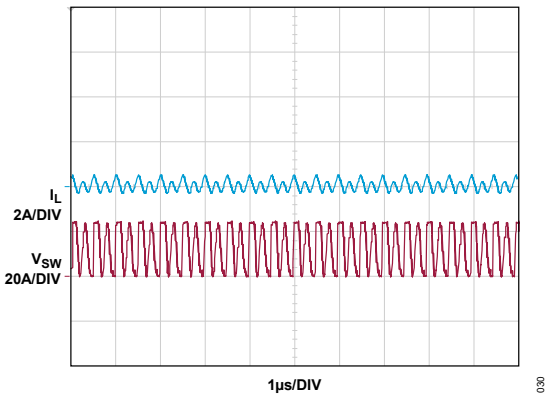


Figure 30. Discontinuous Pulse-Skipping Mode. See Figure 1, SYNC/MODE open, V_{IN} = 12V, I_{LOAD} = 0A

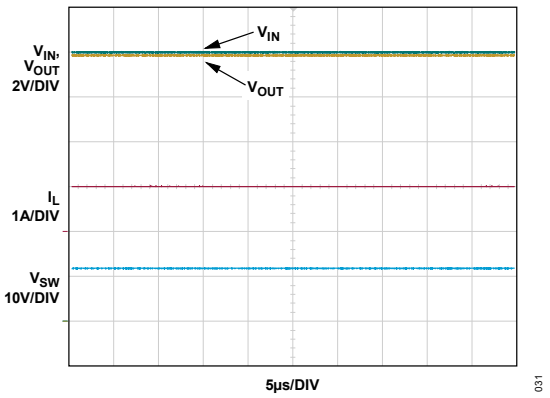


Figure 31. PassThru Mode Operation. See Circuit in Figure 49, V_{IN} = 12V, I_{LOAD} = 1A

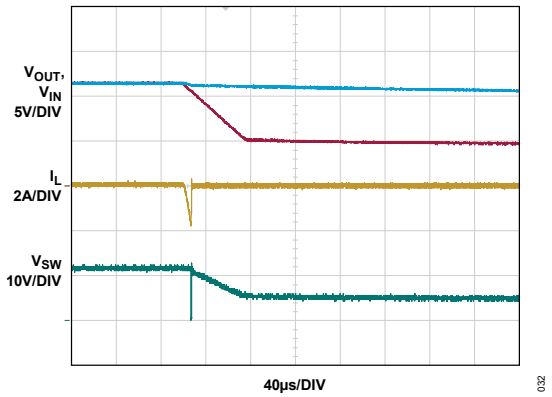


Figure 32. Reverse Current Protection in PassThru Mode. See Circuit in Figure 49, V_{IN} drops from 11V to 5V with no load

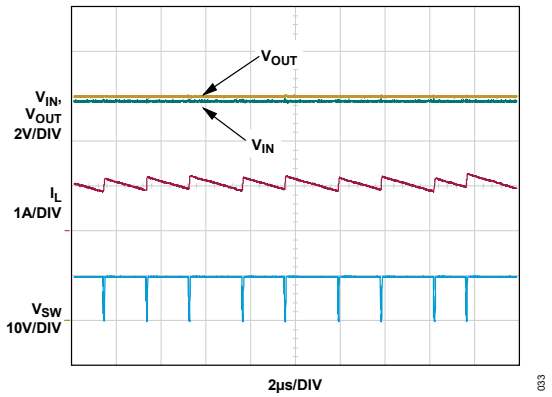


Figure 33. Frequency Foldback when V_{IN} is close to V_{OUT}. See Circuit in Figure 49, V_{IN} = 9.8V, V_{OUT} = 10V, I_{LOAD} = 1A

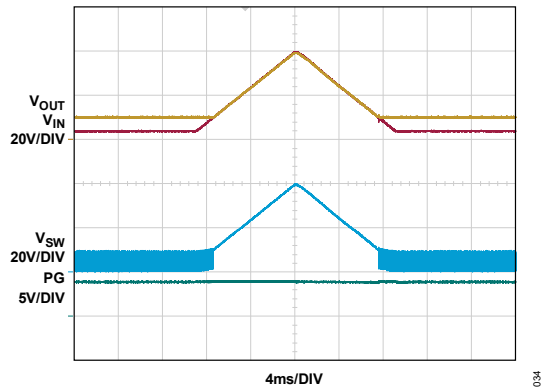


Figure 34. Preboost Line Transient. See Circuit in Figure 49. V_{IN} transient between 3V and 40V, with 1.8A load.

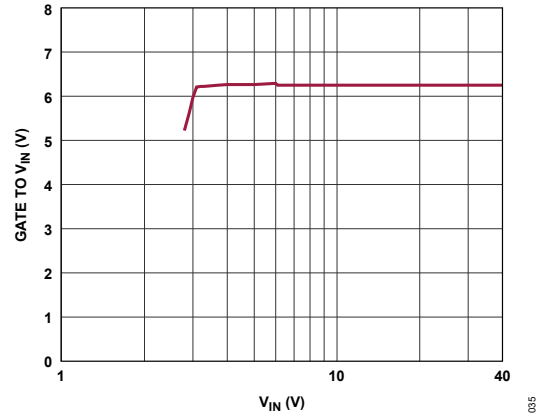


Figure 35. GATE to VIN Regulation Voltage vs V_{IN}

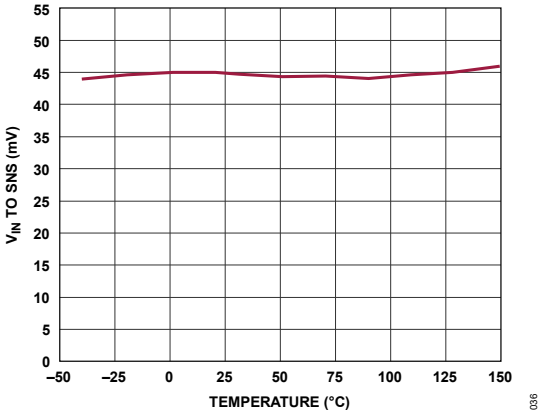


Figure 36. V_{IN} to SNS Threshold Voltage vs Temperature

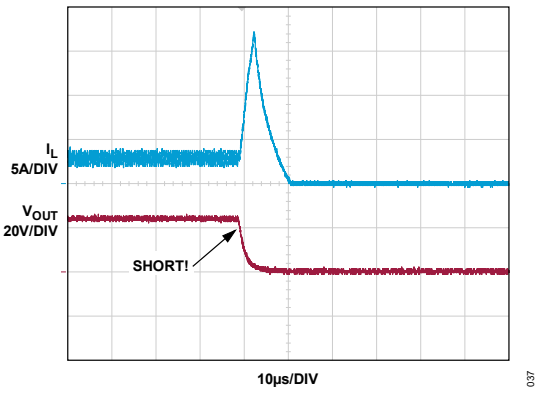


Figure 37. Output Short Circuit Protection. See Figure 1, V_{IN} = 9V.

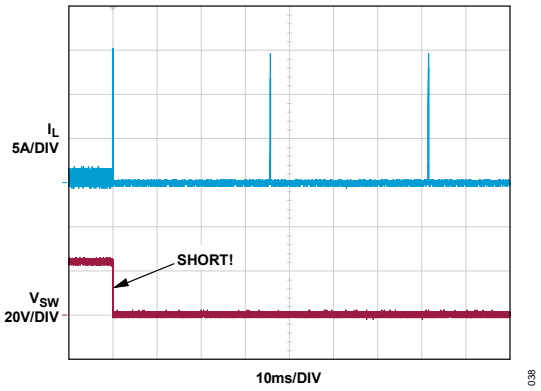


Figure 38. Hiccup during Output Short Circuit. See Figure 1, V_{IN} = 9V.

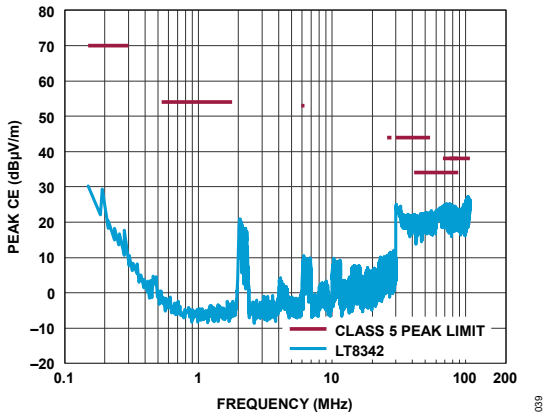


Figure 39. Conducted EMI Performance (CISPR 25 Class 5 Peak). See Circuit in Figure 45. V_{IN} = 12V, V_{OUT} = 24V, I_{LOAD} = 3A. SSFM on. f_{SW} = 2MHz to 2.3MHz.

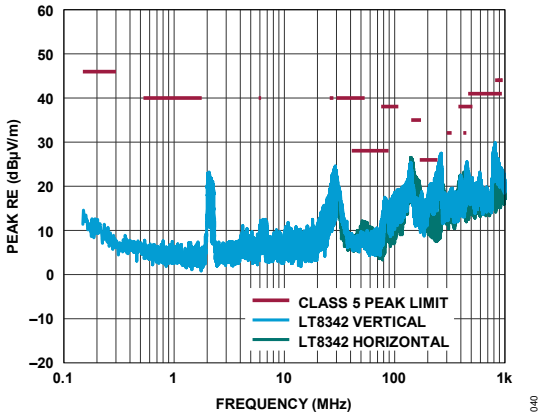


Figure 40. Radiated EMI Performance (CISPR 25 Class 5 Peak). See Circuit in Figure 45. V_{IN} = 12V, V_{OUT} = 24V, I_{LOAD} = 3A. SSFM on. f_{SW} = 2MHz to 2.3MHz.

BLOCK DIAGRAM

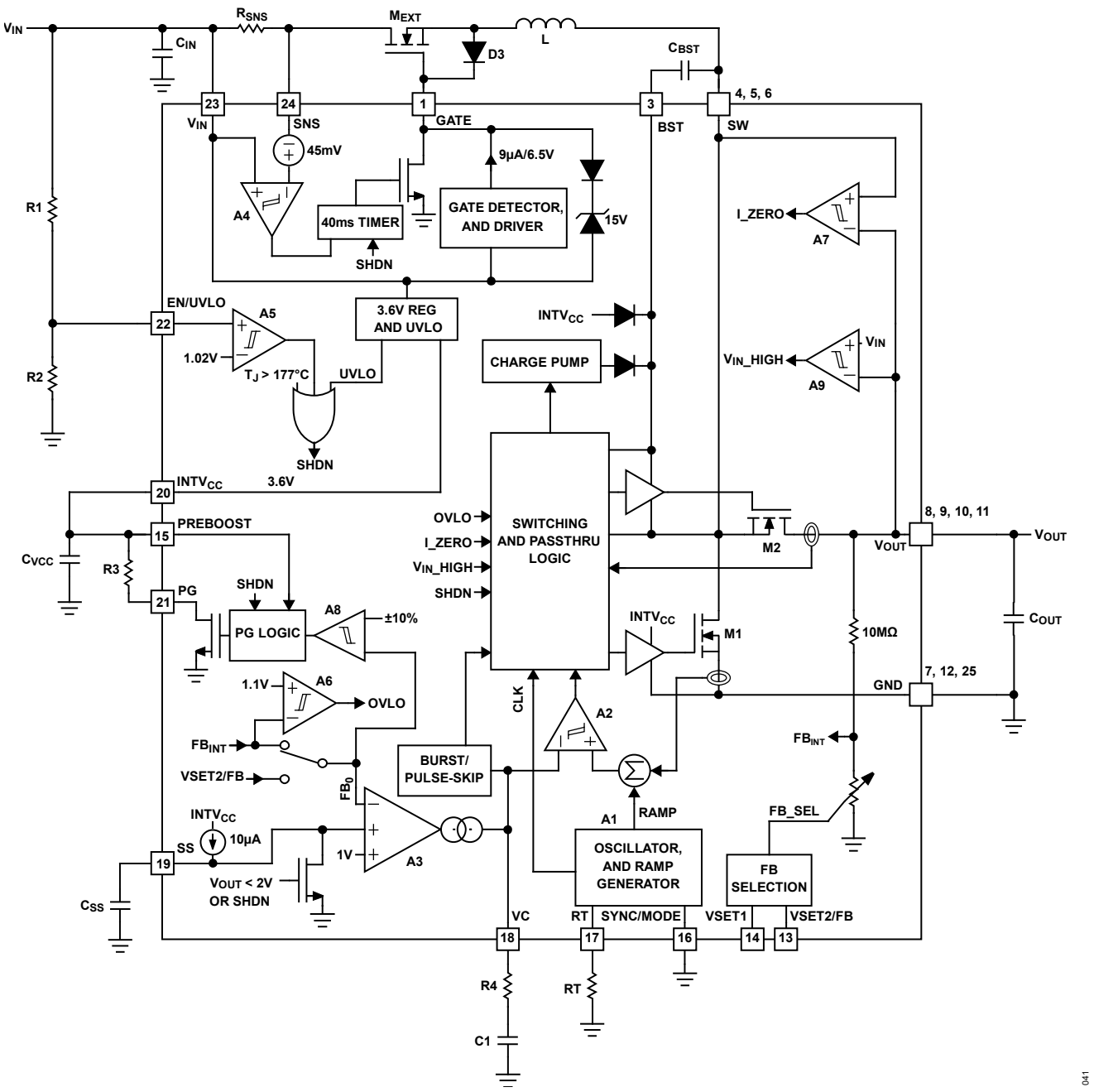


Figure 41. Block Diagram

THEORY OF OPERATION

The LT8342 is a monolithic, synchronous step-up DC/DC converter that uses fixed frequency and peak current mode control to provide excellent line and load regulation. It contains a Silent Switcher architecture that enables a significant reduction in EMI and can be configured to control an optional external input-disconnect N-channel FET (M_{EXT}) for output short-circuit protection and reduction of inrush current.

See the *Block Diagram* for the following explanation of the LT8342's operation. An optional resistor divider from the converter input to the EN/UVLO pin, with a 1.08V rising threshold and an accurate 1.02V falling threshold, allows the user to program turn on/off levels for the converter input. Alternatively, the EN/UVLO pin can be connected to the converter input or driven from an external logic-level signal. EN/UVLO pin voltage below 0.15V shuts down all internal circuitry and draws less than 1µA from the V_{IN} pin.

With the EN/UVLO pin voltage high enough and the V_{IN} pin voltage at least 2.8V, the internal circuitry is activated. The LT8342 will check whether internal feedback (FB_{INT}) or external feedback (VSET2/FB pin) will be used as the feedback node (FB_0). If internal feedback is used, FB_SEL will automatically determine the correct internal feedback ratio accordingly. 10µA from the SS pin will gradually charge up the external soft-start capacitor (C_{SS}), which slowly ramps up the regulation reference voltage. An oscillator (A1), with frequency set using a resistor from the RT pin to GND, turns on the internal bottom power switch (M1) at the beginning of each clock cycle.

Current in the inductor then increases until the bottom switch current comparator (A2) trips and turns off the bottom power switch. The peak inductor current at which the bottom switch turns off is controlled by the voltage on the VC pin. The error amplifier (A3) servos the VC pin by comparing the voltage on the feedback node (FB_0) with the internal 1V reference. The error amplifier drives the VC pin voltage to set the correct peak switch current level that keeps the output voltage in regulation. When the load current increases, it causes a reduction in the feedback node (FB_0) voltage relative to the internal 1V reference. This causes the error amplifier to raise the VC pin voltage, to increase the peak inductor current until enough power is delivered to the output to maintain the output voltage in regulation. When the bottom power switch (M1) turns off, the synchronous power switch (M2) turns on until the next clock cycle begins or the inductor current falls to zero.

For applications requiring a PreBoost regulator to maintain output voltage, for example, during the automotive cold crank or start-stop, the V_{IN} and V_{OUT} pins are constantly monitored to determine when V_{IN} exceeds V_{OUT}. If V_{IN} exceeds V_{OUT} and V_{OUT} is above its programmed regulation voltage, the LT8342 enters PassThru Mode and turns on the top side synchronous switch to maximize efficiency.

Optional output short-circuit protection, and inrush current reduction are available by adding an external sense resistor (R_{SNS}) and an N-channel FET (M_{EXT}) in series with the converter input. If M_{EXT} is not used, connect the GATE pin to GND. The LT8342 can automatically detect whether M_{EXT} is configured.

At startup, an internal 9µA current source charges up the GATE pin (connected to the gate of M_{EXT}) to 6.5V above V_{IN}. During an output short circuit, when the converter input current rises high enough in the sense resistor R_{SNS} to trip the 45mV threshold of comparator A4, the LT8342 pulls the GATE Pin to GND, turning off M_{EXT} and limits the maximum short circuit inductor current. After M_{EXT} is turned off, the LT8342 waits 40ms before charging up the GATE pin to turn on M_{EXT} again.

The LT8342's SYNC/MODE pin allows synchronization to an external clock. It can also be used to select between burst or pulse-skipping modes of operation to optimize the converter performance based on the application requirements. SSFM can be activated with either of the two modes to reduce the EMI further.

The LT8342's protection features include output over-voltage and short-circuit protection, thermal shutdown, and under-voltage lockout. The IC also prevents inductor current runaway in conditions requiring extremely low converter duty cycles by adjusting switching frequency to maintain volt-second balance of the inductor.

APPLICATIONS INFORMATION

Programming V_{IN} Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

System V_{IN} turn-on/-off thresholds can be programmed by driving the EN/UVLO pin with a resistor divider connected from V_{IN} to GND (See *Block Diagram*). The threshold voltages are determined by equations (*1*) and (*2*).

$$V_{(FALLING,TURN\ OFF)} = 1.02V \times \frac{R_1 + R_2}{R_2} \quad (1)$$

$$V_{(RISING,TURN\ ON)} = 1.082V \times \frac{R_1 + R_2}{R_2} \quad (2)$$

When in Burst Mode operation with light load currents, the current through the resistor network R_1 and R_2 can easily be greater than the supply current consumed by the LT8342. Therefore, R_1 and R_2 should be large to minimize their effect on efficiency at low loads.

The EN/UVLO pin can be connected to V_{IN} if the shutdown feature is not used, or alternatively, the pin may be tied to a logic level if shutdown control is required. The IC draws a low V_{IN} quiescent current of 0.35µA (typical) when EN/UVLO is below 0.15V.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.6V supply from VIN that powers the gate drivers and the internal bias circuitry. The INTVCC pin must be bypassed to GND with a minimum of 2.2µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Do not connect any external load to the INTVCC pin.

Programming the Output Voltage

LT8342 features an adjustable internal feedback divider which programs the regulated output voltage level. Configuring VSET1 and VSET2/FB pins as shown in *Table 6* to select the preset level. The >10MΩ (typical) resistor divider guarantees that the quiescent current from the V_{OUT} pin is much reduced compared with a conventional external potential divider.

In some applications where external feedback is still desired, one can tie the VSET1 pin to INTVCC through a 100kΩ resistor, which programs the VSET2/FB pin as the conventional feedback pin. In this case, the output voltage is programmed with a resistor divider between the output and the VSET2/FB pin, as shown in *Figure 1.* Choose the resistor values according to the equation (*3*).

$$R_{FB1} = R_{FB2} \times \left(\frac{V_{OUT}}{1V} - 1\right) \quad (3)$$

The resistance in equation (*3*) refer to reference designators in *Figure 42*. The 1% resistors are recommended to maintain output voltage accuracy. When using large feedback resistors, a 4.7pF to 22pF phase-lead capacitor may be required from V_{OUT} to VSET2/FB. Note that when external feedback is used, if the fault occurs where VSET2/FB is short to ground, instead of producing an excessively high output voltage, as shown in *Table 6*, LT8342 will automatically switch to internal feedback with 19V output regulation.

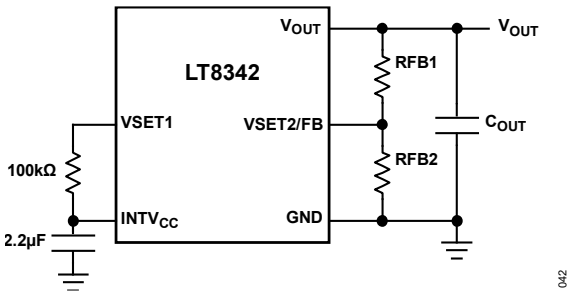


Figure 42. Simplified LT8342 External Feedback Configuration

Light Load Current Operation — Burst Mode or Pulse-Skipping Mode

The LT8342 can be programmed (using the SYNC/MODE pin) to automatically enter Burst Mode during light load to maintain efficiency. In this condition, the LT8342 maintains an inductor peak current at a minimum of 1.6A (typical), reducing the switching frequency as the load decreases. This regulates the output voltage while minimizing the input quiescent current and output voltage ripple. In light load Burst Mode operation, the LT8342 delivers single small pulses of current to the output capacitor, followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode, the LT8342 consumes only 28µA when operating with the external input-disconnect N-Channel FET (M_{EXT}, see *Figure 41*) or 9µA when operating without M_{EXT}. As the output load decreases, the frequency of single current pulses decreases, and the percentage of time the LT8342 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters.

To achieve higher light load efficiency, more energy must be delivered to the output during each single small pulse in Burst Mode operation so that the LT8342 can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen. Increasing the output capacitance will decrease the output ripple proportionally. As the output load ramps upward from zero, the switching frequency will increase until the fixed frequency is defined by the resistor at the RT pin. The output load at which the LT8342 reaches the fixed frequency varies based on input voltage, output voltage, and the choice of inductor.

Pulse-skipping mode offers two major differences from Burst Mode. Firstly, the internal clock stays awake at all times, and all switching cycles are aligned to the clock. In this mode, the internal circuitry is always awake, increasing the V_{IN} pin quiescent current to 1.9mA compared to the 9µA in Burst Mode. Secondly, as the load ramps upward from zero, the switching frequency programmed by the resistor at the RT pin is reached at a lower output load than in the Burst Mode operation. Therefore, the pulse-skipping mode exhibits a lower output ripple across a wider load range.

Programming Switching Frequency and Synchronization

The choice of operating frequency is a trade-off between efficiency and component size. Low-frequency operation improves efficiency by reducing the power switches' switching losses and gate driver current. However, lower-frequency operation requires a physically larger inductor. The LT8342 uses a constant-frequency architecture that can be programmed over a 300kHz to 3MHz range with a single external resistor from the RT pin to ground, as shown in *Figure 41*, the Block Diagram. *Table 7* shows the value of R_T for a given switching frequency.

The operating frequency of the LT8342 can be synchronized to an external clock source with a 100ns minimum pulse width. By providing a digital clock signal to the SYNC/MODE pin, the LT8342 operates at the SYNC pulse frequency and automatically enters pulse-skipping mode operation at light load. If this feature is used, an RT resistor should be chosen to program a switching frequency as close as possible to the SYNC pulse frequency.

Table 7. Switching Frequency (f_{SW}) vs R_T Value

f_{SW} (MHz)	R_T (kΩ)	f_{SW} (MHz)	R_T (kΩ)
0.3	110	1.7	18.2
0.4	84.5	1.8	16.9
0.5	68.1	1.9	15.8
0.6	56.2	2.0	15
0.7	48.7	2.1	14.3
0.8	42.2	2.2	13.7
0.9	36.5	2.3	13
1.0	31.6	2.4	12.4
1.1	28.7	2.5	11.8
1.2	26.1	2.6	11.3
1.3	24.3	2.7	10.7
1.4	22.1	2.8	10.2
1.5	20.5	2.9	9.76
1.6	19.1	3.0	9.53

Spread Spectrum Frequency Modulation

The LT8342 features SSFM to further reduce electromagnetic emissions. The user can select SSFM with Burst Mode operation by connecting the SYNC/MODE pin to ground through a 100kΩ resistor. The user can also select SSFM with pulse-skipping operation by connecting the SYNC/MODE pin to $INTV_{CC}$. When SSFM is selected, a stepped triangular frequency modulation is used to vary the internal oscillator frequency between the value programmed by the R_T resistor to approximately 13% higher than that value. The modulation frequency is approximately 0.45% of the switching frequency. For example, when the LT8342 is programmed to 2MHz, and spread spectrum frequency modulation is selected, the oscillator frequency varies from 2MHz to 2.3MHz at a 9kHz rate (see *Figure 12*, Oscillator Frequency with Spread Spectrum Modulation in the *Typical Performance Characteristics* section).

V_{IN} to V_{OUT} PassThru Mode Operation

In automotive PreBoost applications, the input voltage of the boost converter is normally above the regulated output voltage programmed by the feedback resistor network. Under this condition, the LT8342 enters PassThru mode operation, where the synchronous power switch M2 (See *Block Diagram*) is kept on continuously, and the power switch M1 is kept off continuously. The voltage across the boost capacitor (C_{BST}) is constantly monitored. When it drops below 2.9V, an internal charge pump circuit is turned on to charge the boost capacitor voltage to 3.2V and then turned off, maintaining enough gate drive voltage on M2.

In PassThru mode, the LT8342 intelligently enters a low quiescent current state regardless of the SYNC/MODE pin's configuration. Input quiescent current can be as low as 26.5µA with the input-disconnect FET (M_{EXT}), or 12µA without M_{EXT}. Note that if the input voltage exceeds 110% of the target output voltage, the PG pin will pull low to indicate that V_{OUT} is out of regulation. If PG is externally pulled up, the current through the pull-up resistor can be more significant than the quiescent current of LT8342. To further reduce the power consumption in PassThru, one

can connect the PREBOOST pin to $INTV_{CC}$, so that PG no longer pulls low in PassThru operation when output voltage is above regulation.

When the input voltage drops sharply (such as during stop-start or cold crank) to a level below the voltage stored on the output capacitor of the boost converter, reverse inductor current exceeding −1.8A (typical) will cause M2 to turn off. The output capacitor will naturally discharge due to load current. The LT8342 PassThru mode is maintained as long as V_{OUT} remains above its programmed regulation level, regardless of the level of V_{IN}.

The LT8342 can only exit PassThru mode when V_{OUT} drops below its programmed regulation level, which turns on M1 and turns off M2. The LT8342 will then quickly respond as a boost converter to maintain V_{OUT} at its programmed level.

To ensure the PassThru mode operation works properly, the LT8342's V_{IN} pin must be connected to the input of the boost converter.

Switching Frequency Foldback when V_{IN} Approaches V_{OUT}

In some boost applications, the input voltage may rise to a voltage very close to V_{OUT}. In this condition, the switching regulator must operate at a very low duty cycle to keep output voltage in regulation. However, the minimum on-time limitation of the power switch may prevent the switcher from attaining a sufficiently low duty cycle at the programmed switching frequency. As a result, a typical boost converter may experience a large output ripple under these conditions.

The LT8342 addresses this issue by adopting a switching frequency foldback function to decrease the switching frequency when its minimum on-time starts to limit the switcher from attaining a sufficiently low duty cycle.

Output Short-Circuit Protection

Optional output short-circuit protection is available by adding an external sense resistor (R_{SNS}), and a N-channel FET (M_{EXT}) in series with the converter input. A low-leakage p-n clamp diode (D3) is also required between the source and gate of M_{EXT} (See *Block Diagram*).

At startup, an internal 9µA current source charges up the GATE Pin (connected to the gate of M_{EXT}) to 6.5V above V_{IN}. During an output short circuit, when the converter input current rises high enough in the sense resistor R_{SNS} to trip the 45mV threshold of the comparator A4, the LT8342 pulls the GATE pin to GND, immediately limiting the maximum short-circuit inductor current and eventually turns off M_{EXT}. When the inductor current decreases below zero, the parasitic capacitances on the SW node will cause ringing, possibly creating a big negative gate-to-source voltage (V_{GS}) that could damage the M_{EXT}. The diode D3 protects M_{EXT} by clamping the negative V_{GS} of M_{EXT}. After M_{EXT} is turned off, the LT8342 waits 40ms before charging up the GATE pin to turn on M_{EXT} again. The typical waveforms during output short circuits are shown in *Figure 37* and *Figure 38* in the *Typical Performance Characteristics* section.

When selecting M_{EXT}, the following factors should be taken into consideration:

- The drain-to-source voltage and current ratings should be sufficient for the intended application. Typically, a 40V V_{DS_MAX} and an I_{DS_MAX} higher than the over-current limit (45mV/R_{SNS}) are safe.
- The gate-to-source voltage should be rated to 15V or above. Since the internal charge pump operates to drive the GATE pin 6.5V above V_{IN}, V_{GS_MAX} should be at least +15V. The negative maximum rating can be more relaxed because of the clamp diode from source to gate.
- A gate threshold voltage (V_{GS_TH}) of less than 1.8V is recommended.
- The gate-to-drain charge (Q_{GD}) should be large enough to reduce in-rush current. During the start-up of M_{EXT}, and when V_{GS} just exceeds V_{GS_TH}, all the 9µA charging current flows into the gate-to-drain capacitance

(C_{RSS}) while V_{GS} remains roughly the same. The source voltage V_S, which also acts as the input of the inductor, will ramp up quickly to the drain voltage V_{IN}. Since V_{OUT} is initially at ground, an in-rush current will occur and must be kept below the output short current programmed by R_{SNS}. Note that a larger Q_{GD} might be needed as C_{OUT} or V_{IN} increases.

- Low on-resistance (R_{DSON}) for optimum efficiency; For most applications, M_{EXT} does not have a Safe Operating Area (SOA) violation problem as long as its I_{DS_MAX} is well above the short-circuit current limit. This is because the LT8342 does not regulate M_{EXT}'s current and only turns it off once the limit is reached. In addition, the strong pull-down strength on the GATE pin ensures that excess current only lasts for a very short period, thus limiting the amount of stress on M_{EXT}. The 40ms time-out period before retrying ensures heat is well dissipated.

Start-Up

To limit the peak switch current and V_{OUT} overshoot during start-up, the LT8342 uses an SS pin to provide soft-start operation (see the error amplifier A3 in *Block Diagram*). During soft-start, a 10µA (typical) current source gradually charges the external soft-start capacitor C_{SS}. When the SS pin voltage falls between the FB initial voltage and 1V, the IC regulates the FB pin voltage to the SS pin voltage instead of 1V. This way, the output capacitor is charged gradually toward its final value while limiting the start-up peak switch currents.

The IC selects pulse-skipping mode with no spread spectrum frequency modulation during start-up, and the SYNC/MODE pin configuration is ignored. The IC reads the SYNC/MODE pin configuration after the SS pin voltage exceeds 1.2V (typical).

When the external disconnect FET (M_{EXT}) is used, at power up and EN/UVLO high, the hiccup timer will count 40ms (typical) before turning on M_{EXT} and starting SS pin operation. In case the system is stuck in an under-voltage reset loop when a certain fault happens, this mechanism guarantees sufficient hiccup time between retries to protect M_{EXT} from overheating, even when the IC keeps being reset. If M_{EXT} is not used (GATE ties to ground), no hiccup delay is inserted between enable and start-up. See *Figure 20* and *Figure 21* in the *Typical Performance Characteristics* section for comparing start-up operations under different configurations.

Loop Compensation

Loop compensation determines stability and transient performance. The LT8342 uses peak current mode control to regulate the output, simplifying loop compensation.

To compensate for the feedback loop of the LT8342, a series resistor-capacitor network is usually connected from the VC pin to GND. The *Block Diagram* shows the typical VC compensation network. For most applications, the capacitor should be in the range of 100pF to 10nF, and the resistor should be in the range of 5kΩ to 200kΩ. A small capacitor is often connected in parallel with the RC compensation network to attenuate the VC voltage ripple, which is induced from the output voltage ripple passing all the way through the feedback resistor network and the internal error amplifier. The parallel capacitor usually ranges in value from 2.2pF to 22pF. A practical approach to design the compensation network is to start with one of the circuits in this data sheet, which is close to your application, and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage, and temperature. Refer to the **Application Note 76** for more details.

Thermal Considerations

Care should be taken in the layout of the PCB to ensure good thermal management of the LT8342. The power ground plane should consist of large copper layers with thermal vias; these layers spread heat dissipated by the LT8342. Placing additional vias can further reduce thermal resistance. The maximum load current should be de-

rated as the ambient temperature approaches the maximum junction temperature rating. Power dissipation within the LT8342 (P_{DISS}) can be estimated by subtracting the power losses of the inductor and the sense resistor plus NMOS (if used) from the total power losses calculated in an efficiency measurement. The junction temperature of the LT8342 can then be estimated by equation (4).

$$T_{JUNCTION} = T_{AMBIENT} + \theta_{JA} \times P_{DISS} \quad (4)$$

Thermal Lockout

If the LT8342 die temperature reaches 177°C (typical), the part will stop switching and enter thermal lockout. When the die temperature drops below 170°C (typical), the part will resume switching with a soft-started inductor peak current.

Inductor Selection

When operating in continuous conduction mode (CCM), the duty cycle can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage given by equation (5).

$$D_{MAX} = \frac{V_{OUT} - V_{IN,MIN}}{V_{OUT}} \quad (5)$$

Discontinuous conduction mode (DCM) provides higher conversion ratios at a given frequency at the cost of reduced efficiencies and higher switching currents.

The inductor ripple current ΔIL directly affects the choice of the inductor value, the converter's maximum output current capability, and the light load efficiency in the Burst Mode operation. Choosing smaller values of ΔI_L increases output current capability and light load efficiency in Burst Mode operation, but it requires a large inductance value and reduces the current loop gain. Accepting larger values of ΔI_L provides a fast transient response and allows the use of low inductance values but results in higher input current ripple, greater core losses, lower light load efficiency in Burst Mode operation, and lower output current capability. Large values of ΔI_L at high-duty cycle operation may result in sub-harmonic oscillation.

Given an operating input voltage range and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined by equation (6).

$$L = \frac{V_{IN,MIN}}{\Delta I_L \times f_{SW}} \times D_{MAX} \quad (6)$$

The LT8342 limits the peak switching current to protect the switches and the system from overload faults. The bottom switch current limit is controlled to 10.3A (typical) regardless of the duty cycle. The peak inductor current is equal to the LT8342 bottom switch current limit. The user should choose an inductor with sufficient saturation and RMS current ratings to handle the inductor's peak current.

Input Capacitor Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current) because this current is continuous. The voltage rating of the input capacitor, C_{IN}, should comfortably exceed the maximum input voltage. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance.

The RMS C_{IN} ripple current can be estimated by equation (7).

$$I_{RMS,CIN} = 0.3 \times \Delta I_L \quad (7)$$

Output Capacitor Selection

The output capacitor has two essential functions. First, it filters the LT8342's discontinuous top switch current to produce the DC output. In this role, it determines the output ripple; thus, low impedance at the switching frequency is important. The second function is storing energy to satisfy the transient loads and stabilizing the LT8342's control loop. The X5R or X7R type ceramic capacitors have very low equivalent series resistance (ESR), which provides low output voltage ripple as well as good transient response. Transient performance can be improved with larger output capacitance and the addition of a feedforward capacitor placed between VOUT and VSET2/FB (if external feedback is used). When a feedforward capacitor is used, or output capacitance is adjusted, a careful evaluation of system stability should be made to ensure adequate design margin. Increasing the output capacitance will also decrease the output voltage ripple. Lower value of output capacitance can be used to save space and cost, but transient performance will suffer, and loop instability may result.

In addition to the bulk output capacitors, two small output ceramic capacitors, 0.1µF each, should be placed as close as possible to the IC to complete the Silent Switcher cancellation loops.

See the Board Layout section for more details. Note that larger output capacitance is required when a lower switching frequency is used. If there is significant inductance to the load due to long wires or cables, additional bulk capacitance may be necessary, which can be implemented with an electrolytic capacitor. When choosing a capacitor, special attention should be given to the capacitor's datasheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor, or one with a higher voltage rating, may be required. For good starting values, see the *Typical Applications* section.

Recommended PCB Layout Guidelines

The LT8342 is specifically designed to minimize electromagnetic emissions and maximize efficiency when switching at high frequencies. *Figure 43* shows a recommended PCB layout. For more details and PCB design files, refer to the demo board guide for the LT8342.

For optimal performance, the LT8342 requires the use of multiple output bypass capacitors. It is recommended to connect one 0.1µF capacitor between V_{OUT} at Pin 8 and GND at Pin 7 only, and a matching 0.1µF capacitor between VOUT at Pin 11 and GND at Pin 12 only, to complete the Silent Switcher EMI cancellation loops. These two capacitors must be placed as close as possible to the IC, and the loops formed by these two capacitors should be symmetrical and as small as possible to achieve an optimized EMI cancellation performance. Capacitors with small case sizes, such as 0402 or 0603, are optimal due to the low parasitic inductance. Additional bulk capacitors of 4.7µF or more should be placed close to the IC, with the positive terminals connected to the output, and negative terminals connected to ground plane. The bypass capacitors for V_{IN} and $INTV_{CC}$ pins should also be connected to the ground plane.

The output capacitors, along with the inductor and input capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken power ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible to minimize EMI.

Keep the VSET2/FB (if external feedback is used) and RT nodes small so that the ground traces will shield them from the noise generated by the SW and BST nodes.

The exposed pad on the bottom of the package should be soldered to the ground plane to reduce the package's thermal resistance. To keep the thermal resistance low, extend the ground plane as much as possible, and add many thermal vias to additional power ground planes within the circuit board.

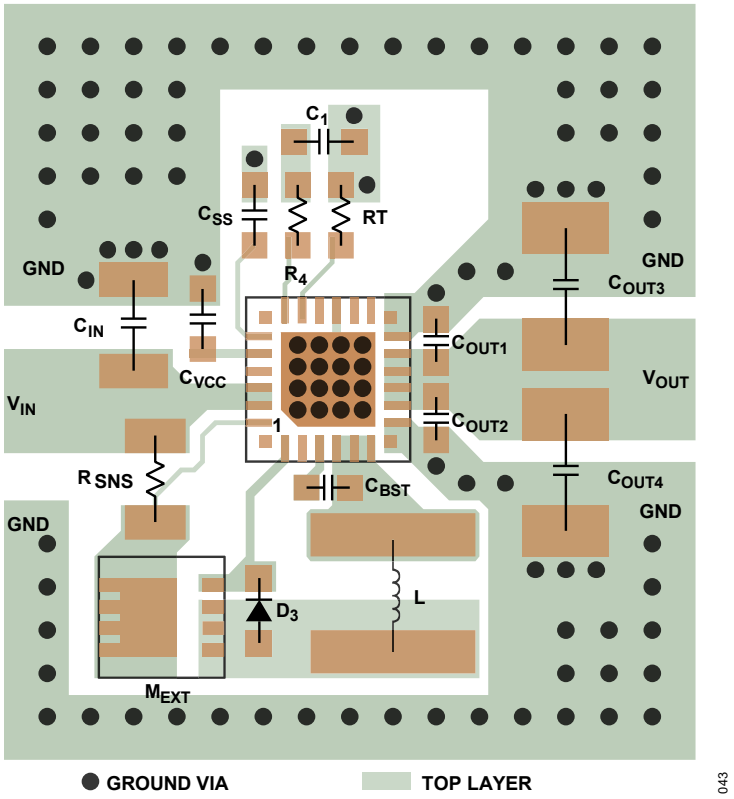


Figure 43. Recommended PCB Layout for LT8342

TYPICAL APPLICATIONS

Low I_Q, Low EMI 24V Boost Converter with SSFM

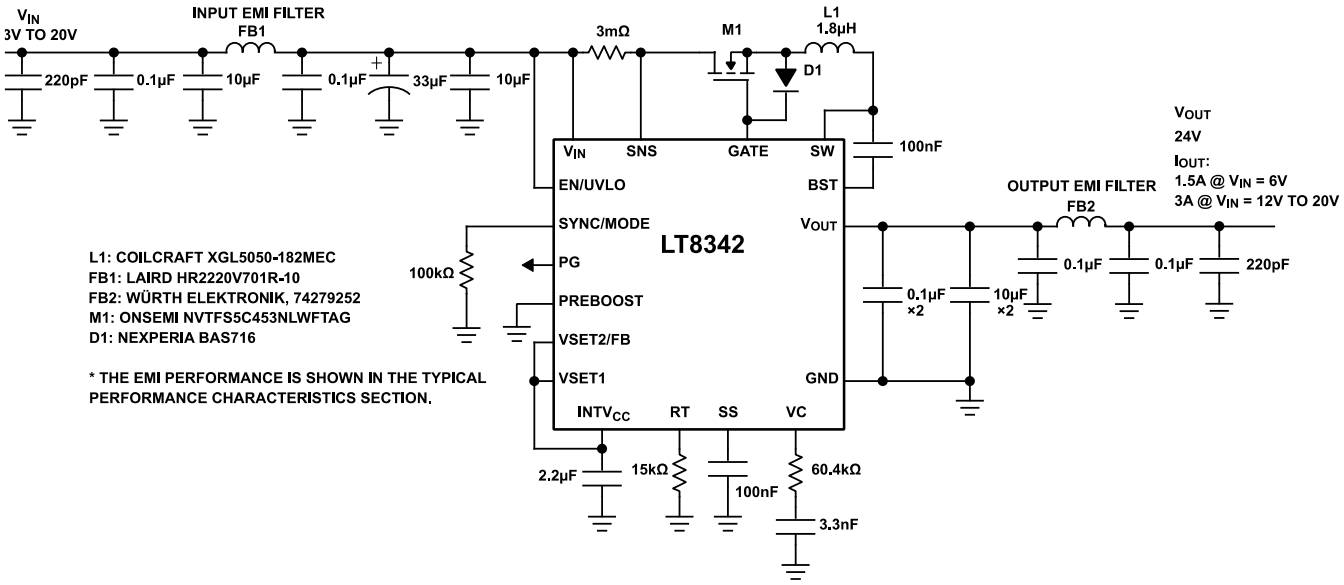


Figure 44. Low I_Q, low EMI, 24V Boost Converter with SSFM and Burst Mode.

2MHz, 12V, Boost Converter

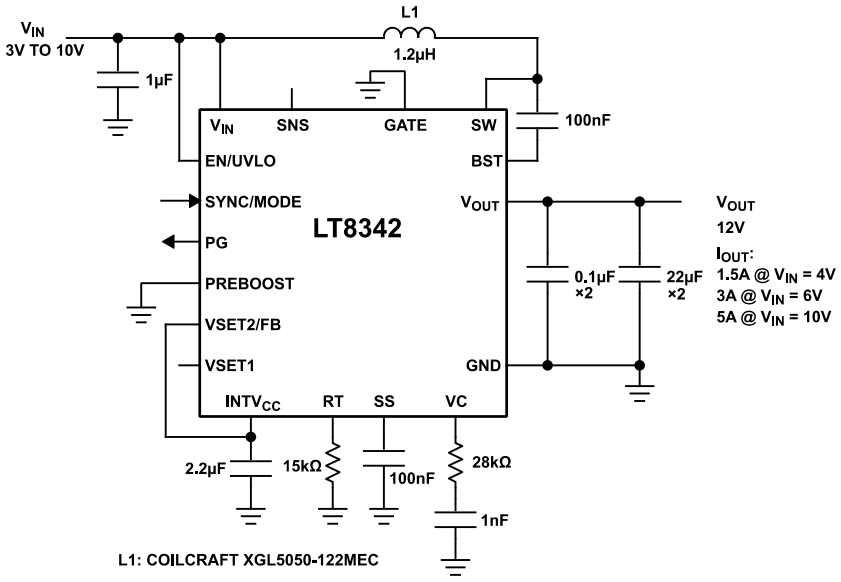


Figure 45. Low I_Q, 2MHz, 12V Boost Converter

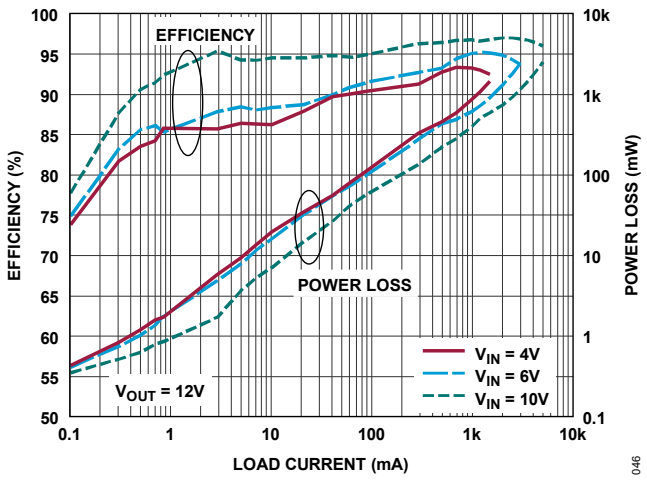


Figure 46. Efficiency vs Load Current of 2MHz, 12V Boost Converter in Burst Mode (SYNC/MODE = 0V).

500kHz, 36V Low I_Q Boost Converter with Output Short Circuit Protection

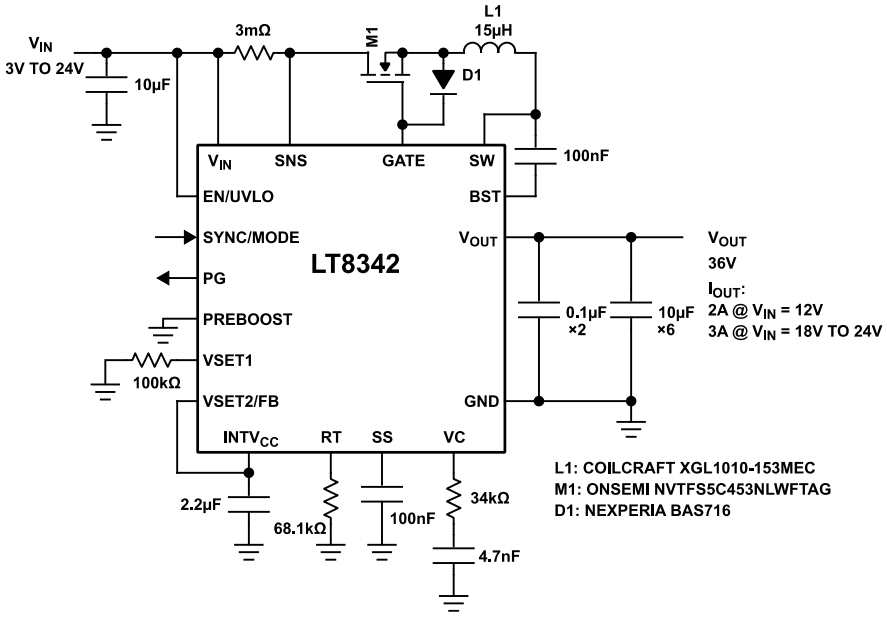


Figure 47. 500kHz, 36V Low I_Q Boost Converter with Output Short Circuit Protection

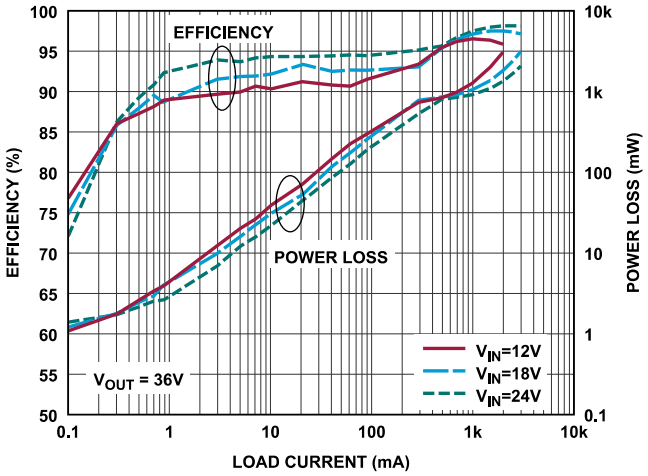


Figure 48. Efficiency vs Load Current of 500kHz, 36V Boost Converter in Burst Mode (SYNC/MODE = 0V).

Automotive 2MHz Pre-Boost Converter for Stop-Start and Cold Crank with 10V Output and Short Circuit Protection

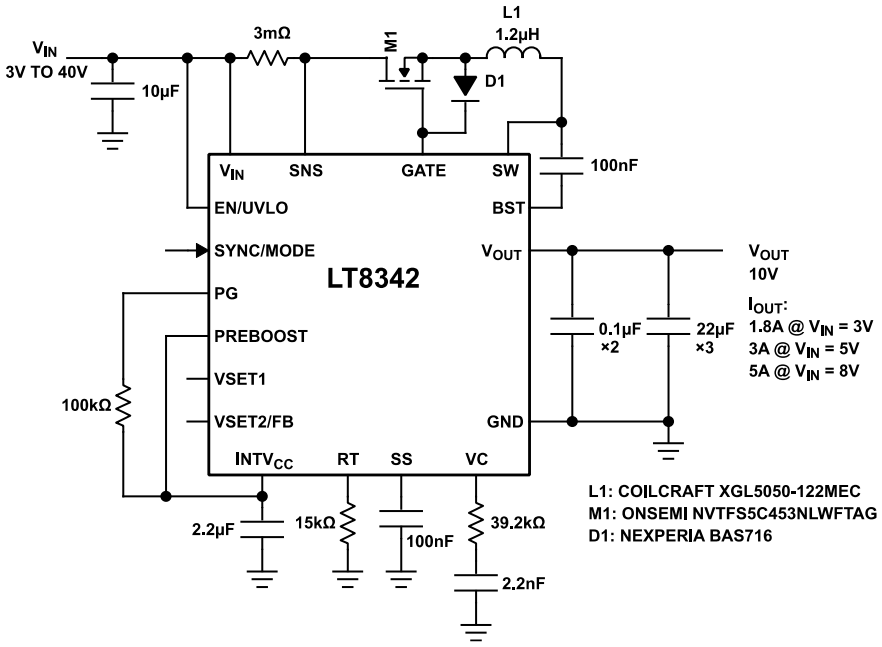


Figure 49. Automotive 2MHz Pre-Boost Converter with 10V Output and Short-Circuit Protection

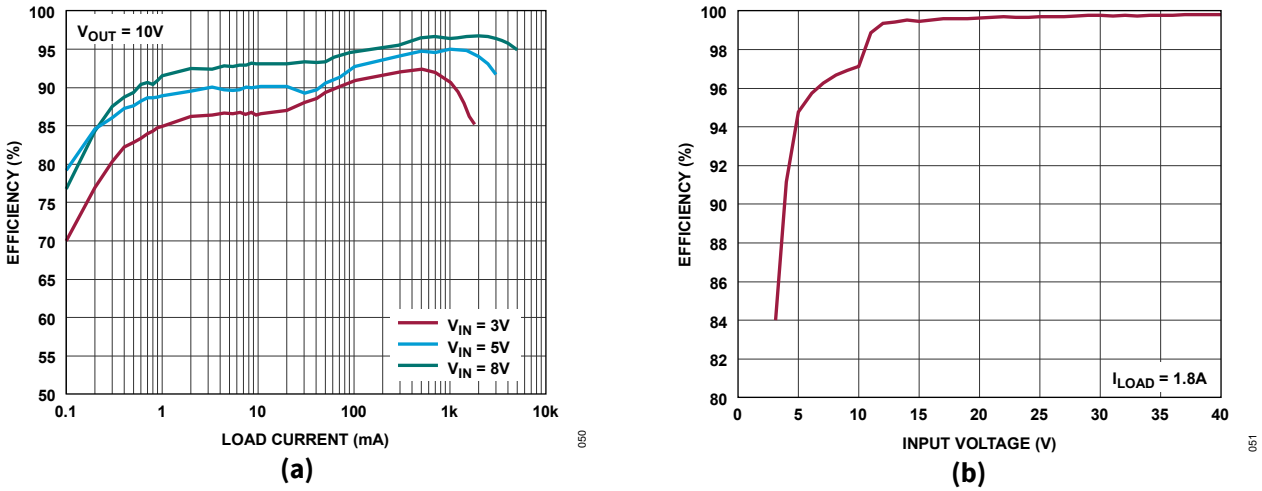
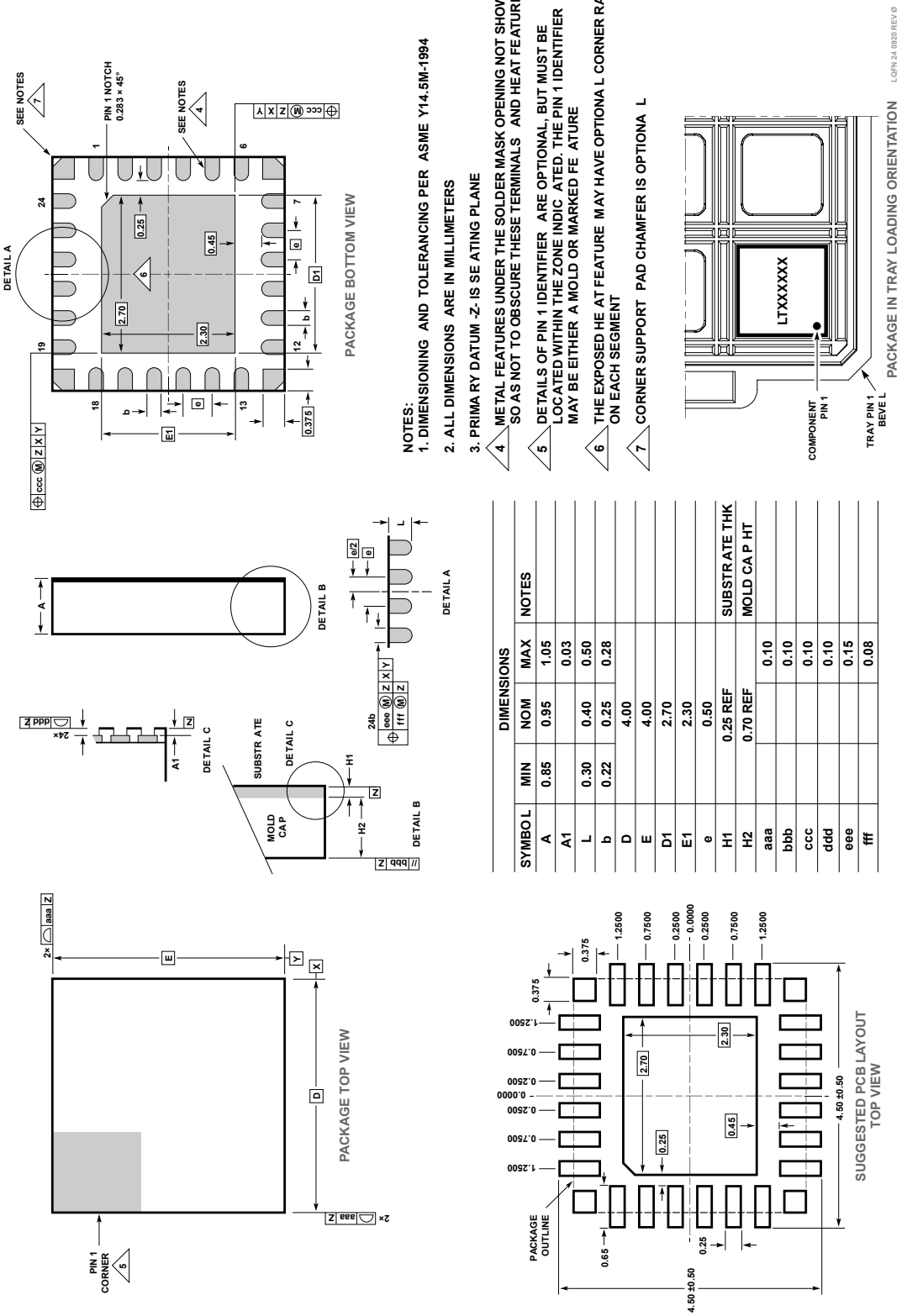


Figure 50. Efficiency of 2MHz 10V Automotive Pre-Boost Converter in Burst Mode (SYNC/MODE = 0V). (a) vs Load Current; (b) vs Input Voltage at 1.8A load current.

PACKAGE INFORMATION



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		4.00		
E		4.00		
D1		2.70		
E1		2.30		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

ORDER INFORMATION

Table 8. Ordering Guide

TAPE AND REEL	TAPE AND REEL (MINI)	PART MARKING*	PAD FINISH	PACKAGE TYPE**	MSL RATING	TEMPERATURE RANGE
LT8342RV#TRPBF	LT8342RV#TRMPBF	8342	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	−40°C to 150°C

*Temperature grades are identified by a label on the shipping container.
**The LT8342 package has the same dimensions as a standard (4mm x 4mm) QFN package.

RELATED PARTS

Table 9. Ordering Guide

PART NUMBER	DESCRIPTION	COMMENTS
LT8336	40V, 2.5A, Low I_Q Synchronous Step-up Silent Switcher with PassThru™	V_{IN}: 2.7V to 40V, $V_{OUT(MAX)}$ = 40V, I_Q = 4µA (Burst Mode Operation), 300kHz to 3MHz Programmable, 16-Lead, 3mm x 3mm LQFN packages
LT8337/ LT8337-1	28V, 5A, Low I_Q Synchronous Step-Up Silent Switcher with PassThru™	V_{IN}: 2.7V to 28V, $V_{OUT(MAX)}$ = 28V, I_Q = 4µA (Burst Mode Operation), 300kHz to 3MHz Programmable, 16-Lead, 3mm x 3mm, LQFN Package
LT8338	40V, 1.2A, Low I_Q Synchronous Step-Up Converter	V_{IN}: 3V to 40V, $V_{OUT(MAX)}$ = 40V, I_Q = 6µA (Burst Mode Operation), 300kHz to 3MHz Programmable, MSOP-10E Package
LT3957/ LT3957A	Boost, Flyback, SEPIC, and Inverting Converter with 5A/40V Switch	V_{IN}: 3V to 40V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN-36 Package
LT3958	High Input Voltage, Boost, Flyback, SEPIC and Inverting Converter with 3.5A/80V Switch	V_{IN}: 5V to 80V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN-36 Package
LT8330	60V, 1A, Low I_Q Boost/SEPIC/Inverting 2MHz Converter	V_{IN} = 3V to 40V, $V_{OUT(MAX)}$ = 60V, I_Q = 6µA (Burst Mode Operation), 6-Lead, TSOT-23, 3mm x 2mm DFN packages
LT8362	60V, 2A Low I_Q Boost/SEPIC/Inverting Converter	V_{IN} = 2.8V to 60V, $V_{OUT(MAX)}$ = 60V, I_Q = 9µA (Burst Mode Operation), MSOP-16(12)E, 3mm × 3mm DFN-10 packages
LT8364	60V, 4A Low I_Q Boost/SEPIC/Inverting Converter	V_{IN} = 2.8V to 60V, $V_{OUT(MAX)}$ = 60V, I_Q = 9µA (Burst Mode Operation), MSOP-16(12)E, 4mm × 3mm DFN-12 packages