

## Description

The 8V19N490 is a fully integrated FemtoClock® NG jitter attenuator and clock synthesizer designed as a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards. The device is optimized to deliver excellent phase noise performance as required in GSM, WCDMA, LTE, and LTE-A radio board implementations. The device supports JESD204B subclass 0 and 1 clocks.

A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the VCXO-PLL output signal and synthesizes the target frequency.

The device supports the clock generation of high-frequency clocks from the selected VCO and low-frequency synchronization signals (SYSREF). SYSREF signals are internally synchronized to the clock signals. Delay functions exist for achieving alignment and controlled phase delay between system reference and clock signals and to align/delay individual output signals. The four redundant inputs are monitored for activity. Four selectable clock switching modes are provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for flexibility.

The device is configured through a 3-wire SPI interface and reports lock and signal loss status in internal registers and via a lock detect (LOCK) output. Internal status bit changes can also be reported via the nINT output. The 8V19N490 is ideal for driving converter circuits in wireless infrastructure, radar/imaging, and instrumentation/medical applications. The device is a member of the high-performance clock family from IDT.

## Typical Applications

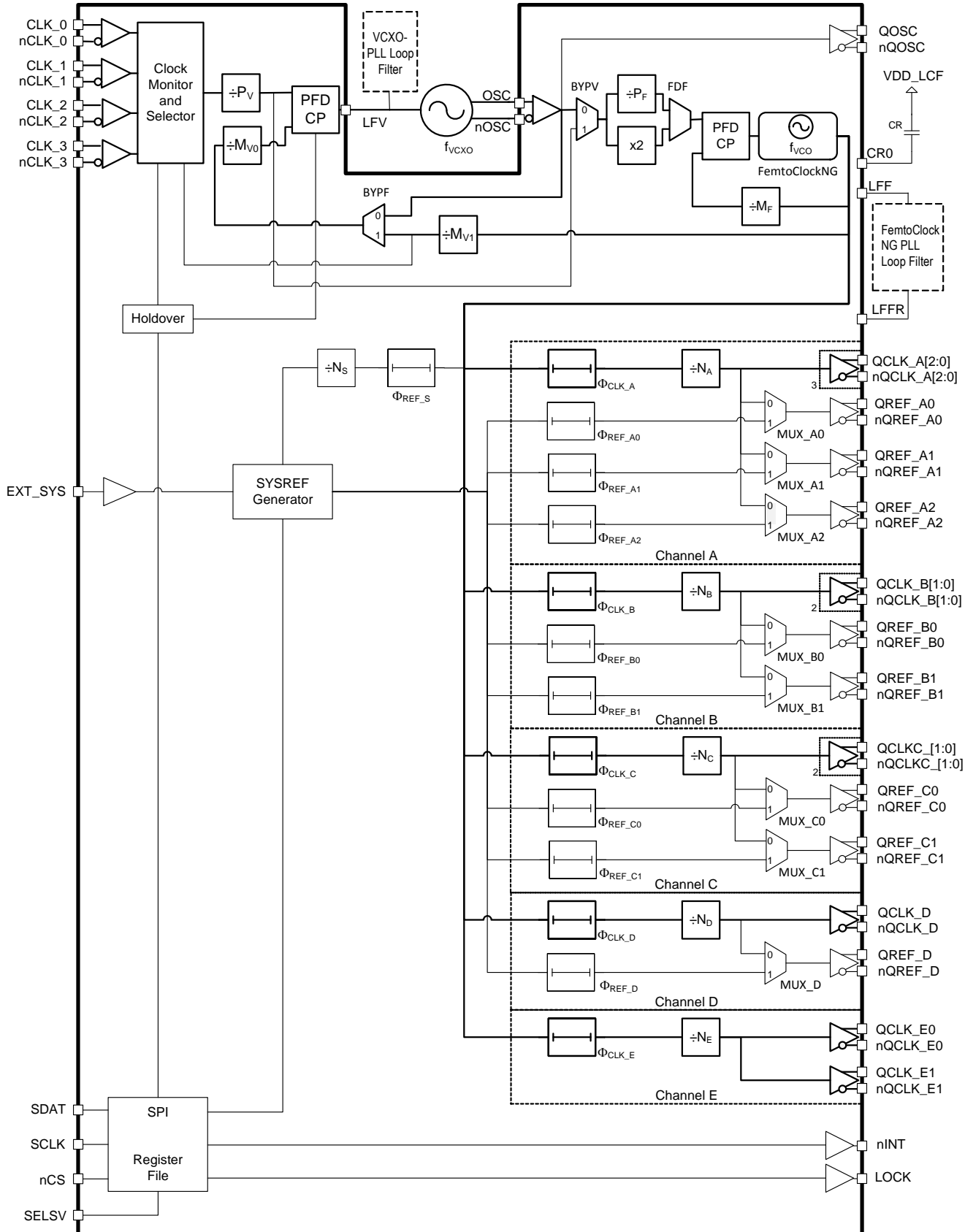
- Wireless infrastructure applications: GSM, WCDMA, LTE, LTE-A
- Ideal clock driver for jitter-sensitive ADC and DAC circuits
- Low-phase noise clock generation
- Ethernet line cards
- Radar and imaging
- Instrumentation and medical

## Features

- High-performance clock RF-PLL with support for JESD204B
- Optimized for low-phase noise: -150dBc/Hz (800kHz offset; 245.76MHz clock)
- Integrated phase noise of 80fs RMS typical (12kHz–20MHz)
- Dual-PLL architecture
- First PLL stage with external VCXO for clock jitter attenuation
- Second PLL with internal FemtoClock NG PLL: 2949.12MHz
- Six output channels with a total of 19 outputs, organized in:
  - Four JESD204B channels (device clock and SYSREF output) with two, four and six outputs
  - One clock channel with two outputs
  - One VCXO output
- Configurable integer clock frequency dividers
- Supported clock output frequencies include: 2949.12, 1474.56, 983.04, 491.52, 245.76, and 122.88MHz
- Low-power LVPECL/LVDS outputs support configurable signal amplitude, DC and AC coupling and LVPECL, LVDS line terminations techniques
- Phase delay circuits:
  - Clock phase delay with 256 steps of 339ps and a range of 0 to 86.466ns
  - Individual SYSREF phase delay with 8 steps of 169ps
  - Additional individual SYSREF fine phase delay with 25ps steps
  - Global SYSREF signal delay with 256 steps of 339ps and a range of 0 to 86.466ns
- Redundant input clock architecture with four inputs, including:
  - Input activity monitoring
  - Manual and automatic, fault-triggered clock selection modes
  - Priority controlled clock selection
  - Digital holdover and hitless switching
  - Differential inputs accept LVDS and LVPECL signals
- SYSREF generation modes include internal and external trigger mode for JESD204B
- Supply voltage: 3.3V
- SPI and control I/O voltage: 1.8V/3.3V (selectable)
- Package: 11 × 11mm 100-CABGA
- Temperature range: -40°C to +85°C

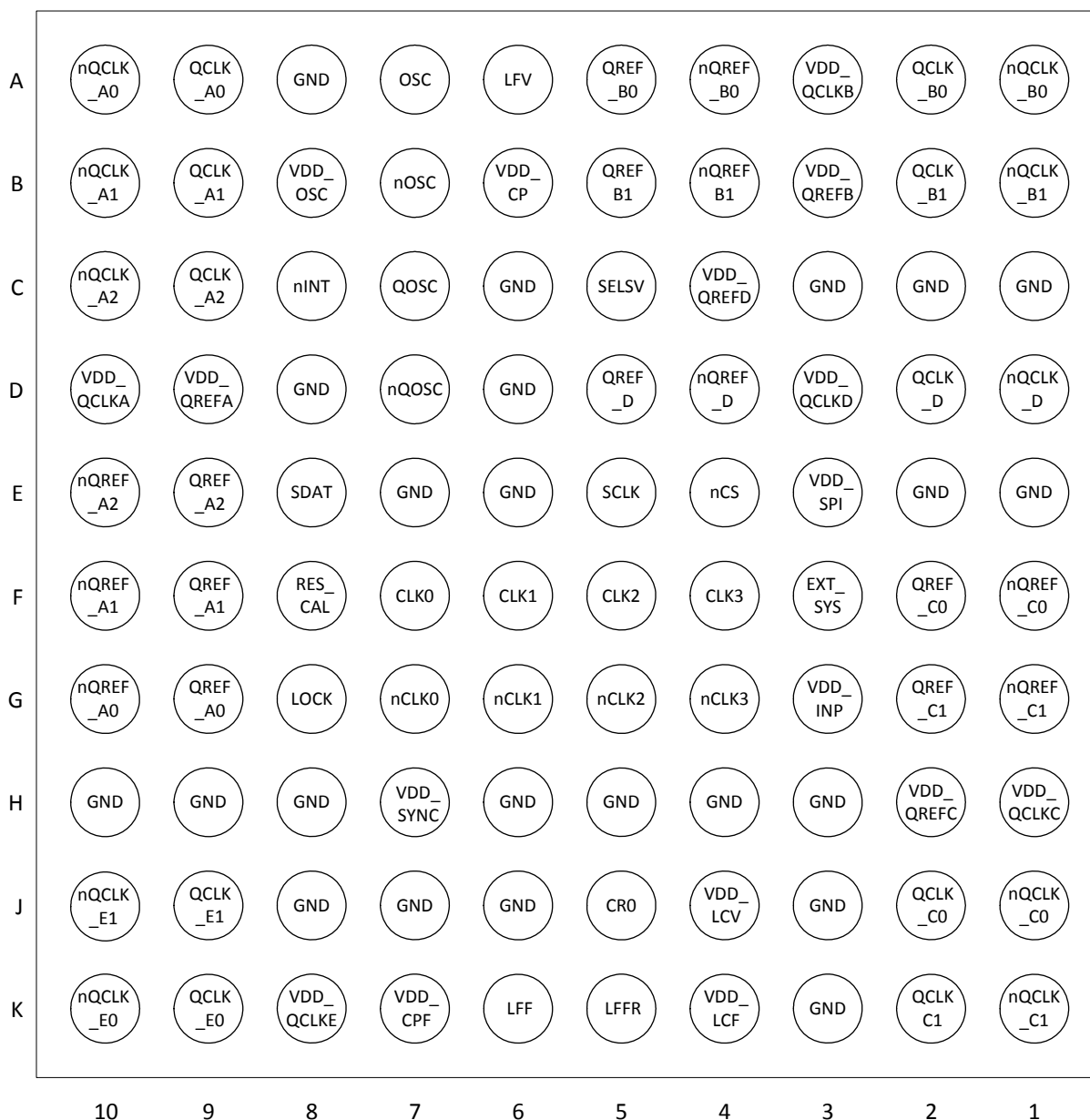
# Block Diagram

Figure 1. Block Diagram ( $f_{VCO} = 2949.12\text{MHz}$ )



# Ball Map

Figure 2. Ball Map for 11 × 11 × 1.2mm 100-CABGA Package with 1mm Ball Pitch (Bottom View)



## Pin Descriptions

Table 1. Pin Descriptions [a]

Ball	Name	Type <sup>[b]</sup>	Description
F7	CLK_0	Input (PD)	Device clock 0 inverting and non-inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
G7	nCLK_0	Input PD/PU	
F6	CLK_1	Input (PD)	Device clock 1 inverting and non-inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
G6	nCLK_1	Input PD/PU	
F5	CLK_2	Input (PD)	Device clock 2 inverting and non-inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
G5	nCLK_2	Input PD/PU	
F4	CLK_3	Input (PD)	Device clock 3 inverting and non-inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
G4	nCLK_3	Input PD/PU	
A9, A10	QCLK_A0, nQCLK_A0	Output	Differential clock output A0 (Channel A). Configurable LVPECL/LVDS style and amplitude.
B9, B10	QCLK_A1, nQCLK_A1	Output	Differential clock output A1 (Channel A). Configurable LVPECL/LVDS style and amplitude.
C9, C10	QCLK_A2, nQCLK_A2	Output	Differential clock output A2 (Channel A). Configurable LVPECL/LVDS style and amplitude.
G9, G10	QREF_A0, nQREF_A0	Output	Differential SYSREF/clock output REF_A0 (Channel A). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
F9, F10	QREF_A1, nQREF_A1	Output	Differential SYSREF/clock output REF_A1 (Channel A). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
E9, E10	QREF_A2, nQREF_A2	Output	Differential SYSREF/clock output REF_A2 (Channel A). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
A2, A1	QCLK_B0, nQCLK_B0	Output	Differential clock output B0 (Channel B). Configurable LVPECL/LVDS style and amplitude.
B2, B1	QCLK_B1, nQCLK_B1	Output	Differential clock output B1 (Channel B). Configurable LVPECL/LVDS style and amplitude.
A5, A4	QREF_B0, nQREF_B0	Output	Differential SYSREF/clock output REF_B0 (Channel B). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
B5, B4	QREF_B1, nQREF_B1	Output	Differential SYSREF/clock output REF_B1 (Channel B). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
J2, J1	QCLK_C0, nQCLK_C0	Output	Differential clock output C0 (Channel C). Configurable LVPECL/LVDS style and amplitude.
K2, K1	QCLK_C1, nQCLK_C1	Output	Differential clock output C1 (Channel C). Configurable LVPECL/LVDS style and amplitude.

Table 1. Pin Descriptions (Cont.)<sup>[a]</sup>

Ball	Name	Type <sup>[b]</sup>	Description
F2, F1	QREF_C0, nQREF_C0	Output	Differential SYSREF/clock output REF_C0 (Channel C). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
G2, G1	QREF_C1, nQREF_C1	Output	Differential SYSREF/clock output REF_C1 (Channel C). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
D2, D1	QCLK_D, nQCLK_D	Output	Differential clock output D (Channel D). Configurable LVPECL/LVDS style and amplitude.
D5, D4	QREF_D, nQREF_D	Output	Differential SYSREF/clock output REF_D (Channel D). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
K9, K10	QCLK_E0, nQCLK_E0	Output	Differential clock output E0. Configurable LVPECL/LVDS style and amplitude.
J9, J10	QCLK_E1, nQCLK_E1	Output	Differential clock output E1. Configurable LVPECL/LVDS style and amplitude.
C7, D7	QOSC, nQOSC	Output	Differential VCXO-PLL clock outputs. Configurable LVPECL/LVDS style and amplitude.
C8	nINT	Output	Status output pin for signaling internal changed conditions. Selectable 1.8/3.3V LVCMOS interface levels.
G8	LOCK	Output	PLL lock detect status output for both PLLs. Selectable 1.8/3.3V LVCMOS interface levels.
F3	EXT_SYS	Input (PD)	External SYSREF pulse trigger input. Selectable 1.8V/3.3V LVCMOS interface levels.
E8	SDAT	Input/Output (PU)	Serial Control Port SPI Mode Data Input and Output. Selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V and set to input.
E5	SCLK	Input (PD)	Serial Control Port SPI Mode Clock Input. Selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
E4	nCS	Input (PU)	Serial Control Port SPI Chip Select Input. Selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
C5	SELSV	Input (PD)	SPI interface voltage select. 3.3V LVCMOS interface levels. For control input and SPI interface voltage selection (see <a href="#">Table 25</a> ).
J5	CR0	Analog	Internal VCO regulator bypass capacitor. Use a 4.7 $\mu$ F capacitor between the CR0 and the VDD_LCF (K4) terminals.
A6	LFV	Output	VCXO-PLL charge pump output. Connect to the loop filter for the external VCXO.
A7	OSC	Input (PD)	VCXO non-inverting and inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
B7	nOSC	Input PD/PU	
K6	LFF	Output	Loop filter/charge pump output for the FemtoClock NG NG PLL. Connect to the external loop filter.
K5	LFFR	Analog	Ground return path pin for the VCO loop filter.
F8	RES_CAL	Analog	Connect a 2.8 k $\Omega$ (1%) resistor to GND for output current calibration.

Table 1. Pin Descriptions (Cont.)<sup>[a]</sup>

Ball	Name	Type <sup>[b]</sup>	Description
A8, C1, C2, C3, C6, D6, D8, E1, E2, E6, E7, H3, H4, H5, H6, H8, H9, H10, J3, J6, J7, J8, K3	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
D10	VDD_QCLKA	Power	Positive supply voltage (3.3V) for the QCLK_A[2:0] outputs.
D9	VDD_QREFA	Power	Positive supply voltage (3.3V) for the QREF_A[2:0] outputs.
A3	VDD_QCLKB	Power	Positive supply voltage (3.3V) for the QCLK_B[2:0] outputs.
B3	VDD_QREFB	Power	Positive supply voltage (3.3V) for the QREF_B[2:0] outputs.
H1	VDD_QCLKC	Power	Positive supply voltage (3.3V) for the QCLK_C[1:0] outputs.
H2	VDD_QREFC	Power	Positive supply voltage (3.3V) for the QREF_C[1:0] outputs.
D3	VDD_QCLKD	Power	Positive supply voltage (3.3V) for the QCLK_D outputs.
C4	VDD_QREFD	Power	Positive supply voltage (3.3V) for the QREF_D outputs.
K8	VDD_QCLKE	Power	Positive supply voltage (3.3V) for the QCLK_E[1:0] outputs.
E3	VDD_SPI	Power	Positive supply voltage (3.3V) for the SPI interface.
G3	VDD_INP	Power	Positive supply voltage (3.3V) for the differential inputs (CLK0 to CLK3).
J4	VDD_LCV	Power	Positive supply voltage (3.3V).
K4	VDD_LCF	Power	Positive supply voltage (3.3V).
K7	VDD_CPF	Power	Positive supply voltage (3.3V) for internal FemtoClock NG circuits.
B8	VDD_OSC	Power	Positive supply voltage (3.3V) for OSC, nOSC input and QOSC, nQOSC output.
B6	VDD_CP	Power	Positive supply voltage (3.3V) for internal VCXO_PLL circuits.
H7	VDD_SYNC	Power	Positive supply voltage (3.3V).

[a] For essential information on power supply filtering, see [Power Supply Design and Recommend Application Schematics](#).

[b] Pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. For values, see [Table 44](#).

# Principles of Operation

## Overview

The 8V19N490 generates low-phase noise, synchronized clock and SYSREF output signals locked to an input reference frequency. The device contains two PLLs with configurable frequency dividers. The first PLL (VCXO-PLL, suffix V) uses an external VCXO as the oscillator and provides jitter attenuation. The external loop filter is used to set the VCXO-PLL bandwidth frequency in conjunction with internal parameters. The second, low-phase noise PLL (FemtoClock NG, suffix F) multiplies the VCXO-PLL frequency to 2949.12MHz. The FemtoClock NG PLL is completely internal and provides a central timing reference point for all output signals. From this point, fully synchronous dividers generate the output frequencies and the internal timing references for JESD204B support.

The device supports the generation of SYSREF pulses synchronous to the clock signals. There are five channels consisting of clock and/or SYSREF outputs. The clock outputs are configurable with support for LVPECL or LVDS formats and a variable output amplitude. Clock and SYSREF offer adjustable phase delay functionality. Individual outputs and channels and unused circuit blocks support powered-down states for operating at lower power consumption. The register map, accessible through SPI interface with read-back capability controls the main device settings and delivers device status information. For redundancy purpose, there are two selectable reference frequency inputs and a configurable switch logic with priority-controlled auto-selection and holdover support.

## Phase-Locked Loop Operation

### Frequency Generation

[Table 2](#) displays the available frequency dividers for clock generation. The dividers must be set by the user to match input, VCXO and VCO frequency, and to achieve frequency and phase lock on both PLLs. The frequency of the external VCXO is selected by the user; the internal VCO frequency is set to 2949.12MHz. Example divider configurations for typical wireless infrastructure applications are shown in [Table 3](#).

Table 2. PLL Operation and Divider Values

Divider	Range	Operation for $f_{VCO} = 2949.12\text{MHz}$		
		Jitter Attenuation, Dual-PLL with Deterministic Input-to-Output Delay (BYPV = 0, BYPF = 1)	Jitter Attenuation, Dual-PLL (BYPV = 0, BYPF = 0)	Frequency Synthesis (VCXO-PLL Bypassed, BYPV = 1)
VCXO-PLL Pre-Divider $P_V$	$\div 1 \dots \div 4095$ : (12 bit)	Input clock frequency: $f_{CLK} = P_V \times \frac{f_{VCXO}}{P_F} \times \frac{M_F}{M_{V0} \times M_{V1}}$	Input clock frequency: $f_{CLK} = f_{VCXO} \times \frac{P_V}{M_{V0}}$  $M_{V1}$ setting is not applicable to PLL operation.	Input clock frequency: $f_{CLK} = f_{VCO} \times \frac{P_V \times P_F}{M_F}$  $M_{V0}$ and $M_{V1}$ settings are not applicable to the PLL operation.  $P_F$ : Set $P_F$ to 0.5 in above equation if the frequency doubler is engaged by setting FDF = 1.
VCXO-PLL Feedback Divider $M_{V0}$	$\div 1 \dots \div 4095$ : (12 bit)			
PLL Feedback Divider <sup>[a]</sup> $M_{V1}$	$\div 4 \dots \div 511$ : (9 bit)			
FemtoClock NG Pre-Divider $P_F$	$\div 1 \dots \div 63$ : (6 bit)	VCXO frequency: $f_{VCXO} = f_{VCO} \times \frac{P_F}{M_F}$  $P_F$ : Set $P_F$ to 0.5 in above equation if the frequency doubler is engaged by setting FDF = 1.		
FemtoClock NG Feedback Dividers $M_F$	$\div 8 \dots \div 511$ : (9 bit)			
Output Divider $N_x$ ( $x = A, B, C, D, E$ )	$\div 1 \dots \div 160$	Output frequency: $f_{OUT} = \frac{f_{VCO}}{N_x}$		
SYSREF Divider <sup>[b]</sup> $N_S$	$\div 16 \dots \div 5120$ : $\{2, 4\} \times \{2, 4, 8, 16\} \times \{2, 3, 4, 5\}$	SYSREF frequency/rate: $f_{SYSREF} = \frac{f_{VCO}}{N_S}$		

[a] For input monitoring, configure  $M_{V1}$  as described in [Monitoring and LOS of Input Signal](#).

[b] For SYSREF operation, configure SYNC[6:0] as described in [Synchronizing SYSREF and Clock Output Dividers](#).



## VCXO-PLL

The prescaler  $P_V$  and the VCXO-PLLs feedback divider  $M_{V0}$  and  $M_{V1}$  require configuration to match the input frequency to the VCXO-frequency. The BYPF setting allows to route the VCXO-PLLs feedback path through the  $M_{V0}$  divider. Alternatively, the feedback path is routed through the second PLL and both the  $M_{V0}$  and  $M_{V1}$  feedback divider.  $M_{V0}$  has a divider value range of 12 bit;  $M_{V1}$  has 9 bit. The feedback path through the second PLL, in combination with the divider setting  $P_F = \div 1$ , is the preferred setting for achieving deterministic delay from the clock input to the outputs. Multiple divider settings are available to enable support for input frequencies of e.g., 245.76MHz, 122.88MHz, 61.44MHz and 30.72MHz and the VCXO-frequencies of 122.88MHz, 61.44MHz, 38.4MHz, 30.72MHz, and 245.76MHz. In addition, the range of available input and feedback dividers allows to adjust the phase detector frequency independent of the input and VCXO frequencies. In general, the phase detector may be set into the range from 120kHz to the input reference frequency. The VCXO-PLL charge pump current is controllable via registers and can be set in 50 $\mu$ A steps from 50 $\mu$ A to 1.6mA. The VCXO-PLL may be bypassed: the FemtoClock NG PLL locks to the pre-divider input frequency.

Table 3. Example Configurations for  $f_{VCXO} = 122.88\text{MHz}$ <sup>[a]</sup>

Input Frequency (MHz)	VCXO-PLL Divider Settings		$f_{PFD}$ (MHz)
	$P_V$	$M_{V0}$	
245.76	2	1	122.88
	32	16	7.68
	256	128	0.96
	2048	1024	0.12
122.88	1	1	122.88
	16	16	7.68
	128	128	0.96
	1024	1024	0.12

[a] BYPF = 0.

Table 4. Example Configurations for  $f_{VCXO} = 38.4\text{MHz}$ <sup>[a]</sup>

Input Frequency (MHz)	VCXO- PLL Divider Settings		$f_{PFD}$ (MHz)
	$P_V$	$M_{V0}$	
245.76	32	5	7.68
	128	20	1.92
	512	80	0.48
	2048	320	0.12
122.88	16	5	7.68
	64	20	1.92
	256	80	0.48
	1048	320	0.12

[a] BYPF = 0.

Table 5. VCXO-PLL Bypass Settings

BYPV	Operation
0	VCXO-PLL operation.
1	VCXO-PLL bypassed and disabled. The reference clock for the FemtoClock NG PLL is the input clock divided by the pre-divider $P_V$ . The input clock selection must be set to manual by the user. Clock switching and holdover are not defined. The device will not attenuate input jitter. No external VCXO component and loop filter required.

Table 6. PLL Feedback Path Settings

BYPF	Operation <sup>[a]</sup>
0	VCXO-PLL feedback path through the $M_{V0}$ divider. FemtoClock NG feedback path uses the $M_F$ divider.
1	VCXO-PLL feedback path through the $M_{V1} \times M_{V0}$ dividers. FemtoClock NG feedback path uses the $M_F$ divider. Preferred setting for achieving deterministic delay from input to the outputs.

[a] Regardless of the selected internal feedback path, the  $M_{V1}$  divider should be set to match its internal output frequency to the input reference frequency: the  $M_{V1}$  output signal is the internal reference for input loss-of-signal detect.

## FemtoClock NG PLL

This PLL locks to the output signal of the VCXO-PLL ( $BYPV = 0$ ). It requires configuration of the frequency doubler FDF or the pre-divider  $P_F$  and the feedback divider  $M_F$  to match the VCXO-PLL frequency to the VCO frequency of 2949.12MHz. This PLL is internally configured to high-bandwidth. Best phase noise is typically achieved by engaging the internal frequency doubler ( $FDF = 1$ ). If engaged, the signal from the first PLL stage is doubled in frequency, increasing the phase detector frequency of the FemtoClock NG PLL. Enabling the frequency doubler disables the frequency pre-divider  $P_F$ . If the frequency doubler is not used ( $FDF = 0$ ), the  $P_F$  pre-divider has to be configured. Typically  $P_F$  is set to  $\div 1$  to keep the phase detector frequency as high as possible. Set  $P_F$  to other divider values to achieve specific frequency ratios (1 to 19.2, 1 to 76.8, etc.) between first and second PLL stage.

Table 7. Frequency Doubler

FDF	Operation
0	Frequency doubler off. $P_F$ divides clock signal from VCXO-PLL or input (in bypass).
1	Frequency doubler on. Signal from VCXO-PLL or input (in bypass) is doubled in frequency. $P_F$ divider has no effect.

Table 8. Example PLL Configurations

VCXO-Frequency (MHz)	FemtoClock NG Divider Settings				Output Frequency (MHz)
	FDF	$P_F$	$M_F$	$Nx^{[a]}$	
122.88	x2	–	12	3	983.04
				6	491.52
				12	245.76
				24	122.88
122.88	–	1	24	3	983.04
				6	491.52
				12	245.76
				24	122.88
38.4	–	5	384	3	983.04
				6	491.52
				12	245.76
				24	122.88

[a]  $x = A$  to  $E$ .

## Channel Frequency Divider

The device supports five independent channels A to E. Each channel has a frequency divider  $N_x$  ( $x = A$  to  $E$ ) that divides the VCO frequency to the output frequency. Each divider be individually set to a value in the range of  $\div 1$  to  $\div 160$ . For typical divider values (see [Table 9](#)). For the complete set of supported divider values (see [Table 28](#)).

Table 9. Integer Frequency Divider Settings

Channel Divider $N_x$ <sup>[a]</sup>	Output Clock Frequency (MHz)
	$f_{VCO} = 2949.12$ (MHz)
$\div 1$	2949.12
$\div 2$	1474.56
$\div 3$	983.04
$\div 4$	737.28
$\div 6$	491.52
$\div 8$	368.64
$\div 12$	245.76
$\div 16$	184.32
$\div 24$	122.88
$\div 30$	98.304
$\div 32$	92.16
$\div 36$	81.92
$\div 48$	61.44
$\div 60$	49.152
$\div 64$	46.08
$\div 72$	40.96
$\div 96$	30.72
$\div 120$	24.576
$\div 128$	23.04

[a]  $x = A$  to  $E$ .

## Redundant Inputs

The four inputs are compatible with LVDS and LVPECL signal formats, and also support single-ended LVCMOS signals. For applicable input interface circuits, see [Application Information](#).

### Monitoring and LOS of Input Signal

The four inputs of the device are individually monitored for activity. Inactivity is defined by a static input signal.

The clock input monitors compare the device input frequency ( $f_{CLK}$ ) to the frequency of the VCO divided by  $M_{V1}$  (regardless of the internal feedback path using or not using  $M_{V1}$ ). A clock input is declared invalid with the corresponding LOS (Loss-of-input signal) indicator bit set after three consecutive missing clock edges. For correct operation of the LOS detect circuit,  $M_{V1}$  must be powered on by setting  $PD\_MV1 = 0$ .

The  $M_{V1}$  divider must be set so that the LOS detect reference frequency matches the input frequency. For instance, if the input frequency is 245.76MHz,  $M_{V1}$  should be set to  $\div 12$ : The VCO frequency of 2949.12MHz divided by 12 equals the input frequency of 245.76MHz. For an input frequency of 122.88MHz, set  $M_{V1}$  to  $\div 24$ . Failure to set  $M_{V1}$  to match the input frequency will result in added latency to the LOS circuit (if,  $f_{VCO} \div M_{V1} < f_{CLK}$ ) or false LOS indication (if,  $f_{VCO} \div M_{V1} > f_{CLK}$ ). The minimum frequency that the circuit can monitor is:  $f_{VCO} / M_{V1(MAX)} = 5.77\text{MHz}$ . In applications with a lower input frequency than 5.77MHz, disable the monitor to trigger the status flags by setting  $BLOCK\_LOR = 1$ .

If differential input signals are applied, the input will also detect an LOS condition in case of a zero differential input voltage.

### Input Re-Validation

A clock input is declared valid and the corresponding LOS status bit is reset after the clock input signal returns for user-configurable number of consecutive input periods. This re-validation of the selected input clock is controlled by the CNTV setting (verification pulse counter).

## Clock Selection

The device supports four input selection modes: manual, short-term holdover, and two automatic switch modes. The modes are described in the following table.

Table 10. Clock Selection Settings

Mode	Description	Application
Manual nM/A[1:0] = 00	Input selection follows user configuration of SEL[1:0]. Selection is <i>never</i> changed by the internal state machine. A failing reference clock will cause an LOS event and the PLL will unlock if the failing clock is selected. Re-validation of the selected input clock will result in the PLL to re-lock on that input clock.	Startup and external selection control
Automatic nM/A[1:0] = 01	Input selection follows LOS status by user preset input switch priorities. A failing input clock will cause an LOS event for that clock input. If the selected clock has an LOS event, the device will immediately initiate a clock fail-over switch. The switch target is determined by pre-set input priorities.  No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will not enter the holdover state. The PLL is not locked. Re-validation of any input clock that is not the selected clock will result in the PLL to attempt to lock on that input clock.  For additional information see, <a href="#">Revertive Switching</a> .	Multiple inputs with qualified clock signals
Short-term Holdover nM/A[1:0] = 10	Input selection follows user-configuration of SEL[1:0]. Selection is never changed by the internal state machine. A failing reference clock will cause an LOS event. If the selected reference fails, the device will enter holdover <i>immediately</i> . Re-validation of the selected input clock is controlled by the CNTV setting. A successful re-validation will result in the PLL to re-lock on that input clock.  For additional information see, <a href="#">Short-Term Holdover</a> .	Single reference
Automatic with Holdover nM/A[1:0] = 11	Input selection follows LOS status by user preset input priorities. Each failing input clock will cause an LOS event for that clock input. If the <i>selected</i> clock detects an LOS event, the device will go into holdover and the hold-off down-counter (CNTH) starts. The device initiates a clock fail-over switch <i>after</i> expiration of the hold-off counter. The switch target is determined by the preset input priorities.  No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will remain in the holdover state. Re-validation of any input clock will result in the PLL to attempt to lock on that input clock.  For additional information see, <a href="#">Automatic with Holdover (nM/A[1:0] = 11)</a> , and <a href="#">Revertive Switching</a> .	Multiple inputs

## Holdover

In holdover state, the output frequency and phase is derived from an internal, digital value based on previous frequency and phase information. Holdover characteristics are defined in [Table 51](#).

## Input Priorities

Configurable settings encompass four selectable priorities with the range 0 (lowest priority) to 3 (highest priority). The user can change the input priorities at any time. In the automatic switch modes, input priority changes may cause immediate input selection changes.

## Hold-off Counter

A configurable down-counter applicable to the “Automatic with holdover” selection mode. The purpose of this counter is a deferred, user-configurable, input switch after an LOS event. The hold-off counter is triggered by a transition of ST\_REF upon detection of an LOS event. The counter expires when a zero-transition occurs; this triggers a new reference clock selection. The counter is clocked by the frequency-divided VCXO-PLL signal. The CNTR setting determines the hold-off counter frequency divider and the CNTH setting the start value of the hold-off counter. For instance, set CNTR to a value of  $\div 131072$  to achieve 937.5Hz (or a period of 1.066ms at  $f_{VCXO} = 122.88\text{MHz}$ ): the 8-bit CNTH counter is clocked by 937.5Hz and the user configurable hold-off period range is 0ms (CNTH = 0x00) to 272ms (CNTH = 0xFF). After the counter expires, it reloads automatically from the CNTH SPI register. After the LOS status bit (LS\_CLK\_*n*) for the corresponding input CLK\_*n* has been cleared by the user, the input is enabled for generating a new LOS event.

The CNTR counter is only clocked if the device is configured in the clock selection mode, *Automatic with holdover*, and the selected reference clock experiences an LOS event. Otherwise, the counter is automatically disabled (not clocked).

## Revertive Switching

Revertive switching is applicable only to the two automatic switch modes shown in [Table 10](#). When revertive switching is enabled, re-validation of any non-selected input clock(s) will cause a new input selection according to the user-preset input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the currently selected reference clock.

When revertive switching is disabled, re-validation of a non-selected input clock has no impact on the clock selection. Default setting is revertive switching disabled.

## Short-Term Holdover

If an LOS event is detected on the reference clock designated by the SEL[1:0] bits:

1. Holdover begins immediately.
2. ST\_REF, LS\_REF go low immediately.
3. No transitions will occur of the active REF clock; ST\_SEL[1:0] does not change.
4. The hold-off countdown is not active.

When the designated reference clock resumes and has met the programmed validation count of consecutive rising edges:

1. Holdover turns off.
2. ST\_SEL[1:0] does not change.
3. ST\_REF returns to 1.

LS\_REF can be cleared by an SPI write of 1 to that register.

## Automatic with Holdover (nM/A[1:0] = 11)

If an LOS event is detected on the active reference clock:

1. Holdover begins immediately.
2. Corresponding ST\_REF and LS\_REF go low immediately.
3. Hold-off countdown begins immediately.

During this time, all clocks continue to be monitored and their respective ST\_CLK, LS\_CLK flags are active. LOS events will be indicated on ST\_CLK, LS\_CLK when they occur.

If the active reference clock resumes and is validated during the hold-off countdown:

1. Its ST\_CLK status flag will return high and the LS\_CLK is available to be cleared by an SPI write of 1 to that register bit.
2. No transitions will occur of the active REF clock; ST\_SEL[1:0] does not change. LS\_REF can be cleared by an SPI write of 1 to that register.
3. Revertive bit has no effect during this time (whether 0 or 1).

When the hold-off countdown reaches zero.

If the active reference has resumed and has been validated during the countdown, it will maintain being the active reference clock:

1. ST\_SEL1:0 does not change.
2. ST\_REF returns to 1.
3. LS\_REF can be cleared by an SPI write of 1 to that register.
4. Holdover turns off and the VCXO-PLL attempts to lock to the active reference clock

If the active reference has not resumed, but another (sorted by next priority) clock input CLK\_n is validated, then:

1. ST\_SEL1:0 changes to the new active reference.
2. ST\_REF returns to 1.
3. LS\_REF can be cleared by an SPI write of 1 to that register.
4. Holdover turns off.

If there is no validated CLK:

1. ST\_SEL1:0 does not change.
2. ST\_REF remains low.
3. LS\_REF cannot be cleared by an SPI write of 1 to that register.
4. Holdover remains active.

Revertive capability returns if REVS = 1.

## VCXO-PLL Lock Detect (LOLV)

The VCXO-PLL lock detect circuit uses the signal phase difference at the phase detector as loss-of-lock criteria. Loss-of-lock is reported if the actual phase difference is larger than a configurable phase window set by the  $\Phi_{MV0}$  and  $\Phi_{PV}$  configuration bits. Configuration of the width window allows for an application-specific loss-of-lock reporting. A loss-of-lock state is reported through the nST\_LOLV and nLS\_LOLV status bit (see Table 22).

### Loss-of-Lock Window Description

The selected clock input signal is the reference signal (CLK) for lock detection. The rising edge of CLK defines the reference point  $t_0$ .  $\Phi_{PV}$  configures the start of the lock window  $t_B$  (which occurs before  $t_0$ ) and  $\Phi_{MV0}$  configures the end of the window  $t_E$  (which occurs after  $t_0$ ). The width of the lock window is defined by  $t_E - t_B$ . The VCXO-PLL declares lock when the rising edge of the feedback signal (FB) is within this window, otherwise the PLL reports loss-of-lock.

Figure 3. Lock Detect Window

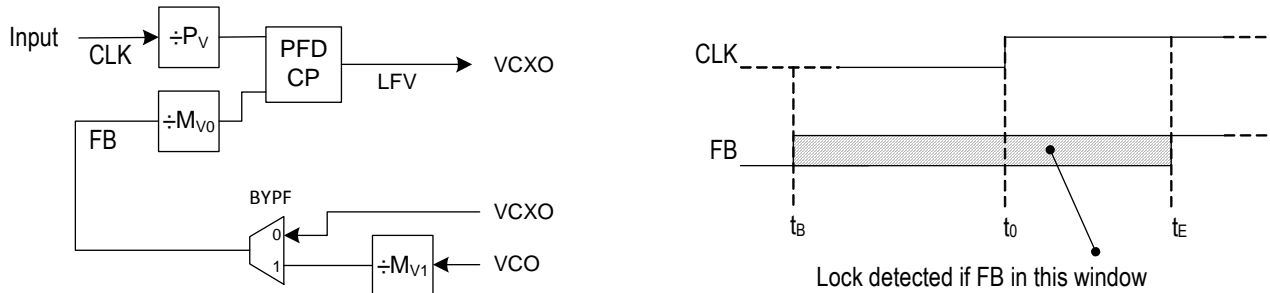


Table 11.  $t_B$  and  $t_E$  Calculation

Operation	Jitter Attenuation, Dual-PLL with deterministic Input-to-Output Delay (BYPV = 0, BYPF = 1)	Jitter Attenuation, Dual-PLL (BYPV = 0, BYPF = 0)
$t_B$	$t_B = -\frac{2^{\Phi_{PV}} - 1}{f_{CLK}}$	
$t_E$	$t_E = \frac{(2^{\Phi_{MV0}} - 1) \times M_{V1}}{f_{VCO}}$	$t_E = \frac{2^{\Phi_{MV0}} - 1}{f_{VCXO}}$

Figure 3 shows that  $\Phi_{PV}$  configures the begin and  $\Phi_{MV0}$  the end of the window in integer multiples of PLL input and feedback periods. Both  $\Phi_{PV}$  and  $\Phi_{MV0}$  use three configuration bits with valid settings from 010 to 111 (2 to 7, decimal). This range allows configuring both  $t_B$  and  $t_E$  from 3 to 127 periods of the input signal ( $T_{IN}$ ) and the feedback signal ( $T_{FB}$ ), respectively, is implied.



### Loss-of-Lock Window Configuration Example

With given  $P_V$ ,  $M_{V0}$ , and  $M_{V1}$  divider values, select the corresponding  $\Phi_{PV}$  and  $\Phi_{MV0}$  settings from Table 12 and apply the  $\Phi_{PV}$  and  $\Phi_{MV0}$  values to the  $\Phi_{PV}[1:0]$  and  $\Phi_{MV0}[1:0]$  registers. Table 12 shows the lock window calculation formulas. For instance, if an input frequency of 245.76MHz and a  $P_V$  divider of 128 is desired, set  $\Phi_{PV}[1:0]$  to a binary value of 100 (decimal 4). This results in  $t_B = -61.035\text{ns}$  (15 periods of 4.069ns). With a VCXO-PLL (BYPF = 0) and a VCXO frequency of 122.88MHz and  $M_{V0} = 64$ , select 011 (decimal 3) resulting in  $t_E = 56.96\text{ns}$  (7 periods of 8.138ns) and an overall lock detect window of  $t_E - t_B = 56.96\text{ns} + 61.035\text{ns} = 118.001\text{ns}$ . The user may select a smaller lock detect window. For instance, a  $P_V$  divider of 128 allows to set  $\Phi_{PV}[1:0]$  to 010, 011 or 100 (decimal 2 to 4). Correspondingly, a  $M_{V0}$  divider of 64 allows  $\Phi_{MV0}[1:0]$  settings from 010 to 011 (decimal 2 to 3). With smaller settings, the lock detect window size is reduced exponentially.

$\Phi_{PV}[1:0] = 000$  will set  $t_B$  to  $0.5 \times T_{REF}$ , and  $\Phi_{PV}[1:0] = 001$  will set  $t_B$  to  $1.5 \times T_{REF}$ .

$\Phi_{MV0}[1:0] = 000$  will set  $t_E$  to  $0.5 \times T_{REF}$ , and  $\Phi_{MV0}[1:0] = 001$  will set  $t_E$  to  $1.5 \times T_{REF}$ .

Table 12. Recommended Lock Detector Phase Window Settings

$P_V$ Divider Value	$\Phi_{PV}[1:0]$ Setting	$M_{V0}$ Divider Value	$\Phi_{MV0}[1:0]$ Setting
1–31	N/A	1–31	N/A
32–63	010	32–63	010
64–127	$\leq 011$	64–127	$\leq 011$
128–255	$\leq 100$	128–255	$\leq 100$
256–511	$\leq 101$	256–511	$\leq 101$
512–1023	$\leq 110$	512–1023	$\leq 110$
1024 and higher	$\leq 111$	1024 and higher	$\leq 111$

### FemtoClock NG Loss-of-Lock (LOLF)

FemtoClock NG-PLL loss-of-lock is signaled through the  $nST\_LOLF$  (momentary) and  $nLS\_LOLF$  (sticky, resettable) status bits and can be reported as hardware signal on the LOCK output as well as an interrupt signal on the  $nINT$  output.

## Channel, Output, and JESD204B Logic

### Channel

Each of the four channels, A to D, consists of one to three clock outputs, and one associated to three SYSREF outputs. Each SYSREF output in a channel can be individually configured to generate JESD204B (SYSREF) signals or copy the clock signal of that channel. The fifth channel (E) consists of two clock outputs without SYSREF support in that channel.

If JESD204B/SYSREF operation is assigned to a QREF output, the channel logic controls the outputs: outputs automatically turn on and off in a SYSREF sequence. QREF outputs configured to clock operation can have individually configured output states.

Table 13. Channel Configuration<sup>[a]</sup>

MUX_ <i>r</i>	0	1
Description	Clock Configuration	JESD204B
QCLK_ <i>y</i>	Clock signal	Clock signal
QREF_ <i>r</i>		SYSREF/JESD204B
Frequency Divider	QCLK_ <i>y</i> and QREF_ <i>r</i> : $N_x$	QCLK_ <i>y</i> : $N_x$ QREF_ <i>r</i> : $N_S$ (Global to all QREF_ <i>r</i> )
Phase Delay	QCLK_ <i>y</i> and QREF_ <i>r</i> : $\Phi_{CLK\_x}$ $\Phi_{REF\_r}$ settings do not apply	QCLK_ <i>y</i> : $\Phi_{CLK\_x}$ QREF_ <i>r</i> : $\Phi_{REF\_r}$
Power-down	Per output	Per channel
Output Enable	Per output	Per output

[a] *x* = A to E

*y* = A0, A1, A2, B0, B1, C0, C1, D, E0, E1;

*r* = A0, A1, A2, B0, B1, C0, C1, D.

## Differential Outputs

Table 14. Output Features

Output	Style	Amplitude <sup>[a]</sup>	Disable	Power-down	Termination
QCLK_y, QREF_r (Clock)	LVPECL	250-1000mV 4 steps	Yes	Yes	50Ω to V <sub>T</sub>
	LVDS				100Ω differential <sup>[b]</sup>
QREF_r (SYSREF)	LVDS	500mV A[1:0] = 01	Controlled by SYSREF <sup>[c]</sup>		100Ω differential <sup>[b]</sup>
QOSC	LVPECL	250–750mV 3 steps	Yes	Yes	50Ω to V <sub>T</sub>
	LVDS				100Ω differential <sup>[b]</sup>

[a] Amplitudes are measured single-endedly. Differential amplitudes supported are 500mV, 1000mV, 1500mV and 2000mV.

[b] AC coupling and DC coupling supported.

[c] State of SYSREF outputs is controlled by an internal SYSREF state machine.

Table 15. Individual Clock Output Settings<sup>[a]</sup>

PD <sup>[b]</sup>	STYLE	EN <sup>[c]</sup>	A[1:0] <sup>[d]</sup>	Output Power	Termination	State	Amplitude (mV)
1	X	X	X	Off	100Ω differential or no termination	Off	X
0	0	0	XX	On	100Ω differential (LVDS)	Disable (logic low)	X
		1	00			Enable	250
			01				500
			10				750
			11				1000
	1	0	XX		50Ω to V <sub>T</sub> (LVPECL)	Enable	X
		1	00		50Ω to V <sub>T</sub> = V <sub>DD_V</sub> - 1.50V (LVPECL)		250
			01		50Ω to V <sub>T</sub> = V <sub>DD_V</sub> - 1.75V (LVPECL)		500
			10		50Ω to V <sub>T</sub> = V <sub>DD_V</sub> - 2.00V (LVPECL)		750
			11		50Ω to V <sub>T</sub> = V <sub>DD_V</sub> - 2.25V (LVPECL)		1000
					Enable		

[a] Applicable to clock outputs: QCLK\_y and QREF\_r outputs in clock mode (MUX\_r = 0).

[b] Power-down modes are available for the individual channels A-E and the outputs QCLK\_y (A0 to E1).

[c] Output enable is supported on each individual QCLK\_y and QREF\_r output.

[d] Output amplitude control is supported on each individual QCLK\_y and QREF\_r output.

Table 16. Individual SYSREF Output Settings<sup>[a]</sup>

PD	STYLE	EN	nBIAS	A[1:0]	Output Power	Termination	State	Amplitude (mV)
1	X	X	X	X	Off	100Ω differential or no termination	Off	X
0	0	0	0	01	On <sup>[b]</sup>	100Ω differential (LVDS)	Disable (logic low)	X
		1					Enable	500
		X	1	XX			Line bias <sup>[c]</sup>	XX
	1	0	0	01		50Ω to V <sub>T</sub> = V <sub>DD_V</sub> – 1.50V (LVPECL)	Disable (logic low)	X
		1					Enable	500
		X	1	XX				

[a] Applicable QREF\_r outputs when configured as SYSREF output (MUX\_r = 1).

[b] Output amplitude should be set to a 500mV swing (A[1:0] to 01) by SPI. SYSREF output states are controlled by an internal state machine. An internal SYSREF event will automatically turn SYSREF outputs on. After the event, outputs are automatically turned off. Setting nBIAS = 1 will bias powered-off outputs to the LVDS midpoint voltage.

[c] Output (both Q, and nQ) bias the line to the differential signal cross-point voltage. Available if output is AC-coupled and set to LVDS style.

Table 17. QOSC (VCXO-PLL Output) Settings

nPD	STYLE	A[1:0]	Output Power	Termination	Amplitude (mV)
0	X	X	Off	100Ω differential (LVDS) or no termination	X
1	0	00	On	100Ω differential (LVDS)	250
		01			500
		10			750
		11			500
	1	00		50Ω to $V_T = V_{DD\_V} - 1.50V$ (LVPECL)	250
		01		50Ω to $V_T = V_{DD\_V} - 1.75V$ (LVPECL)	500
		10			
		11		50Ω to $V_T = V_{DD\_V} - 2.00V$ (LVPECL)	750

Table 18. QREF\_r Setting for JESD204B Applications

BIAS_TYPE	nBIAS_r	QREF_r Outputs (LVDS, 500mV Amplitude)			Application
		Initial	During SYSREF Event	SYSREF Completed	
0	0	Static low (QREF = L, nQREF_r = H)	Start switching for the number of configured SYSREF pulses	Released to static low (QREF = L, nQREF_r = H)	QREF_r DC coupled
	1	Static low (QREF = L, nQREF_r = H)			
1	0	Static LVDS crosspoint level (QREF = nQREF_r = VOS)	Start switching for the number of configured SYSREF pulses	Released to static LVDS crosspoint level (QREF = nQREF_r = VOS)	QREF_r AC coupled
	1	Static LVDS crosspoint level (QREF = nQREF_r = VOS)			

## Output Phase-Delay

Output phase delay is independently supported on both clock and SYSREF outputs.

Table 19. Delay Circuit Settings<sup>[a]</sup>

Delay Circuit	Unit	Steps	Range (ns)	Alignment <sup>[b]</sup>
Clock $\Phi_{CLK\_x}$	$\frac{1}{f_{VCO}} = 339\text{ps}$	256	0–86.466	Incident rising clock edges are aligned, independent of the divider $N_x$ across channels
SYSREF $\Phi_{REF\_r}$	Coarse delay: $\frac{1}{2f_{VCO}} = 169\text{ps}$	8	0–1.187	SYSREF rising edge is aligned to the incident rising clock edge across channels
	Fine delay: 0ps, 25ps, 50ps, 75ps, 85ps, 110ps, 135ps, 160ps	8	0–0.160	
SYSREF (Global) $\Phi_{REF\_S}$	$\frac{1}{f_{VCO}} = 339\text{ps}$	256	0–86.466	Global alignment of SYSREF signals

[a] Supports  $\geq 12$  SYSREF rising edge stops within a device clock period of 1017ps (983.04MHz), 2.034ns (491.52MHz), 4.096ns (245.76MHz), and 8.137ns (122.88MHz), respectively. Clock output inversion supported by setting phase delay to a 180° setting.

[b] Default configuration (all delay settings = 0).  $\Phi_{REF\_r}$  coarse delay values are exact, fine delay value vary over PVT by  $\pm 20\%$ .

## Configuration for JESD204B Operation

### Synchronizing SYSREF and Clock Output Dividers

The SYNC[6:0] divider controls the release of SYSREF pulses at coincident QCLK\_y clock edges. For SYSREF operation, set the SYNC divider value to the least common multiple of the clock divider values  $N_x$  ( $x = A$  to  $E$ ). For instance, if  $N_A = N_B = \div 2$ ,  $N_C = N_D = \div 3$ ,  $N_E = \div 4$ , set the SYNC divider to  $\div 12$ .

### SYSREF Generation

A SYSREF event is the generation of one or more consecutive pulses on the QREF outputs. An event can be triggered by SPI commands or by a signal-transition on the EXT\_SYS input. The number of SYSREF pulses generated is programmable from 1 to 255. The SYSREF signal can also be programmed to be continuous. The SYSREF pulse rate is configurable to the frequencies shown in Table 20. SYSREF output pulses are aligned to coincident rising clock edges of the clock outputs QCLK\_y. Device settings for phase alignment between QCLK\_y and QREF\_r outputs is detailed in the section, [QCLK to QREF Phase Alignment](#). The following SYSREF pulse generation modes are available and configurable by SPI:

- Counted pulse mode: 1 to 255 pulses are generated by the device. SYSREF activity stops automatically after the transmission of the selected number of pulses and the QREF output powers down.
- Continuous mode. The SYSREF signal is a clock signal.

The generation of SYSREF pulses is configured by SPI commands and is available after the initial setup of output clock divider and QREF phase delay stages. A SYSREF event will automatically turn on the SYSREF outputs. After the event, SYSREF outputs are automatically turned off (power-down). SYSREF outputs with the nBIAS bit set high will bias the outputs at the LVDS crosspoint voltage level (requires BIAS\_TYPE = 1).

Table 20. SYSREF Generation<sup>[a]</sup>

SRO	N <sub>S</sub>	SYSREF Operation (f <sub>SYSREF</sub> )	
		f <sub>VCO</sub> = 2949.12MHz	
0	Counted pulse mode (Use the SRPC register to configure the number of generated SYSREF pulses)		
	÷64	46.08	
	÷96	30.72	
	÷128	23.04	
	÷192	15.36	
	÷256	11.52	
	÷384	7.68	
	÷512	5.76	
	÷768	3.84	
	÷1024	2.88	
	÷2048	1.44	
	÷4096	0.72	
	÷5120	0.576	
1	Continuous pulse mode		
	÷64	46.08	
	÷96	30.72	
	÷128	23.04	
	÷192	15.36	
	÷256	11.52	
	÷384	7.68	
	÷512	5.76	
	÷768	3.84	
	÷1024	2.88	
	÷2048	1.44	
	÷4096	0.72	
	÷5120	0.576	

[a] SRO and SRPC are global settings.

## Internal SYSREF Generation

SYSREF generation is set to internal (SRG = 0). The SRO setting defines if SYSREF pulses are counted or continuous and the NS[6:0] divider sets the frequency. In counted pulse mode, the SRPC register contains the number of pulses to generate. Any number from 1 to 255 pulses may be generated. SYSREF pulses are generated upon completion of the SPI command RS (SYSREF release). Setting RS activates the SYSREF outputs, loads the number of pulses from the SRPC register and starts the generation of SYSREF pulses synchronized to the incident edge of the clock signals. After the programmed number of pulses are generated, SYSREF outputs will go into logic low state or bias the output voltage to the static LVDS crosspoint level (see [Table 18](#) for settings and details). In continuous mode, SYSREF is a clock signal and the content of the SRPC signal is ignored.

## External SYSREF Generation

SYSREF generation is set to external (SRG = 1): SYSREF pulses are generated in response to the detection of a rising edge at the EXT\_SYS input. The EXT\_SYS input rising edge releases SYSREF pulses. Both SRO and SRPC register settings apply as in internal SYSREF generation mode for generating single shot and repetitive SYSREF output signals. Set RS = 1 to prepare for SYSREF generation; the generation of SYSREF pulses is triggered by a rising edge at EXT\_SYS pin.

## QCLK to QREF (SYSREF) Phase Alignment

[Figure 4](#) and [Table 21](#) show how to achieve output phase alignment between the QCLK<sub>y</sub> clock and the QREF<sub>r</sub> SYSREF outputs. Output phase will be different for different N<sub>x</sub> dividers. For a given example in [Figure 4](#), the closest (smallest phase error) output alignment is achieved by setting the clock phase delay register  $\Phi_{QCLK\_y}$  to 0x00, the coarse SYSREF output phase delay register  $\Phi_{REF\_r}$  to 0x01, fine SYSREF delay to  $\Phi_{REF\_F\_r} = 1$  and the global  $\Phi_{REF\_S}$  delay register to 0x29. With a SYSREF phase delay setting of  $\Phi_{REF\_r} = 0x01$ ,  $\Phi_{REF\_F\_r} = 0$ , the QREF<sub>r</sub> output phase is in advance of the QCLK<sub>y</sub> phase, which is applicable in JESD204B application. Phase delay settings and propagation delays are dependent on the clock and SYSREF frequency dividers, but independent of the SYSREF generation mode (SRG = 0 or SRG = 1). Recommended phase delay setting for several device configurations are shown in [Table 21](#).

Figure 4. QCLK to QREF Phase Alignment

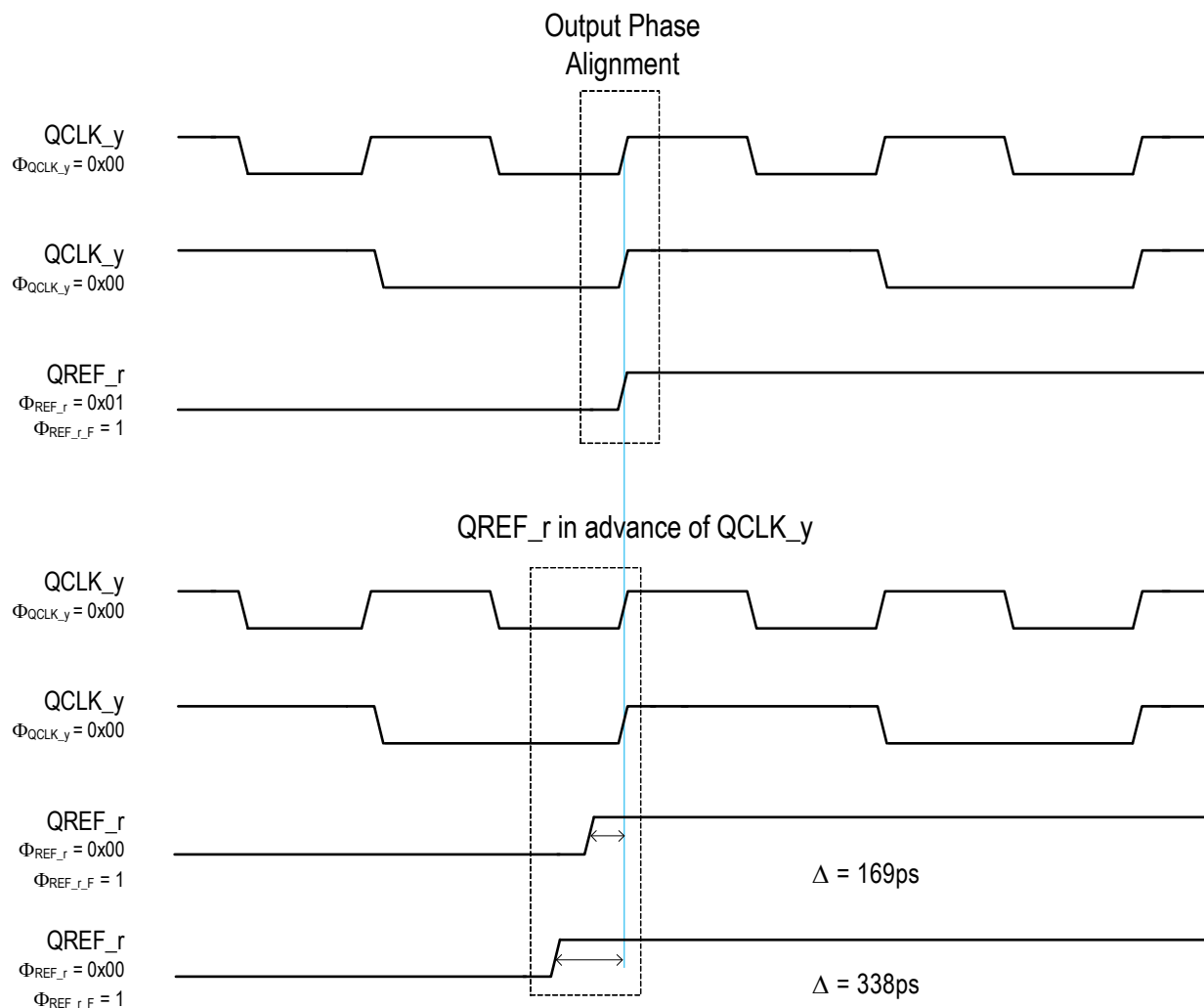


Table 21. Recommended Delay Settings for Closest Clock-SYSREF Output Phase Alignment<sup>[a]</sup>

Divider Configuration	$\Phi_{CLK\_y}$	$\Phi_{REF\_r}$	$\Phi_{REF\_r\_F}$	$\Phi_{REF\_S}$
$N_{A-E} = \div 3$ $N_S = \div 384$	0x00	0x01	1	0x29
$N_{A-E} = \div 3, \div 6, \div 12$ $N_S = \div 384$	0x00	0x01	1	0x29
$N_{A-E} = \div 8$ $N_S = \div 384$	0x00	0x03	1	0x00

[a] QCLK and QREF outputs are aligned on the incident edge.



## Deterministic Phase Relationship and Phase Alignment

Input to output delay is deterministic when the device is configured as dual PLL with the  $BYPV = 0$ ,  $BYPF = 1$  (PLL feedback path through  $M_{V0} \times M_{V1}$ ). Refer to the application note [AN-952: 8V19N480/490 Design Guide for JESD204B Output Phase Alignment and Termination](#) for additional information on phase alignment, termination and coupling techniques.

### Status Conditions & Interrupts

The device has an interrupt output to signal changes in status conditions. The devices have several conditions that can indicate faults and status changes in the operation of the device. These are shown in [Table 22](#), and can be monitored directly in the status registers. Status bits (named: *ST\_condition*) are read-only and reflect the momentary device status at the time of read-access. Several status bits are also copied into latched bit positions (named: *LS\_condition*). The latched version is controlled by the corresponding fault and status conditions and remains set ("sticky") until reset by the user by writing "1" to the status register bit. The reset of the status condition only has an effect if the corresponding fault condition is removed, otherwise, the status bit will set again. Setting a status bit on several latched registers can be programmed to generate an interrupt signal (nINT) via settings in the Interrupt Enable bits (named: *IE\_condition*). A setting of "0" in any of these bits will mask the corresponding latched status bits from affecting the interrupt status pin. Setting all IE bits to 0 has the effect of disabling interrupts from the device. Interrupts are cleared by resetting the appropriate bit(s) in the latched register after the underlying fault condition has been resolved. When all valid interrupt sources have been cleared in this manner, this will release the nINT output until the next unmasked fault.

Table 22. Status Bit Functions

Status Bit		Function			Interrupt Enable Bit
Momentary	Latched	Description	Status if Bit is:		
			1	0	
ST_CLK_0	LS_CLK_0	CLK 0 input status	Active	LOS	IE_CLK_0
ST_CLK_1	LS_CLK_1	CLK 1 input status	Active	LOS	IE_CLK_1
ST_CLK_2	LS_CLK_2	CLK 2 input status	Active	LOS	IE_CLK_2
ST_CLK_3	LS_CLK_3	CLK 3 input status	Active	LOS	IE_CLK_3
nST_LOLV	nLS_LOLV	VCXO-PLL Loss-of-lock	Locked	Loss-of-lock	IE_LOLV
nST_LOLF <sup>[a]</sup>	nLS_LOLF	FemtoClock NG-PLL Loss-of-lock	Locked	Loss-of-lock	IE_LOLF
nST_HOLD	nLS_HOLD	Holdover	Not in holdover	Device in holdover	IE_HOLD
ST_VCOF	—	FemtoClock NG VCO calibration	Not completed	Completed	—
ST_SEL[1:0]	—	Clock input selection	00 = CLK_0 01 = CLK_1 10 = CLK_2 11 = CLK_3		—
ST_REF	LS_REF	PLL reference status	Valid reference	Reference lost <sup>[b]</sup>	IE_REF

[a] If the VCXO-PLL is bypassed by setting  $BYPV = 1$ , VCXO-PLL lock status is blocked from affecting the LOCK pin.

[b] Manual and short-term holdover mode: 0 indicates if the reference selected by SEL[1:0] is lost, 1 if not lost.  
 Automatic with holdover mode: 0 indicates the reference is lost and while still in holdover, or no valid CLK[3:0].  
 Automatic mode: 0 indicates no valid CLK[3:0].

Table 23. LOCK Output Function

Status Bit (PLL)		Status Reported on LOCK Output
nST_LOLV (VCXO-PLL)	nST_LOLF (FemtoClock NG)	
Locked <sup>[a]</sup>	Locked	1
	Not locked	0
Not locked	Locked	0
	Not locked	0

[a] If the VCXO-PLL is bypassed by setting BYPV = 1, VCXO-PLL lock status is blocked from affecting the LOCK. pin.

## Device Startup, Reset and Synchronization

At startup, an internal POR (power-on reset) resets the device and sets all register bits to their default value. The device forces the VCXO control voltage at the LFV pin to half of the power supply voltage to center the VCXO-frequency. In the default configuration the QCLK\_y and QREF\_r outputs are disabled at startup.

### Recommended Configuration Sequence:

- (Optional) set the value of the CPOL register bit to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
- Configure all PLL settings, output divider and delay circuits as well as other device configurations:
  - BYPF and BYPV for the desired PLL operation mode and configure the PLL dividers  $P_V$ ,  $M_{V0}$ ,  $M_{V1}$ ,  $M_F$  and  $P_F$  as required to achieve PLL lock (see [Table 2](#) for details).
  - VCXO-PLL lock detect window by configuring the phase settings  $\Phi_{M_{V0}}$  and  $\Phi_{P_V}$ .
  - Charge pump currents for both PLLs (CPV[4:0] and CPF[4:0]) and POLV for the desired VCXO polarity.
  - (optional) OSVEN and OFFSET[4:0] for the VCXO-PLL static phase offset.
  - Channel dividers (see [Table 8](#)).
  - MUX\_r for the desired operation of the QREF\_r outputs.
  - QCLK\_y, QREF\_r and QOSC output features such as desired output power-down state, style and amplitude.
  - Desired input selection and monitoring modes: this involves nM/A[1:0] and SEL[1:0] for input selection. In any of the automatic modes, configure PRIO[1:0]\_n, and REVS. Configure the CNTH[7:0], CNTR[1:0] counters for the desired holdover characteristics and DIV4\_VAL, CNTV[1:0] for input revalidation if applicable to the operation mode.
  - Individual  $\Phi_{CLK_X}$  and  $\Phi_{REF_r}$  registers and the global delay  $\Phi_{REF_S}$  register for the desired phase delay between clock and SYSREF outputs; (see [QCLK to QREF \(SYSREF\) Phase Alignment](#)).
  - Interrupt enable configuration bits IE\_status\_condition, as desired for fault reporting on the nINT output.
- For SYSREF operation:
  - Configure the  $N_S$  and SYNC divider as described in, [Synchronizing SYSREF and Clock Output Dividers](#).
  - Configure the SYSREF registers SRG, SRO and SRPC[7:0] according to the desired SYSREF operation.
- Set the initialization bit INIT\_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT\_CLK bit will self-clear.
- Set both the RELOCK bit and PB\_CAL bit. This step should not be combined with the previous step (setting INIT\_CLK) in a multi SPI-byte register access. Both bits will self-clear.
- Clear the FVCV bit to release the VCXO control voltage and VCXO-PLL will attempt to lock to the input clock signal starting from its center frequency.
- Clear the status flags.

8. At this point, the basic configuration of the registers 0x00 to 0x73 should be completed and the SPI transfer ended (set nCS to high level).
9. In a separate SPI write access, enable the outputs as desired by accessing the output-enable registers 0x74 and 0x76.
10. For SYSREF operation, see Step 9, [SYSREF Frequency Divider, Delay and Starting/Re-Starting SYSREF Pulse Sequences](#).

Reserved registers and registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

## Changing Frequency Dividers and Phase Delay Values

### **Clock Frequency Divider and Delay**

The following procedure has to be applied for a change of a clock divider and phase delay value  $N_{A-E}$ , and  $\Phi_{CLKA-E}$ :

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. (Optional) disable the outputs whose frequency divider or delay value is changed.
3. Configure the  $N_{A-E}$  dividers and the delay circuits  $\Phi_{CLKA-E}$  to the desired new values.
4. (Optional) configure the SYNC divider if required for synchronization between clock and SYSREF signals.
5. Set the initialization bit INIT\_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT\_CLK bit will self-clear. During this initialization step, all QCLK\_y and QREF\_r outputs are reset to the logic low state.
6. Set the RELOCK bit. This step should not be combined with the setting INIT\_CLK in a multi SPI-byte register access. Bit will self-clear.
7. (Optional) enable the outputs whose frequency divider was changed.

### **SYSREF Frequency Divider, Delay and Starting/Re-Starting SYSREF Pulse Sequences**

The following procedure has to be applied for a change of a SYSREF divider and phase delay value  $N_S$  and  $\Phi_{REF_S}$ :

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. (Optional) disable the outputs whose frequency divider or delay value is changed.
3. Configure any  $N_S$  divider and any delay circuits  $\Phi_{REF_S}$  to their desired new values.
4. Configure the SYNC divider if required for synchronization between clock and SYSREF signals.
5. Set the initialization bit INIT\_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT\_CLK bit will self-clear. During this initialization step, all QCLK\_y and QREF\_r outputs are reset to the logic low state.
6. Set the RELOCK bit. This step should not be combined with the setting INIT\_CLK in a multi SPI-byte register access. Bit will self-clear.
7. Set the SRO bit to counted pulse mode, or to continue pulse mode, as desired.
8. (Optional) enable the outputs whose frequency divider was changed.
9. For SYSREF operation, set the RS bit to start (or re-start) generating the configured number of SYSREF pulses.
  - a. In internal SYSREF generation mode (SRG = 0) the SYSREF pulses are generated as a result of setting the RS bit. Set RS for each repeated SYSREF generation.
  - b. In external SYSREF mode the SYSREF pulses are generated at the next rising edge of the EXT\_SYS input. Set RS before each rising edge at the EXT\_SYS input.

## SPI Interface

The device has a 3-wire serial control port capable of responding as a slave in an SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), SDAT (serial data input and output), and nCS (chip select) pins. A data transfer consists any integer multiple of 8 bits and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8 bit each.

If nCS is at logic high, the SDAT data I/O is in high-impedance state and the SPI interface of the device is disabled.

In a write operation, data on SDAT will be clocked in on the rising edge of SCLK. In a read operation, data on SDAT will be clocked out on the falling or rising edge of SCLK depending on the CPOL setting (CPOL = 0: output data changes on the falling edge, CPOL = 1: output data changes on the rising edge).

Starting a data transfer requires nCS to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface with SDAT in data input mode. The master must initiate the first 8-bit transfer. The first bit presented to the slave is the direction bit R/nW (1 = Read, 0 = Write) and the following seven bits are the address bits A[0:6] pointing to an internal register in the address space 0 to 127. Data is presented with the LSB (least significant bit) first.

**Read operation from an internal register:** A read operation starts with an 8 bit transfer from the master to the slave: SDAT is clocked on the *rising* edge of SCLK. The first bit is the direction bit R/nW which must be to “1” to indicate a read transfer, followed by seven address bits A[0:6]. After the first 8 bits are clocked into SDAT, the SDAT I/O changes to output: The register content addressed by A[0:6] is loaded into the shift register and the next eight SCLK *falling* (CPOL = 1) clock cycles will then present the loaded register data on the SDAT output and transfer these to the master. Transfers must be completed by de-asserting nCS after any multiple 8 of SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. SPI byte (8 bit) and back-to-back read transfers of multiple registers are supported with an address auto-increment. During multiple transfers, nCS must stay at logic low level and SDAT will present multiple registers (A), (A + 1), (A + 2), etc. with each eight SCLK cycles. During SPI Read operations, the user may continue to hold nCS low and provide further bytes of data for up to a total of 127 bytes in a single block read.

**Write operation to a device register:** During a write transfer, an SPI master transfers one or more bytes of data into the internal registers of the device. A write transfer starts by asserting nCS to low logic level. The first bit presented by the master must set the direction bit R/nW to 0 (Write) and the seven address bits A[0:6] must contain the 7-bit register address. Bits D0 to D7 contain 8 bit of payload data, which is written into the register addressed by A[0:6] at the end of a 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported by holding nCS asserted at logic low level during write transfers. The 7 bit register address will auto-increment. Transfers must be completed by de-asserting nCS after any multiple eight of SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined.

**End of transfer:** After nCS is de-asserted to logic “1”, the SPI bus is available to transfers to other slaves on the SPI bus. The READ (Figure 5) and WRITE (Figure 6) diagrams display the transfer of two bytes of data from and into registers.

**Registers 0x78 to 0xFF.** Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

Figure 5. Logic Diagram: READ Data from Registers for CPOL = 0 and CPOL = 1

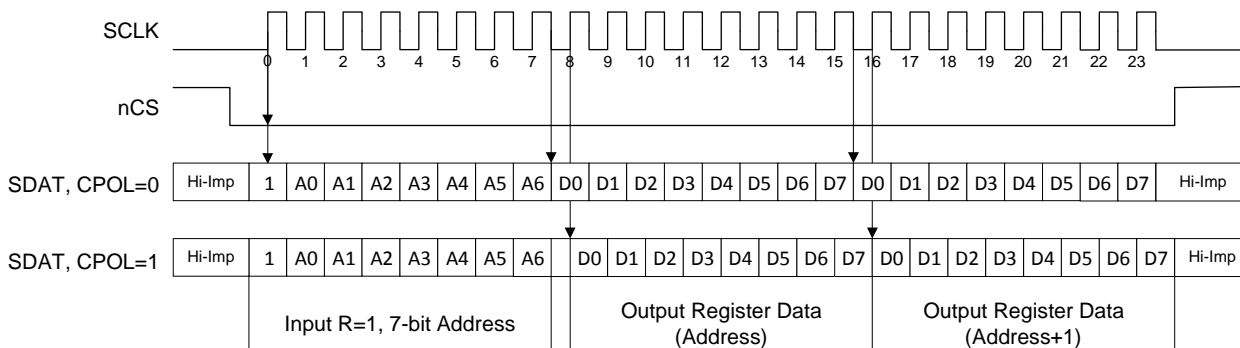


Figure 6. Logic Diagram: WRITE Data into Registers

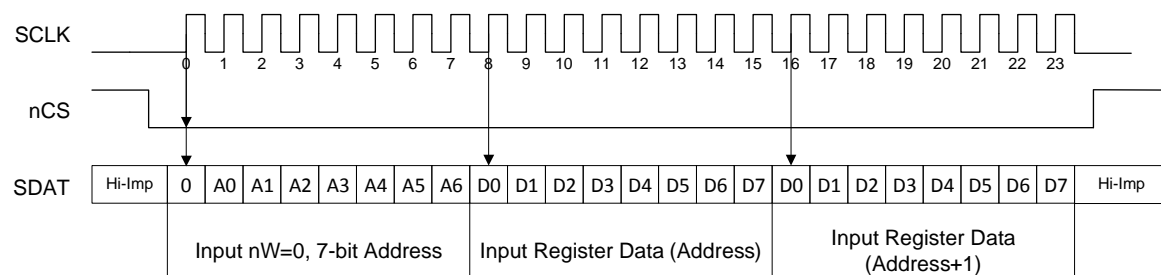


Table 24. SPI Read / Write Cycle Timing Parameters

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
$f_{SCLK}$	SCLK Frequency			20	MHz
$t_{S1}$	Setup Time, nCS (falling) to SCLK (rising)		5		ns
$t_{S2}$	Setup Time, SDAT (input) to SCLK (rising)		5		ns
$t_{S3}$	Setup Time, nCS (rising) to SCLK (rising)		5		ns
$t_{H1}$	Hold Time, SCLK (rising) to SDAT (input)		5		ns
$t_{H2}$	Hold Time, SCLK (falling) to nCS (rising)		5		ns
$t_{PD1F}$	Propagation Delay, SCLK (falling) to SDAT	CPOL = 0		12	ns
$t_{PD1R}$	Propagation Delay, SCLK (rising) to SDAT	CPOL = 1		12	ns
$t_{PD2}$	Propagation Delay, nCS to SDAT (disable)			12	ns

Figure 7. SPI Timing Diagram

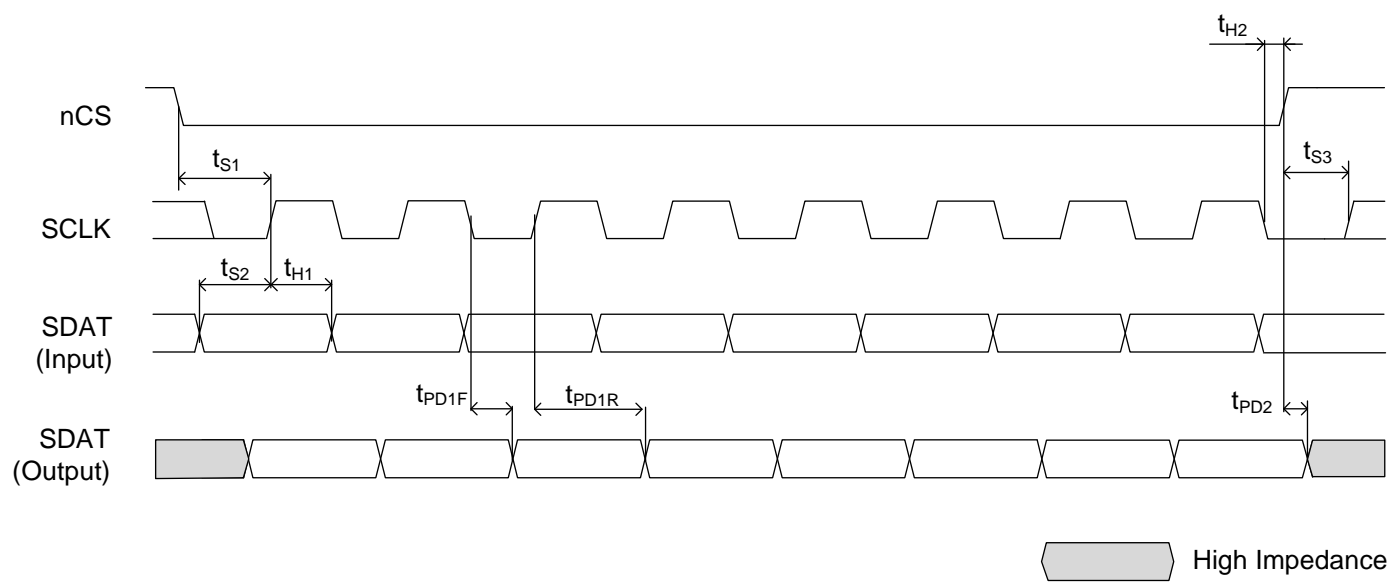


Table 25. Serial Interface Logic Voltage

SELSV	SPI Interface (SCLK, SDAT, nCS, EXT_SYS) Logic Voltage
0 (default)	1.8V
1	3.3V

# Register Descriptions

## List of Registers

Table 26. Configuration Registers

Register Address	Register Description
0x00–0x01	PLL Frequency Divider: $\Phi_{MV}$ , $M_{V0}$
0x02–0x03	PLL Frequency Divider: $M_{V1}$ , BYPF
0x04–0x05	VCXO-PLL Control: Frequency Divider, $\Phi_{PV}$ , $P_V$
0x06–0x07	Reserved
0x08–0x09	PLL Frequency Divider $M_F$
0x0A	VCXO-PLL Control BYPV
0x0B	Reserved
0x0C	PLL Frequency Divider: $P_F$ , FDF
0x0D–0x0F	Reserved
0x10–0x12	VCXO-PLL Control, output state QOSC
0x13	Reserved
0x14	Input Selection Mode Priority
0x15	Input Selection Mode Switching
0x16	Input Selection Mode CNTH
0x17	Input Selection Mode: CNTR, CNTV
0x18	SYSREF Control: divider, PD
0x19	SYSREF Control SYNC
0x1A	SYSREF Control SRPC
0x1B	SYSREF Control $\Phi_{REF\_S}$
0x1C	SYSREF Control SRG, SRO
0x1D–0x1F	PLL Control
0x20–0x22	Channel A
0x23	Reserved
0x24	Output State QCLK_A0
0x25	Output State QCLK_A1
0x26	Output State QCLK_A2
0x27	Reserved
0x28	QREF_A0: delay, MUX
0x29	QREF_A1: delay, MUX
0x2A	QREF_A2: delay, MUX
0x2B	Reserved
0x2C	Output State QREF_A0

Table 26. Configuration Registers (Cont.)

Register Address	Register Description
0x2D	Output State QREF_A1
0x2E	Output State QREF_A2
0x2F	Reserved
0x30–0x32	Channel B
0x33	Reserved
0x34	Output State QCLK_B0
0x35	Output State QCLK_B1
0x36–0x37	Reserved
0x38	QREF_B0: delay, MUX
0x39	QREF_B1: delay, MUX
0x3A–0x3B	Reserved
0x3C	Output State QREF_B0
0x3D	Output State QREF_B1
0x3E–0x3F	Reserved
0x40–0x42	Channel C
0x43	Reserved
0x44	Output State QCLK_C0
0x45	Output State QCLK_C1
0x46–0x47	Reserved
0x48	QREF_C0: delay, MUX
0x49	QREF_C1: delay, MUX
0x4A–0x4B	Reserved
0x4C	Output State QREF_C0
0x4D	Output State QREF_C1
0x4E–0x4F	Reserved
0x50–0x52	Channel D
0x53	Reserved
0x54	Output State QCLK_D
0x55–0x57	Reserved
0x58	QREF_D: delay, MUX
0x59–0x5B	Reserved
0x5C	Output State QREF_D
0x5D–0x5F	Reserved
0x60–0x62	Channel E
0x63	Reserved



Table 26. Configuration Registers (Cont.)

Register Address	Register Description
0x64	Output State QCLK_E0
0x65	Output State QCLK_E1
0x66–0x67	Reserved
0x68–0x69	Interrupt Enable
0x6A–0x6B	Reserved
0x6C	Status (Latched)
0x6D	Status (Momentary)
0x6E	Status (Latched)
0x6F	Reserved
0x70	SYSREF Control RS
0x71–0x73	General Control
0x74–0x75	Output State QCLK
0x76	Output State QREF
0x77	Reserved
0x78–0x7A	Reserved
0x7B	Reserved
0x7C–0x7F	Reserved
0x80–0xFF	Reserved

## Register Descriptions

This section contains all addressable registers, sorted by function, followed for a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, with an additional table to indicate their addresses and default values. All writable register fields will come up with a default values as indicated in the *factory defaults* column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields may be used for internal debug test and debug functions.

### Channel and Clock Output Registers

The content of the channel register and clock output registers set the channel state, the clock divider, the QCLK output state and clock phase delay.

Table 27. Channel and Clock Output Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x20: Channel A 0x30: Channel B 0x40: Channel C 0x50: Channel D 0x60: Channel E				N_A[7:0] N_B[7:0] N_C[7:0] N_D[7:0] N_E[7:0]				
0x21: Channel A 0x31: Channel B 0x41: Channel C 0x51: Channel D 0x61: Channel E				ΦCLK_A[7:0] ΦCLK_B[7:0] ΦCLK_C[7:0] ΦCLK_D[7:0] ΦCLK_E[7:0]				
0x22: Channel A 0x32: Channel B 0x42: Channel C 0x52: Channel D 0x62: Channel E	PD_A PD_B PD_C PD_D PD_E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x24: QCLK_A0 0x25: QCLK_A1 0x26: QCLK_A2	PD_A0 PD_A1 PD_A2	Reserved	Reserved	STYLE_A0 STYLE_A1 STYLE_A2	A_A0[1:0] A_A1[1:0] A_A2[1:0]		Reserved	
0x34: QCLK_B0 0x35: QCLK_B1	PD_B0 PD_B1	Reserved	Reserved	STYLE_B0 STYLE_B1	A_B0[1:0] A_B1[1:0]		Reserved	
0x44: QCLK_C0 0x45: QCLK_C1	PD_C0 PD_C1	Reserved	Reserved	STYLE_C0 STYLE_C1	A_C0[1:0] A_C1[1:0]		Reserved	
0x54: QCLK_D	PD_D	Reserved	Reserved	STYLE_D	A_D[1:0]		Reserved	
0x64: QCLK_E0 0x65: QCLK_E1	PD_E0 PD_E1	Reserved	Reserved	STYLE_E0 STYLE_E1	A_E0[1:0] A_E1[1:0]		Reserved	
0x74	EN_QCLK_A0	EN_QCLK_A1	EN_QCLK_A2	EN_QCLK_B0	EN_QCLK_B1	EN_QCLK_C0	EN_QCLK_C1	EN_QCLK_D
0x75	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EN_QCLK_E1	EN_QCLK_E0

Table 28. Channel and Clock Output Register Descriptions<sup>[a]</sup>

Bit Field Location						
Bit Field Name	Field Type	Default (Binary)	Description			
N_x[7:0]	R/W	0000 0100 Value: ÷6	Output Frequency Divider N: N_x[7:0]      Divider Value			
			1000 0000	÷1	0100 0011	÷10
			0000 0000	÷2	0100 0100	÷12
			0000 0001	÷3	0100 0110	÷16
			0000 0010	÷4	0100 1011	÷20
			0000 0011	÷5	0100 1100	÷24
			0000 0100	÷6		
			0000 0110	÷8		
			0101 0011	÷30	0101 1011	÷40
			0100 1110	÷32	0101 0110	÷48
			0101 0100	÷36		
			0110 0011	÷50	0110 0100	÷60
					0101 1110	÷64
			0101 1111	÷72	0110 0110	÷80
0110 1110	÷96	0111 1011	÷100			
			0111 1100	÷120		
			0111 0110	÷128		
			0111 1110	÷160		
PD_x	R/W	0	0 = Channel <i>x</i> is powered-up. 1 = Channel <i>x</i> is powered-down.			
PD_y	R/W	0	0 = Output QCLK_y is powered-up. 1 = Output QCLK_y is powered-down.			
ΦCLK_x[7:0]	R/W	0000 0000	CLK_x Phase Delay: ΦCLK_x[7:0]			
			Delay in ps = ΦCLK_x × 339ps (256 steps): 0000 0000 = 0ps ... 1111 1111 = 86.466ns			

Table 28. Channel and Clock Output Register Descriptions<sup>[a]</sup> (Cont.)

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
A_y[1:0]	R/W	00	QCLK_y Output Amplitude
			Setting for STYLE = 0 (LVDS)
			Setting for STYLE = 1 (LVPECL)
			<div> <div> A[1:0] = 00: 250mV  A[1:0] = 01: 500mV  A[1:0] = 10: 750mV  A[1:0] = 11: 1000mV  Termination: 100Ω across </div> <div> A[1:0] = 00: 250mV  A[1:0] = 01: 500mV  A[1:0] = 10: 750mV  A[1:0] = 11: 1000mV  Termination: 50Ω to VT </div> </div>
STYLE_y	R/W	0	QCLK_y Output Format: 0 = Output is LVDS (requires an LVDS 100Ω output termination). 1 = Output is LVPECL (requires an LVPECL 50Ω output termination of the specified recommended termination voltage).
EN_y	R/W	0	QCLK_y Output Enable: 0 = QCLK_y Output is disabled at the logic low state. 1 = QCLK_y Output is enabled.

[a] x = A, B, C, D, E;  
 y = A0, A1, A2, B0, B1, C0, C1, D, E0, E1;  
 r = A0, A1, A2, B0, B1, C0, C1, D.

## QREF Output State Registers

The content of the output registers set the output frequency and divider, several output states, the power state, the output style and amplitude.

Table 29. QREF Output State Register Bit Field Locations<sup>[a]</sup>

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x28: QREF_A0 0x29: QREF_A1 0x2A: QREF_A2	Reserved	$\Phi$ REF_F[1:0]_A0 $\Phi$ REF_F[1:0]_A1 $\Phi$ REF_F[1:0]_A2		MUX_A0 MUX_A1 MUX_A2		$\Phi$ REF_AQ[2:0] $\Phi$ REF_AI[2:0] $\Phi$ REF_AZ[2:0]		$\Phi$ REF_F[2]_A0 $\Phi$ REF_F[2]_A1 $\Phi$ REF_F[2]_A2
0x38: QREF_B0 0x39: QREF_B1	Reserved	$\Phi$ REF_F[1:0]_B0 $\Phi$ REF_F[1:0]_B1		MUX_B0 MUX_B1		$\Phi$ REF_BQ[2:0] $\Phi$ REF_BI[2:0]		$\Phi$ REF_F[2]_B0 $\Phi$ REF_F[2]_B1
0x48: QREF_C0 0x49: QREF_C1	Reserved	$\Phi$ REF_F[1:0]_C0 $\Phi$ REF_F[1:0]_C1		MUX_C0 MUX_C1		$\Phi$ REF_CQ[2:0] $\Phi$ REF_CI[2:0]		$\Phi$ REF_F[2]_C0 $\Phi$ REF_F[2]_C1
0x58: QREF_D	Reserved	$\Phi$ REF_F[1:0]_D		MUX_D		$\Phi$ REF_D[2:0]		$\Phi$ REF_F[2]_D
0x2C: QREF_A0 0x2D: QREF_A1 0x2E: QREF_A2	PD_A0 PD_A1 PD_A2	Reserved	nBIAS_A0 nBIAS_A1 nBIAS_A2	STYLE_A0 STYLE_A1 STYLE_A2	A_AQ[1:0] A_AI[1:0] A_AZ[1:0]		Reserved	
0x3C: QREF_B0 0x3D: QREF_B1	PD_B0 PD_B1	Reserved	nBIAS_B0 nBIAS_B1	STYLE_B0 STYLE_B1	A_BQ[1:0] A_BI[1:0]		Reserved	
0x4C: QREF_C0 0x4D: QREF_C1	PD_C0 PD_C1	Reserved	nBIAS_C0 nBIAS_C1	STYLE_C0 STYLE_C1	A_CQ[1:0] A_CI[1:0]		Reserved	
0x5C: QREF_D	PD_D	Reserved	nBIAS_D	STYLE_D	A_D[1:0]		Reserved	
0x76	EN_QREF_A0	EN_QREF_A1	EN_QREF_A2	EN_QREF_B0	EN_QREF_B1	EN_QREF_C0	EN_QREF_C1	EN_QREF_D

[a] x = A, B, C, D, E;

y = A0, A1, A2, B0, B1, C0, C1, D, E0, E1;

r = A0, A1, A2, B0, B1, C0, C1, D.

Table 30. QREF Output State Register Descriptions<sup>[a]</sup>

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
MUX_ <i>r</i>	R/W	1	0 = QREF_ <i>r</i> output signal source is the channel's clock signal. 1 = QREF_ <i>r</i> output signal source is the centrally generated SYSREF signal.
ΦREF_ <i>r</i> [2:0]	R/W	000	SYSREF Coarse Phase Delay: ΦREF_ <i>r</i> [2:0]
			Delay in ps = ΦREF_ <i>r</i> [2:0] × 169ps (8 steps): 000 = 0ps ... 111 = 1.187ns
ΦREF_F[2:0]_ <i>r</i>	R/W	000	SYSREF Fine Phase Delay: ΦREF_F[2:0]_ <i>r</i>
			Insert a SYSREF fine phase delay in ps (8 steps) in addition to the delay value in: ΦREF_ <i>r</i> [2:0] 000 = 0ps 001 = 25ps 010 = 50ps 011 = 75ps 100 = 85ps 101 = 110ps 110 = 135ps 111 = 160ps
nBIAS_ <i>r</i>	R/W	0	QREF_ <i>r</i> Output Bias Voltage: 0 = Output is not voltage biased. 1 = Output is biased to the LVDS cross-point voltage if BIAS_TYPE (register 0x19, bit 7) is set to 1. Bit has no effect if BIAS_TYPE = 0. Output bias = 1 requires AC coupling and LVDS style on the corresponding output.

Table 30. QREF Output State Register Descriptions<sup>[a]</sup> (Cont.)

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
A <sub>r</sub> [1:0]	R/W	00	QREF <sub>r</sub> Output Amplitude
			Setting for STYLE <sub>r</sub> = 0 (LVDS)
			Setting for STYLE <sub>r</sub> = 1 (LVPECL)
			<div> A[1:0] = 00: 250mV  A[1:0] = 01: 500mV  A[1:0] = 10: 750mV  A[1:0] = 11:1000mV  Termination: 100Ω across </div> <div> A[1:0] = 00: 250mV  A[1:0] = 01: 500mV  A[1:0] = 10: 750mV  A[1:0] = 11:1000mV  Termination: 50Ω to VT </div>
PD <sub>r</sub>	R/W	0	QREF <sub>r</sub> Output Power-down: 0 = Output is powered-up. 1 = Output is powered-down. STYLE, EN and A[1:0] settings have no effect.
STYLE <sub>r</sub>	R/W	0	QREF <sub>r</sub> Output Format: 0 = Output is LVDS (requires an LVDS 100Ω output termination). 1 = Output is LVPECL (requires an LVPECL 50Ω output termination to the specified recommended termination voltage).
EN <sub>r</sub>	R/W	0	QREF <sub>r</sub> Output Enable: 0 = Output is disabled at the logic low state. 1 = Output is enabled.

[a] *x* = A, B, C, D, E;  
*y* = A0, A1, A2, B0, B1, C0, C1, D, E0, E1;  
*r* = A0, A1, A2, B0, B1, C0, C1, D.



## PLL Frequency Divider Registers

Table 31. PLL Frequency Divider Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00		$\Phi$ MV0[2:0]		PD_MV1		MV0[11:8]		
0x01					MV0[7:0]			
0x02					MV1[7:0]			
0x03	MV1[8]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPF
0x04		$\Phi$ PV[2:0]		Reserved		PV[11:8]		
0x05					PV[7:0]			
0x08	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MF[8]
0x09					MF[7:0]			
0x0C	FDF	Reserved				PF[5:0]		
0x1F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VCO_SEL

Table 32. PLL Frequency Divider Register Descriptions

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
$\Phi MV0[2:0]$	R/W	000	Phase of the $M_{V0}$ feedback divider. Determines the PLL lock-detect phase window in conjunction with $\Phi PV[2:0]$ . Sampling clock phase is relative to the VCXO-PLL phase detector clock edge. Set $\Phi MV0[2:0]$ in relationship to $M_{V0}$ :
			$M_{V0}$ Divider Value $\Phi MV0[2:0]$ Setting
			1–31
			32–63      010
			64–127      011
			128–255      100
			256–511      101
			512–1023      110
			1024+      111
$MV0[11:0]$	R/W	1100 0000 0000 Value: $\div 3072$	VCXO-PLL Feedback-Divider: The value of the frequency divider (binary coding). Range: $\div 1$ to $\div 4095$
$MV1[8:0]$	R/W	0 0110 0000 Value: $\div 96$	PLL Feedback-Divider: The value of the frequency divider (binary coding). Range: $\div 4$ to $\div 511$
$PD\_MV1$	R/W	0 Value: MV1 enabled	PLL Feedback-Divider $MV1$ Power-down/Disabled: 0 = $MV1$ Divider is enabled. 1 = $MV1$ Divider is powered down and disabled. Disabled $MV1$ to save power consumption in configurations not using the input clock monitors.
$\Phi PV[2:0]$	R/W	000	Phase of the $P_V$ input (reference) divider. Determines the PLL lock-detect phase window in conjunction with $\Phi MV0[2:0]$ . Sampling clock phase is relative to the VCXO-PLL phase detector clock edge. Set $\Phi PV[2:0]$ in relationship to $P_V$ :
			$P_V$ Divider Value $\Phi PV[2:0]$ Setting
			1–31
			32–63      010
			64–127      011
			128–255      100
			256–511      101
			512–1023      110
			1024+      111
$PV[11:0]$	R/W	1100 0000 0000 Value: $\div 3072$	VCXO-PLL Input Frequency Pre-Divider: The value of the frequency divider (binary coding). Range: $\div 1$ to $\div 4095$

Table 32. PLL Frequency Divider Register Descriptions (Cont.)

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
MF[8:0]	R/W	0 0001 1000 Value: $\div 24$	FemtoClock NG Pre-Divider: The value of the frequency divider (binary coding). Range: $\div 8$ to $\div 511$
PF[5:0]	R/W	00 0000 Value: Bypass	FemtoClock NG Pre-Divider: The value of the frequency divider (binary coding). Range: $\div 1$ to $\div 63$ 00 0000: $P_F$ is bypassed
FDF	R/W	0 Value: $f_{VCXO} \div P_F$	Frequency Doubler: The input frequency of the FemtoClock NG PLL (2nd stage) is: 0 = The output signal of the BYPV multiplexer, divided by the $P_F$ divider. 1 = The output signal of the BYPV multiplexer, doubled in frequency. Use this setting to improve phase noise. The $P_F$ divider has no effect if FDF = 1.
VCO_SEL	R/W	0 Value: $f_{VCO} = 2949.12\text{MHz}$	VCO Select: 0 = Selects VCO at $f_{VCO} = 2949.12\text{MHz}$ . 1 = Do not use.

# VCXO-PLL Control Registers

Table 33. VCXO-PLL Control Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x03	MV1[8]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPF
0x0A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPV
0x10	POLV	FVCV	Reserved			CPV[4:0]		
0x11	nPD_QOSC	STYLE_QOSC	OSVEN			OFFSET[4:0]		
0x12	Reserved	A_QOSC[1:0]				CPF[4:0]		

Table 34. VCXO-PLL Control Register Descriptions

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
BYPF	R/W	0	PLL Feedback Bypass: 0 = VCXO-PLL feedback divider: $M_{V0}$ 1 = VCXO-PLL feedback divider: $M_{V0} \times M_{V1}$
BYPV	R/W	0	VCXO-PLL Bypass: 0 = VCXO-PLL is enabled. 1 = VCXO-PLL is disabled and bypassed.
POLV	R/W	0	VCXO Polarity: 0 = Positive polarity. Use for an external VCXO with a positive $f(V_C)$ characteristics. 1 = Negative polarity. Use for an external VCXO with a negative $f(V_C)$ characteristics.
FVCV	R/W	1	VCXO-PLL Force VC Control Voltage: 0 = Normal operation. 1 = Forces the voltage at the LFV control pin (VCXO input) to $V_{DD\_V} / 2$ . VCXO-PLL unlocks and the VCXO is forced to its mid-point frequency. FVCV = 1 is the default setting at startup to center the VCXO frequency. FVCV should be cleared after startup to enable the PLL to lock to the reference frequency.
CPV[4:0]	R/W	1 1000 Value: 1.25mA	VCXO-PLL Charge-Pump Current: Controls the charge pump current $I_{CPV}$ of the VCXO-PLL. Charge pump current is the binary value of this register plus one multiplied by 50μA. $I_{CPV} = 50\mu A \times (CPV[4:0] + 1)$ CPV[4:0] = 00000 sets ICPV to the minimum current of 50μA. Maximum charge pump current is 1.6mA. Default setting is 1.25mA: $((24 + 1) \times 50\mu A)$ .

Table 34. VCXO-PLL Control Register Descriptions (Cont.)

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
nPD_QOSC	R/W	0	QOSC Power State: 0 = Output QOSC is powered-down. 1 = Output QOSC is powered-up.
STYLE_QOSC	R/W	0	QOSC Output Format: 0 = Output is LVDS (requires an LVDS 100Ω output termination). 1 = Output is LVPECL (requires an LVPECL 50Ω output termination of to the specified recommended termination voltage).
OSVEN	R/W	0	VCXO-PLL Offset Enable: 0 = No offset. 1 = Offset enabled. A static phase offset of OFFSET[4:0] is applied to the PFD of the VCXO-PLL.
OFFSET[4:0]	R/W	0 0000 Value: 0°	VCXO-PLL Static Phase Offset: Controls the static phase detector offset of the VCXO-PLL. Phase offset is the binary value of this register multiplied by 0.9° of the PFD input signal (OFFSET [4:0] × f <sub>PFD</sub> ÷ 400). Maximum offset is 31 × 0.9° = 27.9°. Setting OFFSET to 0.0° eliminates the thermal noise of an offset current. If the VCXO-PLL input jitter period T <sub>JIT</sub> exceeds the average input period: set OFFSET to a value larger than f <sub>PFD</sub> × T <sub>JIT</sub> × 400 to achieve a better charge pump linearity and lower in-band noise of the PLL.
CPF[4:0]	R/W	1 1000 Value: 5.0mA	FemtoClock NG-PLL Charge-Pump Current: Controls the charge pump current I <sub>CPF</sub> of the FemtoClock NG PLL. Charge pump current is the binary value of this register plus one multiplied by 200μA. $I_{CPF} = 200\mu A \times (CPF[4:0] + 1)$ CPV[4:0] = 00000 sets I <sub>CPF</sub> to the minimum current of 200μA. Maximum charge pump current is 6.4mA. Default setting is 5.0mA: ((24+1) × 200μA).
A_QOSC[1:0]	R/W	00 Value: 250mV	QOSC Output Amplitude
			Setting for STYLE_r = 0 (LVDS)
			Setting for STYLE_r = 1 (LVPECL)
			A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 500mV A[1:0] = 11: 750mV Termination: 100Ω across
			A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 500mV A[1:0] = 11: 750mV Termination: 50Ω to VT

## Input Selection Mode Registers

Table 35. Input Selection Mode Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x14	PRIO_0[1:0]		PRIO_1[1:0]		PRIO_2[1:0]		PRIO_3[1:0]	
0x15	Reserved	BLOCK_LOR	DIV4_VAL	REVS	nM/A[1:0]		SEL[1:0]	
0x16	CNTH[7:0]							
0x17	CNTR[1:0]		PD_CLK3	PD_CLK2	PD_CLK1	PD_CLK0	CNTV[1:0]	

Table 36. Input Selection Mode Register Descriptions

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
PRI0_ <i>n</i> [1:0]	R/W	CLK_0: 11 CLK_1: 10 CLK_2: 01 CLK_3: 00	Controls the auto-selection priority of the clock input CLK_ <i>n</i> ( <i>n</i> = 0...3). If multiple inputs have equal priority, the order within that priority is from CLK0 (highest) to CLK3 (lowest): 00 = Priority 0 (lowest) 01 = Priority 1 10 = Priority 2 11 = Priority 3 (highest)
DIV4_VAL	R/W	0 Value: ÷1	Pre-divider for CNTV[1:0]. Use the ÷4 pre-divider for input frequencies >250MHz: 0 = ÷1 1 = ÷4
REVS	R/W	0 Value: off	Revertive Switching: The revertive input switching setting is only applicable to the two automatic selection modes shown in Table 10. If nM/A[1:0] = X0, the REVS setting has no meaning. 0 = Disabled: Re-validation of a non-selected input clock has no impact on the clock selection. 1 = Enabled: Re-validation of any non-selected input clock(s) will cause a new input selection according to the pre-set input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the current VCXO-PLL reference clock. Default setting is revertive switching turned off.
nM/A[1:0]	R/W	00 Value: Manual Selection	Reference Input Selection Mode: In any of the manual selection modes (nM/A[1:0] = 00 or 10), the VCXO-PLL reference input is selected by SEL[1:0]. In any of the automatic selection modes, the VCXO-PLL reference input is selected by an internal state machine according to the input LOS states and the priorities in the input priority registers. 00 = Manual selection 01 = Automatic selection (no holdover) 10 = Short-term holdover 11 = Automatic selection with holdover
SEL[1:0]	R/W	00 Value: CLK0 selected	VCXO-PLL Input Reference Selection: Controls the selection of the VCXO-PLL reference input in the manual selection modes. In automatic selection modes (nM/A[1:0] = X1), SEL[1:0] has no meaning. 00 = CLK_0 01 = CLK_1 10 = CLK_2 11 = CLK_3

Table 36. Input Selection Mode Register Descriptions (Cont.)

Bit Field Location				
Bit Field Name	Field Type	Default (Binary)	Description	
CNTH[7:0]	R/W	1000 0000 Value: 136ms	nMA[1:0] = 11 Automatic with holdover: Hold-off counter period. The device initiates a clock fail-over switch upon counter expiration (zero transition). The counters start to counts backwards after an LOS event is detected. The hold-off counter period is determined by the binary number of VCXO-PLL output pulses divided by CNTR[1:0]. With a VCXO frequency of 122.88MHz and CNTR[1:0] = 10, the counter has a period of (1.066 ms × binary setting). After each zero-transition, the counter automatically re-loads to the setting in this register. The default setting is 136ms (VCXO = 122.88MHz: $1/122.88\text{MHz} \times 2^{17} \times 128$ ).	
CNTR[1:0]	R/W	10 Value: $2^{17}$	nMA[1:0] = 11 Automatic with Holdover: Reference Divider	
			CNTR[1:0]	CNTH frequency (period; range)
			122.88MHz VCXO	38.4MHz VCXO
			00 = $f_{\text{VCXO}} \div 2^{15}$	— 1171Hz (0.853ms; 0–217.6ms)
			01 = $f_{\text{VCXO}} \div 2^{16}$	1875Hz (0.533ms; 0–136ms) —
			10 = $f_{\text{VCXO}} \div 2^{17}$	937.5Hz (1.066ms; 0–272ms) —
CNTV[1:0]	R/W	10 Value: 32	Controls the number of required consecutive, valid input reference pulses for clock re-validation on CLK_n (n = 0...3), in number of input periods. At an LOS event, the re-validation counter loads this setting from the register and counts down by one with every valid, consecutive input signal period. Missing input edges (for one input period) will cause this counter to re-load its setting. An input is re-validated when the counter transitions to zero and the corresponding LOS flag is reset. DIV4_VAL = 0 DIV4_VAL = 1	
			00 = 2 (shortest possible) 01 = 16 10 = 32 11 = 64	00 = 8 (shortest possible) 01 = 64 10 = 128 11 = 256
PD_CLK_3 PD_CLK_2 PD_CLK_1 PD_CLK_0	R/W	0 Powered-up/ Enabled	Input CLK_n Power-down/ Disable: 0 = Input CLK_n is enabled. 1 = Input CLK_n is powered-down and disabled. Disable individual Input CLK_n input to save power consumption in configurations not using the respective input and in manual switching or short-term holdover mode. Enable inputs CLK_n in configurations with automatic switching.	
BLOCK_LOR	R/W	0 Value: Not blocked	Block Loss-of-reference (input activity) Indicator: VCXO-PLL Loss-of-lock signals nST_LOLV and nLS_LOLV are triggered by: 0 = VCXO-PLL Loss-of-lock or by inactivity of the selected reference clock. 1 = Only VCXO-PLL loss-of-lock. BLOCK_LOR = 1 will also block loss-of-reference from triggering a failure on the LOCK output pin.	



# SYSREF Control Registers

Table 37. SYSREF Control Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x18	PD_S				NS[6:0]			
0x19	BIAS_TYPE				SYNC[6:0]			
0x1A					SRPC[7:0]			
0x1B					$\Phi$ REF_S[7:0]			
0x1C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SRG	SRO
0x70	RS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 38. SYSREF Control Register Descriptions

Bit Field Location																							
Bit Field Name	Field Type	Default (Binary)	Description																				
PD_S	R/W	0	SYSREF Global Power-down (including global delay $\Phi$ S, SYSREF frequency divider NS): 0 = SYSREF functional blocks are powered-up. 1 = SYSREF functional blocks are powered-down.																				
NS[6:0]	R/W	010 11 11  Value: ÷1280	<p>SYSREF Frequency Divider:</p> <p>The value of the frequency divider is set by the product of:  <math>NS[6] \times NS[5:4] \times NS[3:2] \times NS[1:0]</math>.</p> <table> <tr> <td>NS[6]</td> <td>NS[5:4]</td> <td>NS[3:2]</td> <td>NS[1:0]</td> </tr> <tr> <td>0 = ÷2</td> <td>00 = ÷2</td> <td>00 = ÷2</td> <td>00 = ÷2</td> </tr> <tr> <td>1 = ÷4</td> <td>01 = ÷4</td> <td>01 = ÷4</td> <td>01 = ÷3</td> </tr> <tr> <td></td> <td>10 = ÷8</td> <td>10 = ÷8</td> <td>10 = ÷4</td> </tr> <tr> <td></td> <td>11 = ÷16</td> <td>11 = ÷16</td> <td>11 = ÷5</td> </tr> </table> <p>The SYSREF contains four serial dividers that can be individually controlled by NS[6], NS[5:4], NS[3:2] and NS[1:0], respectively. The total NS divider is the product of the four serial dividers. Example: to achieve a SYSREF divider value of ÷384 = {2} × {4} × {16} × {3}, set NS[6] = 0, NS[5:4] = 01, NS[3:2] = 11 and NS[1:0] = 01.</p> <p>If a given output divider can be achieved by multiple NS[6:0] settings, use the highest possible divider in NS[1:0], then in NS[3:2], followed by NS[5:4] = 11 and then NS[6].</p>	NS[6]	NS[5:4]	NS[3:2]	NS[1:0]	0 = ÷2	00 = ÷2	00 = ÷2	00 = ÷2	1 = ÷4	01 = ÷4	01 = ÷4	01 = ÷3		10 = ÷8	10 = ÷8	10 = ÷4		11 = ÷16	11 = ÷16	11 = ÷5
NS[6]	NS[5:4]	NS[3:2]	NS[1:0]																				
0 = ÷2	00 = ÷2	00 = ÷2	00 = ÷2																				
1 = ÷4	01 = ÷4	01 = ÷4	01 = ÷3																				
	10 = ÷8	10 = ÷8	10 = ÷4																				
	11 = ÷16	11 = ÷16	11 = ÷5																				

Table 38. SYSREF Control Register Descriptions (Cont.)

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
BIAS_TYPE	R/W	1	SYSREF Output Voltage Bias: 0 = QREF_r outputs are in a low/high state when nBIAS_r is set to 1 or during a SYSREF event. 1 = QREF_r outputs are in a cross-point biased state when nBIAS_r is set to 1 or during a SYSREF event.
SYNC[6:0]	R/W	00 00 001	SYSREF Synchronizer divider value. This divider controls the release of SYSREF pulses at coincident QCLK clock edges. For SYSREF operation, set this divider value to the least common multiple of the clock divider values $N_x$ ( $x = A$ to $E$ ). For instance, if $N_A = N_B = \div 2$ , $N_C = N_D = \div 3$ , $N_E = \div 4$ set the SYNC divider to $\div 12$ .
			SYNC6 Description: 0: SYNC[6] = 0: output frequency divider set by SYNC[2:0]. 1: SYNC[6] = 1: output frequency divider set by the product of SYNC[5:3] $\times$ SYNC[2:0].
			SYNC[5:3]                      SYNC[2:0]
			000 = $\div 2$ 001 = $\div 4$ 010 = $\div 6$ 011 = $\div 8$ 100 = $\div 4$ 101 = $\div 8$ 110 = $\div 12$ 111 = $\div 16$
			000 = $\div 2$ 001 = $\div 3$ 010 = $\div 4$ 011 = $\div 5$ 100 = $\div 6$ 101 = $\div 7$ 110 = $\div 8$ 111 = $\div 9$
			The frequency divider SYNC is composed of 2 serial dividers that can be individually controlled by the bit fields SYNC[5:3] and SYNC[2:0]. Set SYNC[6] = 0 to achieve an output divider in the range of {2, 3, 4, 5, 6, 7, 8, 9}. Set SYNC[6] = 1 to achieve an output divider value of {2, 4, 6, 8, 12, 16} $\times$ {2, 3, 4, 5, 6, 7, 8, 9}. For instance, the output divider of $\div 32 = \{4\} \times \{8\}$ is set by SYNC[6:0] = 1001110. If a given output divider can be achieved by multiple SYNC[6:0] settings, a setting with SYNC[6] = 0 is preferred. If SNYC[6] = 1, the higher divider value should be configured with SYNC[2:0].
SRPC[7:0]	R/W	0000 0010  Value: 2	SYSREF Pulse Count: Binary value of the number of SYSREF pulses generated and output at all enabled QREF outputs. Allows the generation of 1 to 255 pulses after each write access. Requires setting SRG = 0, and SRO = 0.

Table 38. SYSREF Control Register Descriptions (Cont.)

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
ΦREF_S[7:0]	R/W	0000 0000	ΦREF_S global SYSREF phase delay. This setting affects all QREF_r outputs configured as SYSREF: ΦREF_S[7:0]
			Delay in ps = ΦREF_S × 339ps (256 steps): 0000 0000 = 0ps ... 1111 1111 = 86.466ns
SRG	R/W	0	SYSREF Pulse Generation: 0 = Internal SPI controlled SYSREF generation triggered by the RS bit. 1 = External controlled SYSREF generation using the EXT_SYS pin.
SRO	R/W	0	SYSREF Pulse Mode: 0 = Counted SYSREF pulse generation mode. Number of pulses is controlled by SRPC[7:0]. 1 = Continuous SYSREF pulse generation.
RS	W only Auto-Clear	X	Set RS = 1 to initiate the SYSREF pulse generation of SRPC-number of pulses. Powers up the SYSREF circuitry and releases the SYSREF pulse(s) as configured. RS = 1 also phase-aligns the QREF outputs to the QCLK outputs and adds the programmed delay values into the QREF paths. RS auto-clears in SYSREF counted pulse mode (if SRO = 0): SRG = 0 (internal generation): Each setting of RS initiates SYSREF pulse(s). SRG = 1 (external generation): Set RS = 1 to prepare SYSREF generation triggered by a rising edge at the EXT_SYS pin.

# Status Registers

Table 39. Status Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x68	Reserved	Reserved	IE_LOLF	IE_LOLV	IE_CLK_3	IE_CLK_2	IE_CLK_1	IE_CLK_0
0x69	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IE_REF	IE_HOLD
0x6C	Reserved	Reserved	nLS_LOLF	nLS_LOLV	LS_CLK_3	LS_CLK_2	LS_CLK_1	LS_CLK_0
0x6D	ST_SEL[1:0]		nST_LOLF	nST_LOLV	ST_CLK_3	ST_CLK_2	ST_CLK_1	ST_CLK_0
0x6E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LS_REF	nLS_HOLD
0x6F	Reserved	Reserved	Reserved	Reserved	Reserved	ST_VCOF	ST_REF	nST_HOLD

Table 40. Status Register Descriptions<sup>[a]</sup>

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
IE_LOLF	R/W	0	Interrupt Enable for FemtoClock NG-PLL Loss-of-lock: 0 = Disabled: Setting nLS_LOLF will not cause an interrupt on nINT 1 = Enabled: Setting nLS_LOLF will assert the nINT output (nINT = 0, interrupt)
IE_LOLV	R/W	0	Interrupt Enable for VCXO-PLL Loss-of-lock: 0 = Disabled: Setting nLS_LOLV will not cause an interrupt on nINT. 1 = Enabled: Setting nLS_LOLV will assert the nINT output (nINT = 0, interrupt).
IE_CLK <sub>n</sub>	R/W	0	Interrupt Enable for CLK <sub>n</sub> input Loss-of-signal: 0 = Disabled: Setting LS_CLK <sub>n</sub> will not cause an interrupt on nINT. 1 = Enabled: Setting LS_CLK <sub>n</sub> will assert the nINT output (nINT = 0, interrupt).
IE_REF	R/W	0	Interrupt Enable for LS_REF: 0 = Disabled: any changes to LS_REF will not cause an interrupt on nINT. 1 = Enabled: any changes to LS_REF will assert the nINT output (nINT = 0, interrupt).
IE_HOLD	R/W	0	Interrupt Enable for Holdover: 0 = Disabled: Setting nLS_HOLD will not cause an interrupt on nINT. 1 = Enabled: Setting nLS_HOLD will assert the nINT output (nINT = 0, interrupt).
nLS_LOLF	R/W	—	FemtoClock NG-PLL Loss-of-lock (latched status of nST_LOLF): Read 0 = ≥1 Loss-of-lock events detected after the last nLS_LOLF status latch clear. Read 1 = No Loss-of-lock detected after the last nLS_LOLF status latch clear. Write 1 = Clear status latch (clears pending nLS_LOLF interrupt).

Table 40. Status Register Descriptions<sup>[a]</sup> (Cont.)

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
nLS_LOLV	R/W	—	VCXO-PLL Loss-of-lock (latched status of nST_LOLV): Read 0 = $\geq 1$ Loss-of-lock events detected after the last nLS_LOLV status latch clear. Read 1 = No Loss-of-lock detected after the last nLS_LOLV status latch clear. Write 1 = Clear status latch (clears pending nLS_LOLV interrupt).
LS_CLK_n	R/W	—	Input CLK_n Status (latched status of ST_CLK_n): Read 0 = $\geq 1$ LOS events detected on CLK_n after the last LS_CLK_n status latch clear. Read 1 = No Loss-of-signal detected on CLK_n input after the last LS_CLK_n status latch clear. Write 1 = Clear LS_CLK_n status latch (clears pending LS_CLK_n interrupts on nINT).
ST_SEL[1:0]	R	—	Input Selection (momentary): Reference Input Selection Status of the state machine. In any input selection mode, reflects the input selected by the state machine: 00 = CLK_0 01 = CLK_1 10 = CLK_2 11 = CLK_3
nST_LOLF	R	—	FemtoClock NG-PLL Loss-of-lock (momentary): Read 0 = Loss-of-lock event detected. Read 1 = No Loss-of-lock detected. A latched version of this status bit is available (nLS_LOLF).
nST_LOLV	R	—	VCXO-PLL Loss-of-lock (momentary): Read 0 = Loss-of-lock event detected. Read 1 = No Loss-of-lock detected. A latched version of this status bit is available (nLS_LOLV).
ST_CLK_n	R	—	Input CLK_n Status (momentary): 0 = LOS detected on CLK_n. 1 = No LOS detected, CLK_n input is active. Latched versions of these status bits are available (LS_CLK_n).
LS_REF	R/W	—	PLL Reference Status (latched status of ST_REF): Read 0 = Reference is lost after the last LS_REF status latch clear. Read 1 = Reference is valid after the last LS_REF status latch clear. Write 1 = Clear LS_REF status latch (clears pending LS_REF interrupts on nINT).

Table 40. Status Register Descriptions<sup>[a]</sup> (Cont.)

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
nLS_HOLD	R/W	—	Holdover Status Indicator (latched status of nST_HOLD): Read 0 = VCXO-PLL has entered holdover state at least 1 time after the last nLS_HOLD status latch clear. Read 1 = VCXO-PLL is (or attempts to) lock(ed) to an input clock. Write 1 = Clear status latch (clears pending nLS_HOLD interrupt).
ST_VCOF	R	—	FemtoClock NG-PLL Calibration Status (momentary): Read 0 = FemtoClock NG PLL auto-calibration is completed. Read 1 = FemtoClock NG PLL calibration is active (not completed).
ST_REF	R	—	Input Reference Status: 0 = No input reference present. 1 = Input reference is present.
nST_HOLD	R	—	Holdover Status Indicator (momentary): 0 = VCXO-PLL in holdover state, not locked to any input clock. 1 = VCXO-PLL is (or attempts to) lock(ed) to input clock. A latched version of this status bit is available (nLS_HOLD).

[a] CLK $n$  = CLK0, CLK1, CLK2, CLK3.

## General Control Registers

Table 41. General Control Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x71	INIT_CLK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x72	RELOCK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x73	PB_CAL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CPOL

Table 42. General Control Register Descriptions

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
INIT_CLK	W only Auto-Clear	X	Set INIT_CLK = 1 to initialize divider functions. Required as part of the startup procedure.
RELOCK	W only Auto-Clear	X	Setting this bit to 1 will force the FemtoClock NG PLL to re-lock.
PB_CAL	W only Auto-Clear	X	Precision Bias Calibration: Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as a reference for outputs configured as LVDS and as a reference for the charge pump currents. This bit will auto-clear after the calibration is completed. Set as part of the startup procedure.
CPOL	R/W	0	SPI Read Operation SCLK Polarity: 0 = Data bits on SDAT are output at the falling edge of SCLK edge. 1 = Data bits on SDAT are output at the rising edge of SCLK edge.

# Electrical Characteristics

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V19N490 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 43. Absolute Maximum Ratings

Item	Rating
Supply Voltage, $V_{DD\_V}$	3.6V
Inputs	-0.5V to $V_{DD\_V} + 0.5V$
Outputs, $V_O$ (LVCMOS)	-0.5V to $V_{DD\_V} + 0.5V$
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	50mA 100mA
Input Termination Current, $I_{VT}$	$\pm 35mA$
Operating Junction Temperature, $T_J$	125°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
ESD - Human Body Model <sup>[a]</sup>	2000V
ESD - Charged Device Model <sup>[a]</sup>	500V

[a] According to JEDEC JS-001-2012/JESD22-C101.



## Input Characteristics

Table 44. Input Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}^{[a]}$	Input Capacitance	OSC, nOSC			2	4	pF
		Other inputs			2	4	pF
$R_{PU}$	Input Pull-up Resistor	nOSC, SDAT, nCS, nCLK_[0:3]			51		k $\Omega$
$R_{PD}$	Input Pull-down Resistor	EXT_SYS, CLK_[0:3], nCLK_[0:3], OSC, nOSC, SCLK, SELSV			51		k $\Omega$
$R_{OUT}$	LVC MOS Output Impedance	nINT, LOCK			25		$\Omega$

[a] Guaranteed by design.

## DC Characteristics

Table 45. Power Supply DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD\_V}$	Core Supply Voltage		3.135	3.3	3.465	V
$I_{DD\_V}$	Total Power Supply Current			1395		mA

Table 46. Typical Power Supply DC Current Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ <sup>[a]</sup>

Symbol	Supply Pin Current		Test Case						Unit
			1	2	3	4	5	6	
—	QCLK_y	Style	LVPECL	LVPECL	LVPECL	LVPECL	LVDS	LVDS	—
		State	On	On	On	On	On	On	—
		Amplitude	500	750	1000	250	500	750	mV
—	QREF_r	Style	LVDS	LVDS	LVDS	LVDS	LVDS	LVDS	—
		State	On	On	Off	On	Off	Off	—
		Amplitude	500	500	—	250	—	—	mV
$I_{DD\_CA}$	Current through VDD_QCLKA pin		101.1	115.7	135.5	86.6	78.6	102.2	mA
$I_{DD\_CB}$	Current through VDD_QCLKB pin		81.7	93.2	96.6	70.6	58.0	73.0	mA
$I_{DD\_CC}$	Current through VDD_QCLKC pin		82.2	93.3	101.4	71.1	58.3	73.5	mA
$I_{DD\_CD}$	Current through VDD_QCLKD pin		51.1	56.7	61.4	45.5	38.0	46.8	mA
$I_{DD\_CE}$	Current through VDD_QCLKE pin		70.5	79.4	88.7	61.4	59.4	75.3	mA
$I_{DD\_RA}$	Current through VDD_QREFA pin		77.3	77.1	2.3	55.7	2.3	2.3	mA
$I_{DD\_RB}$	Current through VDD_QREFB pin		51.2	51.3	1.5	36.9	1.5	1.6	mA
$I_{DD\_RC}$	Current through VDD_QREFC pin		51.3	51.3	1.6	36.9	1.6	1.6	mA
$I_{DD\_RD}$	Current through VDD_QREFD pin		26.1	25.9	0.8	18.7	0.8	0.8	mA
$I_{DD\_INP}$	Current through VDD_INP pin		80.5	81.0	81.8	80.1	82.6	83.3	mA
$I_{DD\_SPI}$	Current through VDD_SPI pin		6.0	6.5	6.4	4.4	5.9	6.0	mA
$I_{DD\_OSC}$	Current through VDD_OSC and VDD_CP pins		38.7	38.8	38.9	38.6	39.3	39.0	mA
$I_{DD\_SYNC}$	Current through VDD_SYNC pin		82.6	82.6	1.9	82.8	1.9	1.9	mA
$I_{DD\_CPF}$	Current through VDD_CPF pin		59.4	59.5	59.4	59.4	59.4	60.2	mA
$I_{DD\_LCV}$	Current through VDD_LCV pin		72.3	72.3	72.2	72.3	74.4	76.9	mA
$I_{DD\_LCF}$	Current through VDD_LCF pin		52.2	52.0	52.5	52.5	52.4	52.4	mA
$P_{TOT}$	Total Device Power Consumption		2.76	2.87	2.06	2.46	2.03	2.3	W
$P_{TOT, SYS}$	Total System Power Consumption <sup>[b]</sup>		3.25	3.43	2.65	2.89	2.03	2.30	W

[a] Configuration:  $f_{CLK}$  (input) = 122.88MHz,  $f_{SYSREF}$  = 7.68MHz, internal SYSREF generation (continuous), QA[2:0] = 1474.56MHz, QB[1:0] = 245.76MHz, QC[1:0] = 245.76MHz, QD = 491.52MHz, QE[1:0] = 122.88MHz). QCLK\_y outputs terminated according to amplitude settings. QREF\_r outputs unterminated when SYSREF is turned off.

[b] Includes total device power consumption and the power dissipated in external output termination components.

Table 47. LVCMOS DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Control Input SELSV (3.3V logic)							
V <sub>IH</sub>	Input High Voltage			2.0		V <sub>DD_V</sub>	V
V <sub>IL</sub>	Input Low Voltage			-0.3		0.8	V
I <sub>IH</sub>	Input High Current	Input with pull-down resistor	V <sub>DD_V</sub> = 3.3V, V <sub>IN</sub> = 3.3V			150	μA
I <sub>IL</sub>	Input Low Current		V <sub>DD_V</sub> = 3.3V, V <sub>IN</sub> = 0V	-5			μA
SYSREF Trigger Input EXT_SYS (1.8V/3.3V selectable logic)							
V <sub>IH</sub>	Input High Voltage		1.8V logic (SELSV = 0)	1.17		V <sub>DD_V</sub>	V
			3.3V logic (SELSV = 1)	2.0		V <sub>DD_V</sub>	V
V <sub>IL</sub>	Input Low Voltage		1.8V logic (SELSV = 0)	-0.3		0.63	V
			3.3V logic (SELSV = 1)	-0.3		0.8	V
I <sub>IH</sub>	Input High Current	Input with pull-down resistor	V <sub>DD_V</sub> = 3.3V, V <sub>IN</sub> = 1.8V or 3.3V			150	μA
I <sub>IL</sub>	Input Low Current		V <sub>DD_V</sub> = 3.3V, V <sub>IN</sub> = 0V	-5			μA
SPI Inputs SDAT (when input), SCLK, nCS (1.8V/3.3V selectable logic with input hysteresis)							
V <sub>I</sub>	Input Voltage			-0.3		V <sub>DD_V</sub>	V
V <sub>T+</sub>	Positive-going Input Threshold Voltage		1.8V logic (SELSV = 0)	0.660		1.350	V
			3.3V logic (SELSV = 1)		1.8–2.1		V
V <sub>T-</sub>	Negative-going Input Threshold Voltage		1.8V logic (SELSV = 0)	0.495		1.170	V
			3.3V logic (SELSV = 1)		0.75–0.97		V
V <sub>H</sub>	Hysteresis Voltage		V <sub>T+</sub> – V <sub>T-</sub>	0.165		0.780	V
SPI output DAT (when output), nINT, LOCK (1.8V/3.3V selectable logic)							
V <sub>OH</sub>	Output High Voltage		1.8V logic (SELSV = 0) I <sub>OH</sub> = -4mA	1.35			V
			3.3V logic (SELSV = 1) I <sub>OH</sub> = -4mA	2.4			V
V <sub>OL</sub>	Output Low Voltage		1.8V logic (SELSV = 0) I <sub>OL</sub> = 4mA			0.45	V
			3.3V logic (SELSV = 1) I <sub>OL</sub> = 4mA			0.4	V

Table 48. Differential Input DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	Inputs with pull-down resistor <sup>[a]</sup>	$V_{DD\_V} = V_{IN} = 3.465V$			150	$\mu A$
		Pull-down/pull-up inputs <sup>[b]</sup>				150	$\mu A$
$I_{IL}$	Input Low Current	Inputs with pull-down resistor	$V_{DD\_V} = 3.465V$ , $V_{IN} = 0V$	-150			$\mu A$
		Pull-down/pull-up inputs <sup>[b]</sup>		-150			$\mu A$

[a] Non-Inverting inputs: CLK\_n, OSC.

[b] Inverting inputs: nCLK\_n, nOSC.

Table 49. LVPECL DC Characteristics (QCLK\_y, QREF\_r, STYLE = 1),  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage <sup>[a]</sup>	250mV amplitude setting	$V_{DD\_V} - 0.975$	$V_{DD\_V} - 0.875$	$V_{DD\_V} - 0.774$	V
		500mV amplitude setting	$V_{DD\_V} - 1.000$	$V_{DD\_V} - 0.904$	$V_{DD\_V} - 0.805$	V
		750mV amplitude setting	$V_{DD\_V} - 1.100$	$V_{DD\_V} - 0.937$	$V_{DD\_V} - 0.829$	V
		1000mV amplitude setting	$V_{DD\_V} - 1.100$	$V_{DD\_V} - 0.962$	$V_{DD\_V} - 0.861$	V
$V_{OL}$	Output Low Voltage	250mV amplitude setting	$V_{DD\_V} - 1.250$	$V_{DD\_V} - 1.150$	$V_{DD\_V} - 1.040$	V
		500mV amplitude setting	$V_{DD\_V} - 1.540$	$V_{DD\_V} - 1.420$	$V_{DD\_V} - 1.131$	V
		750mV amplitude setting	$V_{DD\_V} - 1.810$	$V_{DD\_V} - 1.690$	$V_{DD\_V} - 1.580$	V
		1000mV amplitude setting	$V_{DD\_V} - 2.090$	$V_{DD\_V} - 1.960$	$V_{DD\_V} - 1.840$	V

[a] Outputs terminated with  $50\Omega$  to  $V_{DD\_V} - 1.5V$  (250mV amplitude setting),  $V_{DD\_V} - 1.75V$  (500mV amplitude setting),  $V_{DD\_V} - 2.0V$  (750mV amplitude setting),  $V_{DD\_V} - 2.25V$  (1000mV amplitude setting).

Table 50. LVDS DC Characteristics (QCLK\_y, QREF\_r, STYLE = 0),  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OS}$	Offset Voltage <sup>[a]</sup>	250mV amplitude setting	2.10	2.40	2.70	V
		500mV amplitude setting	1.90	2.23	2.60	V
		750mV amplitude setting	1.80	2.08	2.4	V
		1000mV amplitude setting	1.60	1.93	2.20	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				80	mV

[a]  $V_{OS}$  changes with  $V_{DD\_V}$ .

## AC Characteristics

Table 51. AC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  [a] [b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$f_{VCO}$	VCO Frequency			2920	2949.12	3000	MHz
$f_{OUT}$	Output Frequency	QCLK_y, QREF_r (lock)	$N = \div 1$		2949.12		MHz
		QCLK_y, QREF_r (lock)	$N = \div 2$		1474.56		MHz
		QCLK_y, QREF_r (clock)	$N = \div 3$		983.04		MHz
		QCLK_y, QREF_r (clock)	$N = \div 6$		491.52		MHz
		QCLK_y, QREF_r (clock)	$N = \div 12$		245.76		MHz
		QCLK_y, QREF_r (clock)	$N = \div 24$		122.88		MHz
		QREF_r (SYSREF)		0.576		30.72	MHz
$f_{CLK}$	Input Frequency	CLK_n		1.92 <sup>[c]</sup>	245.76	2000	MHz
$f_{VCXO}$	VCXO Frequency			30.72	122.88		MHz
$\Delta_{fp}$	Static Frequency Error		$f_{CLK} = 0$ ppb frequency deviation			0	ppb
$\Delta_{frms}$	Dynamic Frequency Error RMS <sup>[d]</sup>		$f_{CLK} = 0$ ppb frequency deviation			0.5	ppb
$V_{IN}$	Input Voltage Amplitude <sup>[e]</sup>	CLK_n, OSC/nOSC		0.15		1.2	V
$V_{DIFF\_IN}$	Differential Input Voltage Amplitude <sup>[e], [f]</sup>	CLK_n, OSC/nOSC		0.3		2.4	V
$V_{CMR}$	Common Mode Input Voltage			1.0		$V_{DD\_V} - (V_{IN} / 2)$	V
odc	Output Duty Cycle		QCLK_y, QREF_r (clock)	45	50	55	%
$t_R / t_F$	Output Rise/Fall Time, Differential	LVPECL QCLK_y, QREF_r	20% to 80%			250	ps
		LVDS QCLK_y, QREF_r	20% to 80%			250	ps
		SYSREF, LVDS QREF_r	20% to 80%			250	ps
	Output Rise/Fall Time	LVC MOS outputs	20% – 80%			1	ns

Table 51. AC Characteristics,  $V_{DD_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ <sup>[a]</sup> <sup>[b]</sup> (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{O(PP)}$ <sup>[g]</sup>	LVPECL Output Voltage Swing, Peak-to-peak; (see Table 54)	250mV amplitude	1474.56MHz 491.52MHz	190 211	272 265	367 327	mV
		500mV amplitude	1474.56MHz 491.52MHz	394 422	505 499	634 581	mV
		750mV amplitude	1474.56MHz 491.52MHz	598 629	733 734	875 841	mV
		1000mV amplitude	1474.56MHz 491.52MHz	784 837	946 970	1090 1110	mV
	LVPECL Differential Output Voltage Swing, Peak-to-peak; 1474.56MHz; (see Table 54)	250mV amplitude	1474.56MHz 491.52MHz	380 422	544 530	734 654	mV
		500mV amplitude	1474.56MHz 491.52MHz	788 844	1010 998	1268 1162	mV
		750mV amplitude	1474.56MHz 491.52MHz	1196 1258	1466 1468	1750 1682	mV
		1000mV amplitude	1474.56MHz 491.52MHz	1586 1674	1892 1940	2180 2220	mV
$V_{OD}$ <sup>[h]</sup>	LVDS Output Voltage Swing, Peak-to-peak; 1474.56MHz; (see Table 54)	250mV amplitude	1474.56MHz 491.52MHz	128 162	193 219	273 290	mV
		500mV amplitude	1474.56MHz 491.52MHz	312 385	404 456	512 536	mV
		750mV amplitude	1474.56MHz 491.52MHz	490 605	615 697	757 795	mV
		1000mV amplitude	1474.56MHz 491.52MHz	676 827	822 938	992 1060	mV
	LVDS Differential Output Voltage Swing, Peak-to-peak; 1474.56MHz; (see Table 54)	250mV amplitude	1474.56MHz 491.52MHz	256 324	386 438	546 580	mV
		500mV amplitude	1474.56MHz 491.52MHz	624 770	808 912	1024 1072	mV
		750mV amplitude	1474.56MHz 491.52MHz	980 1210	1230 1394	1514 1590	mV
		1000mV amplitude	1474.56MHz 491.52MHz	1352 1654	1644 1876	1984 2120	mV
$\Delta t_{PD}$	Propagation Delay Variation between Reference Input and any QCLK_y Output			-200		+200	ps

Table 51. AC Characteristics,  $V_{DD,V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ <sup>[a]</sup> <sup>[b]</sup> (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$t_{sk(o)}$	Output Skew; NOTE <sup>[i]</sup> , [ii], [k]	QCLK_y	Same N divider			100	ps
		QCLK_y	Any N divider, incident rising edge			100	ps
		QREF_r(clock)				100	ps
		QREF_r(SYSREF)			100	150	ps
		QREF_r(clock) to QCLK_y	Any divider, incident rising QCLK edge		100	150	ps
		QREF_r(SYSREF) to QCLK_y	Any divider, incident rising QCLK edge		100	150	ps
$\Delta\Phi$	Output Isolation between any Neighboring Clock Output	$f_{OUT} = 983.04MHz$			75		dB
		$f_{OUT} = 491.52MHz$		65	75		dB
		$f_{OUT} = 245.76MHz$		70	80		dB
$\Delta\Phi$	Output Isolation between any QCLK_y, QREF_r(SYSREF <sup>[ii]</sup> ) Output	Both SYSREF and clock signals active		50	75		dB
$t_{D, LOS}$	LOS State Detected (measured in input reference periods)	$f_{CLK} = 122.88MHz$ $f_{CLK} = 245.76MHz$				2 3	$T_{IN}$ $T_{IN}$
$t_{D, LOCK}$	PLL Lock Detect	PLL re-lock time after a short-term holdover scenario. Measured from LOS to both PLLs lock-detect asserted; hold-off timer = 200 (CNTR = $2^{17}$ , $f_{VCXO} = 122.88MHz$ , $f_{IN} = 245.76MHz$ or $122.88MHz$ ), VCXO-PLL bandwidth = 100Hz, initial frequency error <200 ppm.				300	ms
$t_{D, RES}$	PLL Lock Residual Time Error	Refer to PLL lock detect $t_{D, LOCK}$ . Reference point: final value of clock output phase after all phase transitions settled.				20	ns
$\Delta f_{HOLD}$	Holdover Accuracy	Maximum frequency deviation during a holdover duration of 200ms and after the clock re-validate event.		$\pm 0.5$		$\pm 5$	ppm

Table 51. AC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ <sup>[a]</sup> <sup>[b]</sup> (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$t_{D, RES-H}$	Holdover Residual Error		Measured 50ms after the reference clock re-appeared in a holdover scenario. Reference point: final value of clock output phase after all phase transitions settled.			$\pm 8.138$	ns
$t_H$	Hold Time	EXT_SYS to CLK_n <sup>[m]</sup>		2.5			ns
$t_S$	Setup Time	EXT_SYS to CLK_n <sup>[m]</sup>		0			ns
$t_W$	Pulse Width	EXT_SYS <sup>[m]</sup>		4			ns

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] VCXO-PLL bandwidth = 100Hz.

[c] Minimum input frequency for the loss the input reference detector is  $f_{VCO}/M_{V1}$  (maximum).

[d] RMS frequency error, measured at any QCLK\_y output, caused by Gaussian noise. Weighted with a 1ms low pass time window filter.

[e]  $V_{IL}$  should not be less than -0.3V and  $V_{IH}$  should not be greater than  $V_{DD\_V}$ .

[f] Common Mode Input Voltage is defined as the cross-point voltage.

[g] LVPECL outputs terminated with 50Ω to  $V_{DD\_V} - 1.5V$  (250mV amplitude setting),  $V_{DD\_V} - 1.75V$  (500mV amplitude setting),  $V_{DD\_V} - 2.0V$  (750mV amplitude setting),  $V_{DD\_V} - 2.25V$  (1000mV amplitude setting).

[h] LVDS outputs terminated 100Ω across terminals.

[i] This parameter is defined in accordance with JEDEC standard 65.

[j] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

[k] Align QCLK\_y to QREF\_r outputs according to [Recommended Delay Settings for Closest Clock-SYSREF Output Phase Alignment](#).

[l] SYSREF frequencies: 30.72MHz, 15.36MHz, 7.68MHz.

[m] SYSREF External trigger mode,  $BYPV = 0$ ,  $BYPF = 1$  (PLL feedback through  $M_{V0}$  and  $M_{V1}$ ),  $P_{V0} = \div 1024$ ,  $M_{V0} = \div 1024$ ,  $M_{V1} = \div 12$ ,  $N_S = \div 384$ ,  $SYNC = \div 12$ ,  $f_{IN} = 245.76MHz$  (see [Figure 8](#)).



Table 52. Clock Phase Noise Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  [a] [b] [c]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$j_{it}(\emptyset)$	Clock RMS Phase Jitter (Random), 983.04MHz		Integration Range: 1kHz–76.8MHz		64		fs
			Integration Range: 12kHz–20MHz		52	150	fs
$\Phi_N(10)$	Clock Single-side Band Phase Noise	1474.56MHz	10Hz offset		-61		dBc/Hz
$\Phi_N(100)$			100Hz offset		-92	-79	dBc/Hz
$\Phi_N(500)$			500Hz offset from carrier		-111	-105	dBc/Hz
$\Phi_N(1k)$			1kHz offset from carrier		-117	-110	dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-119	-117	dBc/Hz
$\Phi_N(60k)$			60kHz offset from carrier		-124	-117	dBc/Hz
$\Phi_N(100k)$			100kHz offset from carrier		-125	-120	dBc/Hz
$\Phi_N(200k)$			200kHz offset from carrier		-128	-123	dBc/Hz
$\Phi_N(800k)$			800kHz offset from carrier		-138	-135	dBc/Hz
$\Phi_N(5M)$			5MHz offset from carrier		-151	-147	dBc/Hz
$\Phi_N(\geq 10M)$			$\geq 10MHz$ offset from carrier and noise floor		-153	-150	dBc/Hz
$\Phi_N(10)$	Clock Single-side Band Phase Noise	983.04MHz	10Hz offset		-65	-47	dBc/Hz
$\Phi_N(100)$			100Hz offset		-95	-79	dBc/Hz
$\Phi_N(500)$			500Hz offset from carrier		-115	-100	dBc/Hz
$\Phi_N(1k)$			1kHz offset from carrier		-120	-106	dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-122	-117	dBc/Hz
$\Phi_N(60k)$			60kHz offset from carrier		-127	-117	dBc/Hz
$\Phi_N(100k)$			100kHz offset from carrier		-129	-120	dBc/Hz
$\Phi_N(200k)$			200kHz offset from carrier		-131	-123	dBc/Hz
$\Phi_N(800k)$			800kHz offset from carrier		-141	-138	dBc/Hz
$\Phi_N(5M)$			5MHz offset from carrier		-153	-147	dBc/Hz
$\Phi_N(\geq 10M)$			$\geq 10MHz$ offset from carrier and noise floor		-154	-150	dBc/Hz

Table 52. Clock Phase Noise Characteristics,  $V_{DD_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  [a] [b] [c] **(Cont.)**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$\Phi_N(10)$	Clock Single-side Band Phase Noise	491.52MHz	10Hz offset		-74	-53	dBc/Hz
$\Phi_N(100)$			100Hz offset		-103	-85	dBc/Hz
$\Phi_N(500)$			500Hz offset from carrier		-121	-106	dBc/Hz
$\Phi_N(1k)$			1kHz offset from carrier		-127	-112	dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-128	-123	dBc/Hz
$\Phi_N(60k)$			60kHz offset from carrier		-133	-123	dBc/Hz
$\Phi_N(100k)$			100kHz offset from carrier		-134	-126	dBc/Hz
$\Phi_N(200k)$			200kHz offset from carrier		-137	-129	dBc/Hz
$\Phi_N(800k)$			800kHz offset from carrier		-147	-144	dBc/Hz
$\Phi_N(5M)$			5MHz offset from carrier		-156	-150	dBc/Hz
$\Phi_N(\geq 10M)$			$\geq 10MHz$ offset from carrier and noise floor		-157	-153	dBc/Hz
$\Phi_N(10)$	Clock Single-side Band Phase Noise	245.76MHz	10Hz offset		-74	-59	dBc/Hz
$\Phi_N(100)$			100Hz offset		-109	-91	dBc/Hz
$\Phi_N(500)$			500Hz offset from carrier		-126	-112	dBc/Hz
$\Phi_N(1k)$			1kHz offset from carrier		-132	-118	dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-135	-129	dBc/Hz
$\Phi_N(60k)$			60kHz offset from carrier		-139	-129	dBc/Hz
$\Phi_N(100k)$			100kHz offset from carrier		-141	-134	dBc/Hz
$\Phi_N(200k)$			200kHz offset from carrier		-144	-135	dBc/Hz
$\Phi_N(800k)$			800kHz offset from carrier		-153	-150	dBc/Hz
$\Phi_N(5M)$			5MHz offset from carrier		-159	-153	dBc/Hz
$\Phi_N(\geq 10M)$			$\geq 10MHz$ offset from carrier and noise floor		-160	-153	dBc/Hz

Table 52. Clock Phase Noise Characteristics,  $V_{DD_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  [a] [b] [c] **(Cont.)**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$\Phi$	Spurious Signals (QCLK, QREF as clock)	983.04MHz	100Hz–300Hz		-80	-80	dBc
			300Hz–100kHz		-90	-83	dBc
			100kHz–100MHz		-92	-86	dBc
			122.88MHz reference spurious <sup>[d]</sup>		-80	-70	dBc
			245.76MHz reference spurious <sup>[e]</sup>		-80	-70	dBc
			491.52MHz reference spurious <sup>[f]</sup>		-75	-65	dBc
		491.52MHz	100Hz–300Hz		-88	-83	dBc
			300Hz–100kHz		-90	-89	dBc
			100kHz–100MHz		-100	-85	dBc
			122.88MHz reference spurious		-85	-70	dBc
			245.76MHz reference spurious		-85	-70	dBc
		245.76MHz	100Hz–300Hz		-92	-89	dBc
			300Hz–100kHz		-100	-95	dBc
			100kHz–100MHz		-102	-85	dBc
			122.88MHz reference spurious		-90	-70	dBc

[a] Phase noise and spurious specifications apply for device operation with QREF\_r outputs inactive (no SYSREF pulses generated).  
Phase noise specifications are applicable for all outputs active,  $N_x$  not equal.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Phase noise characteristics at lower frequency offsets (10Hz ~1kHz) is primarily a function of the VCXO phase noise: [VCXO characteristics: f = 122.88MHz; phase noise: -80dBc/Hz\(10Hz\), -113dBc/Hz\(100Hz\), -141dBc/Hz\(1kHz\), -157dBc/Hz\(10kHz\), -160dBc/Hz\(100kHz\)](#); [Input frequency: 245.76MHz](#).

[d] Measured at all offset frequencies except at  $f_{\text{OFFSET}} = 122.88\text{MHz}$ .

[e] Measured at all offset frequencies except at  $f_{\text{OFFSET}} = 245.76\text{MHz}$ .

[f] Measured at all offset frequencies except at  $f_{\text{OFFSET}} = 491.52\text{MHz}$ .

Table 53. SYSREF Phase Noise Characteristics,  $V_{DD_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  [a] [b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$\Phi_N(500)$	SYSREF Single-side Band Phase Noise	30.72MHz	500Hz offset		-133	-130	dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-146	-130	dBc/Hz
$\Phi_N(60k)$			60kHz offset from carrier		-150	-140	dBc/Hz
$\Phi_N(800k)$			800kHz offset from carrier		-154	-145	dBc/Hz
$\Phi_N(\geq 3M)$			$\geq 3MHz$ offset from carrier and noise floor		-154	-145	dBc/Hz
$\Phi_N(500)$	SYSREF Single-side Band Phase Noise	15.36MHz	500Hz offset		-130	-130	dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-146	-130	dBc/Hz
$\Phi_N(60k)$			60kHz offset from carrier		-152	-140	dBc/Hz
$\Phi_N(800k)$			800kHz offset from carrier		-155	-145	dBc/Hz
$\Phi_N(\geq 3M)$			$\geq 3MHz$ offset from carrier and noise floor		-155	-145	dBc/Hz
$\Phi_N(500)$	SYSREF Single-side Band Phase Noise	7.68MHz	500Hz offset		-133		dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-146		dBc/Hz
$\Phi_N(60k)$			60kHz offset from carrier		-156		dBc/Hz
$\Phi_N(800k)$			800kHz offset from carrier		-160		dBc/Hz
$\Phi_N(\geq 3M)$			$\geq 3MHz$ offset from carrier and noise floor				dBc/Hz
$\Phi$	Spurious Signals <sup>[c]</sup>	30.72MHz	>500Hz		-60	-56	dBc
		15.36MHz	>500Hz		-60	-56	dBc
		7.68MHz	>500Hz		-60	-56	dBc

[a] Phase noise is measured as additive phase noise contribution by the device on all SYSREF outputs, dividers and channel logic. SYSREF signals measured as continued clock signal. Clock signals (QCLK) are turned on.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Measured as sum of all spurious amplitudes in one side band in the offset frequency range above 500Hz, excluding the harmonics of the fundamental frequency of  $n \times f_{SYSREF}$  (e.g.  $n \times 7.68MHz$ ).

Table 54. 8V19N490AC Characteristics: Typical QCLK\_y Output Amplitude,  $V_{DD\_V} = 3.3V$ ,  $T_A = 85^{\circ}C$ <sup>[a]</sup>

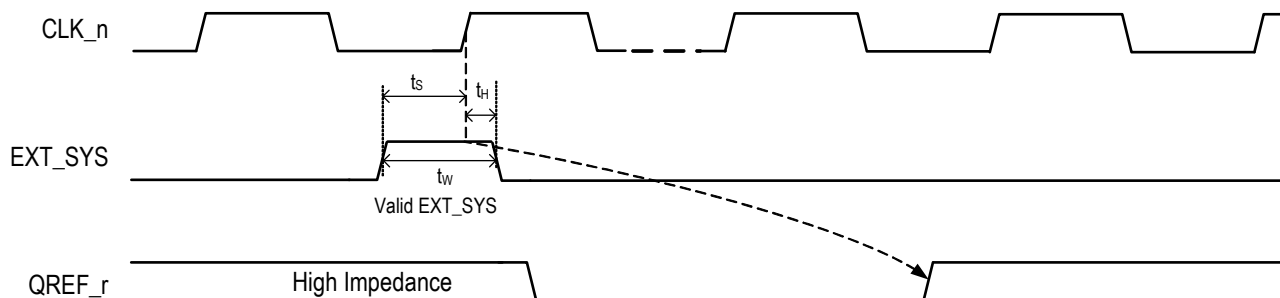
Symbol	Parameter	Test Conditions	QCLK_y Output Frequency in MHz						Units
			2949.12	1474.56	983.04	737.28	491.52	245.76	
$V_{O(PP)}$ <sup>[b]</sup>	LVPECL Output Voltage Swing, Peak-to-peak	250mV amplitude setting	214	283	260	262	264	281	mV
		500mV amplitude setting	376	520	492	484	508	520	mV
		750mV amplitude setting	512	748	740	716	730	768	mV
		1000mV amplitude setting	628	960	984	944	968	1008	mV
$V_{OD}$ <sup>[c]</sup>	LVDS Output Voltage Swing, Peak-to-peak	250mV amplitude setting	120	190	200	210	215	225	mV
		500mV amplitude setting	250	390	410	430	440	470	mV
		750mV amplitude setting	370	592	650	670	682	710	mV
		1000mV amplitude setting	475	790	870	900	920	980	mV

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL outputs terminated with  $50\Omega$  to  $V_{DD\_V} - 1.5V$  (250mV amplitude setting),  $V_{DD\_V} - 1.75V$  (500mV amplitude setting),  $V_{DD\_V} - 2.0V$  (750mV amplitude setting),  $V_{DD\_V} - 2.25V$  (1000mV amplitude setting).

[c] LVDS outputs terminated  $100\Omega$  across terminals.

Figure 8. EXT\_SYS Input Timing Diagram



## Clock Phase Noise Characteristics

Measurement conditions for phase noise characteristics:

- VCXO characteristics:  $f = 122.88MHz$ ; phase noise:  $-80dBc/Hz(10Hz)$ ,  $-113dBc/Hz(100Hz)$ ,  $-141dBc/Hz(1kHz)$ ,  $-157dBc/Hz(10kHz)$ ,  $-160dBc/Hz(100kHz)$ ; Input frequency:  $245.76MHz$
- $I_{CPV}$  VCXO-PLL charge pump current:  $0.2mA$
- VCXO-PLL bandwidth:  $6Hz$
- $I_{CPF}$  FemtoClock NG charge pump current:  $1.6mA$
- FemtoClock NG PLL bandwidth:  $127kHz$
- $V_{DD\_V} = 3.3V$ ,  $T_A = 25^{\circ}C$

Figure 9. 1474.56MHz Output Phase Noise

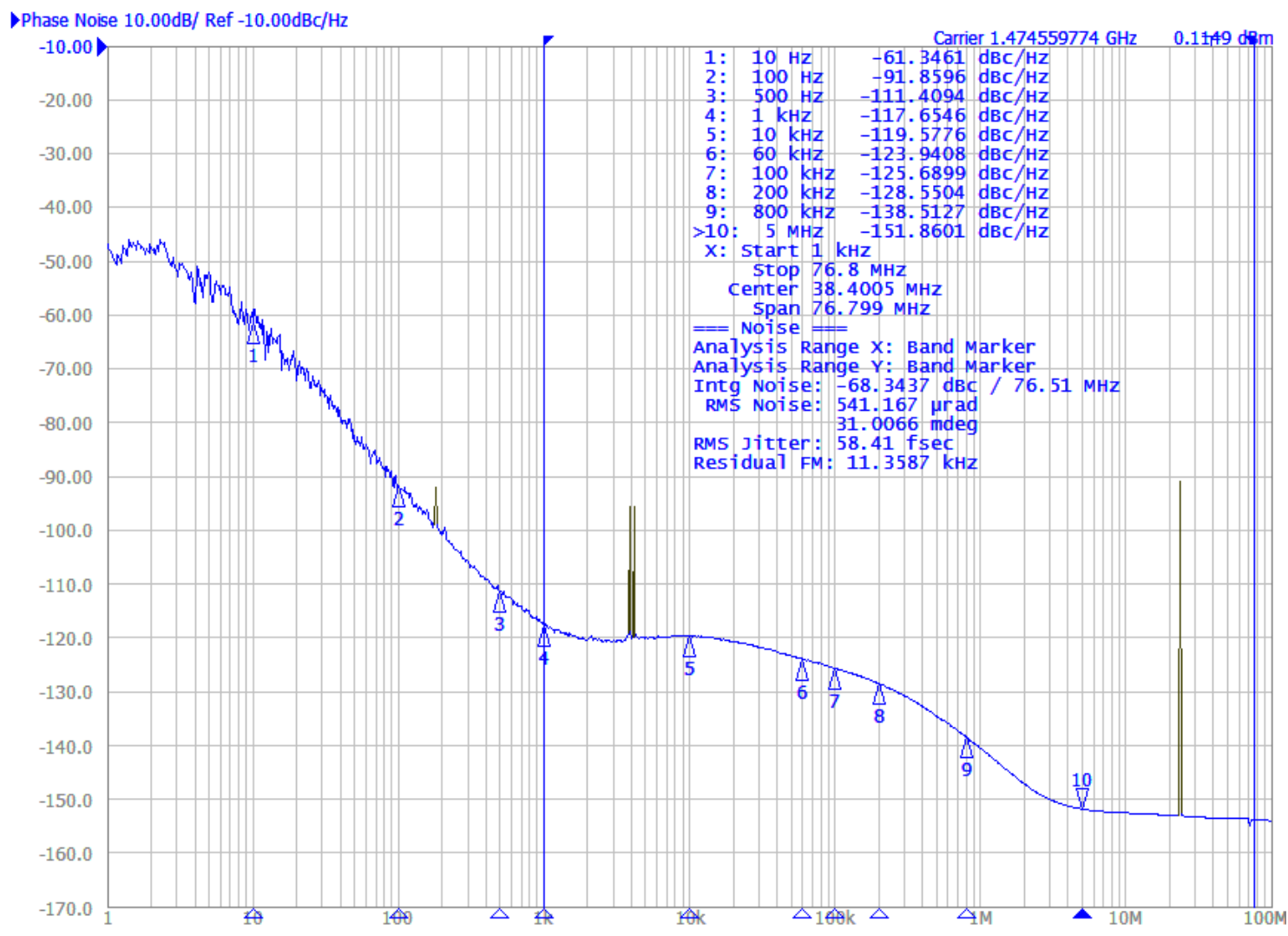


Figure 10. 983.04MHz Output Phase Noise

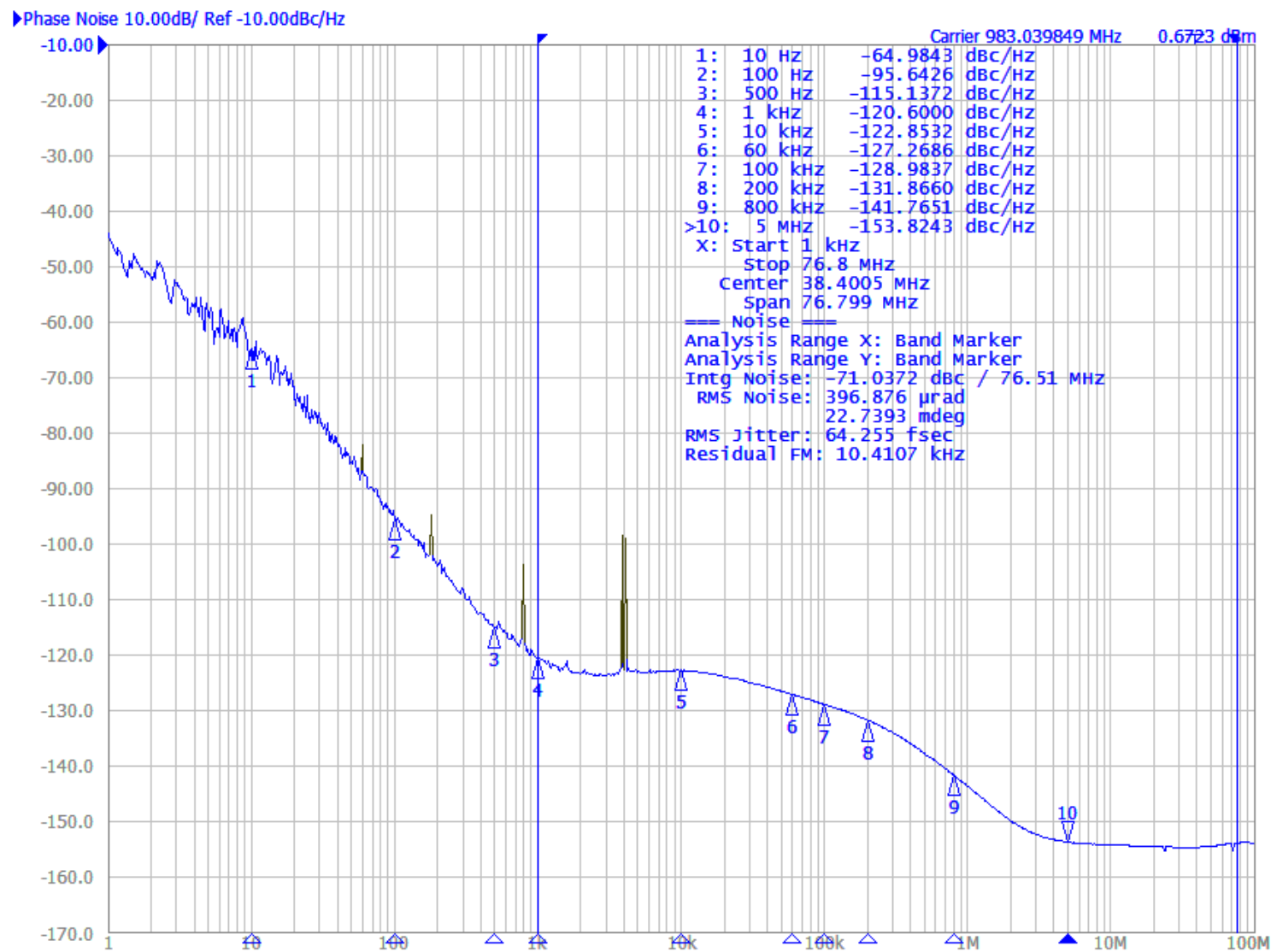


Figure 11. 491.52MHz Output Phase Noise

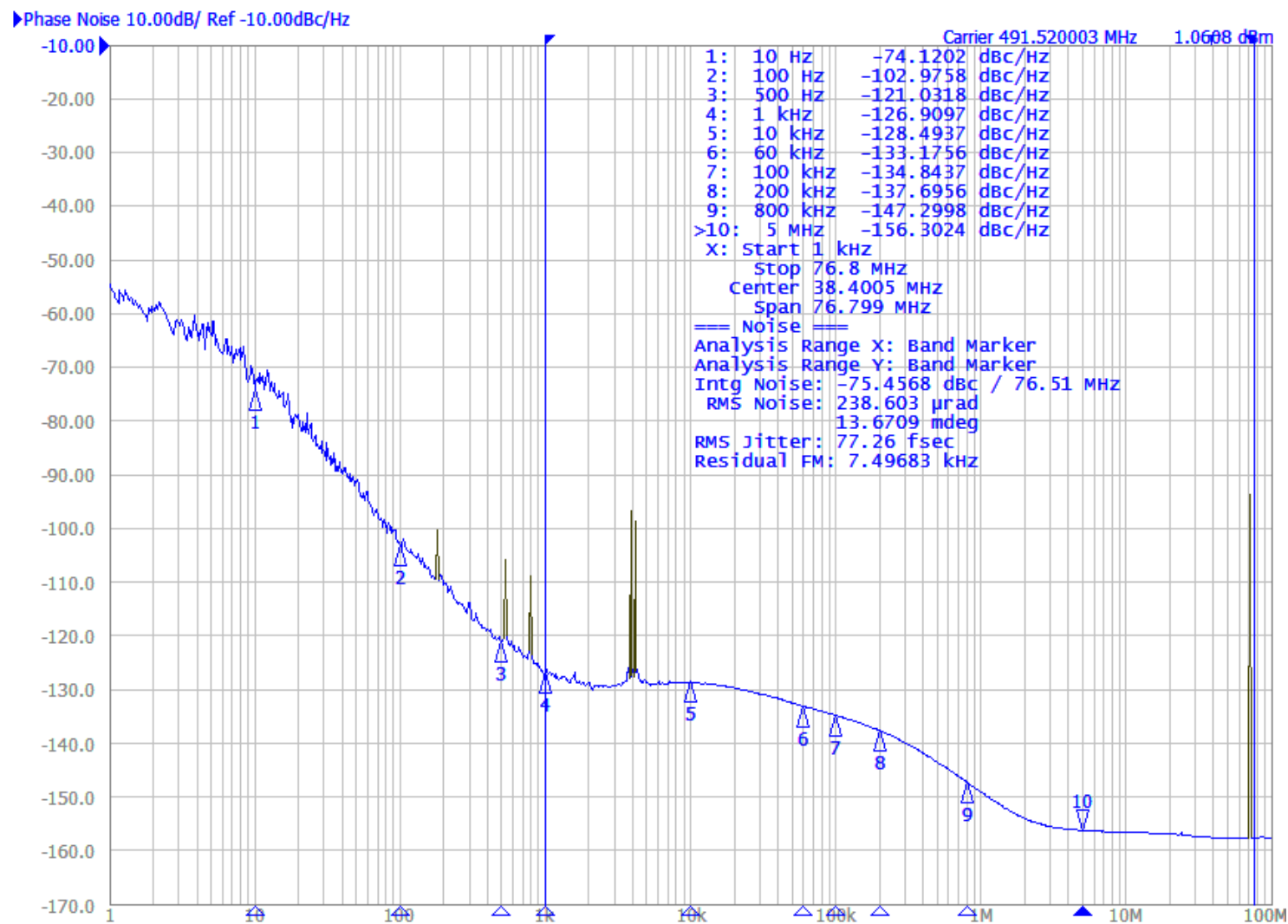
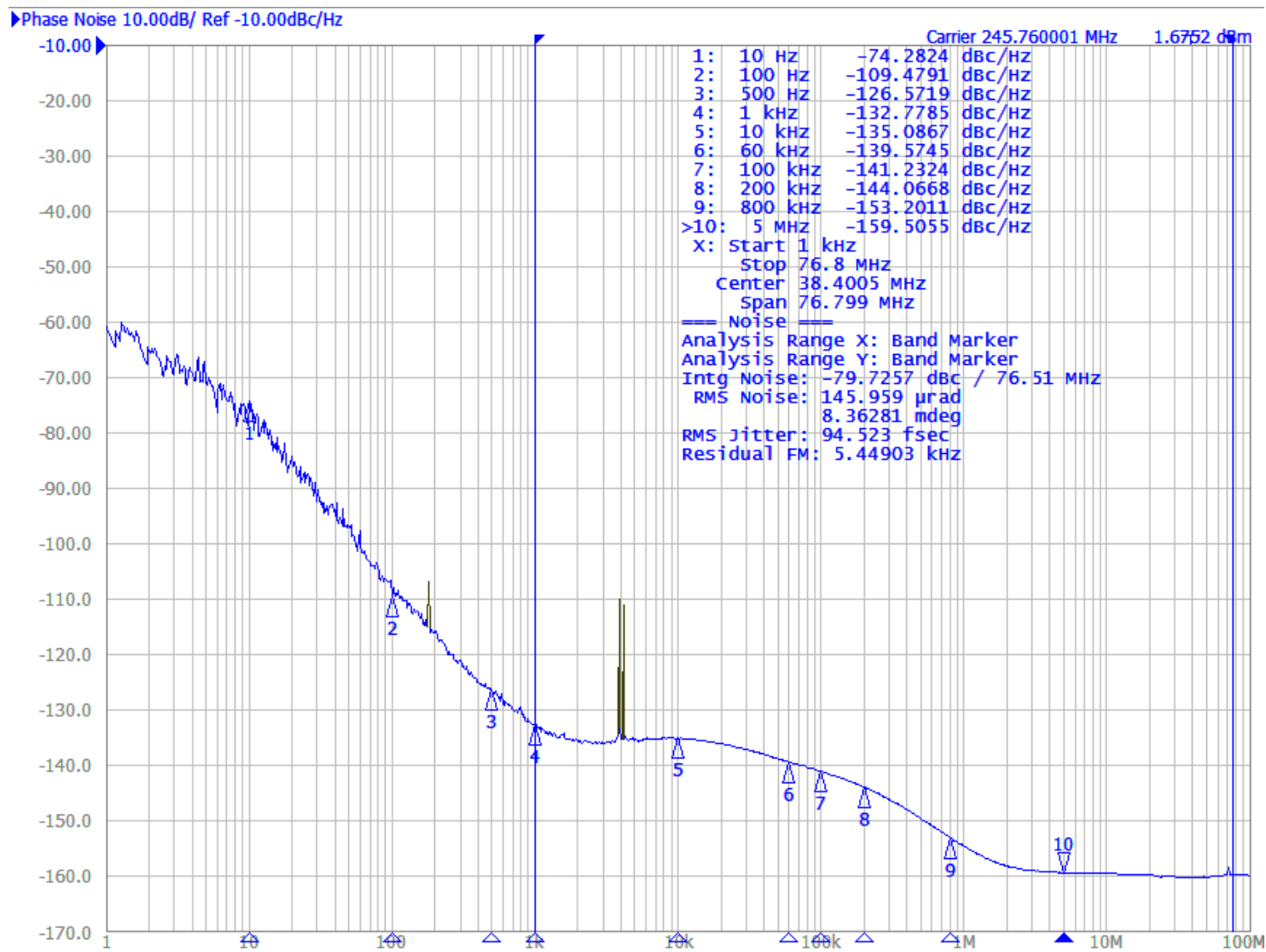




Figure 12. 245.76MHz Output Phase Noise



## Application Information

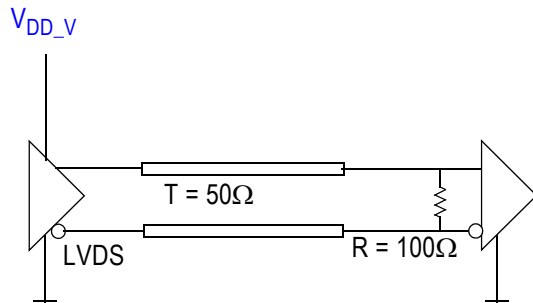
### Power Supply Design and Recommend Application Schematics

Careful power supply and board design is required for best possible AC performance including phase noise and spurious suppression. The analog power supply pins VDD\_OSC, VDD\_CP, VDD\_CPF, VDD\_LCF and VDD\_LCV require a very clean power supply isolated from the output power supply (VDD\_QCLK\_y and VDD\_QREF\_r). Output power supplies should be isolated from each other. The VDD\_LCF power supply pin must be supplied by a low-noise LDO with a noise voltage of  $<6\mu\text{V}$  or lower. Please refer to the *8V19N490 Hardware Design Guide* for information about power supply and isolation, loop filter design for VCXO and VCO, schematics, input and output interfaces/terminations and an example schematics.

### Termination for QCLK\_y, QREF\_r LVDS Outputs (STYLE = 0)

Figure 13 shows an example termination for the QCLK\_y, QREF\_r LVDS outputs. In this example, the characteristic transmission line impedance is  $50\Omega$ . The termination resistor R ( $100\Omega$ ) is matched to the line impedance. The termination resistor must be placed at the end of the transmission line. No external termination resistor is required if R is an internal part of the receiver circuit. The LVDS termination in Figure 13 is applicable for any output amplitude setting specified in Table 15.

Figure 13. LVDS (SYLE = 0) Output Termination



### AC Termination for QCLK\_y, QREF\_r LVDS Outputs (STYLE = 0)

Figure 14 and Figure 15 show AC termination examples for the QCLK\_y, QREF\_r LVDS outputs. In the examples, the characteristic transmission line impedance is  $50\Omega$ . In Figure 14, the termination resistor R ( $100\Omega$ ) is placed at the end of the transmission line. No external termination resistor is required if R is an internal part of the receiver circuit, which is shown in Figure 13. The LVDS terminations in both Figure 14 and Figure 15 are applicable for any output amplitude setting specified in Table 15. The receiver input should be re-biased according to its common mode range specifications.

Figure 14. LVDS (SYLE = 0) AC Output Termination

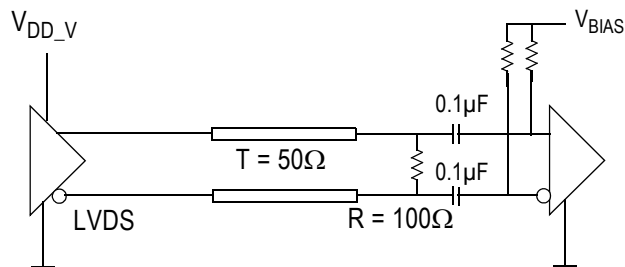
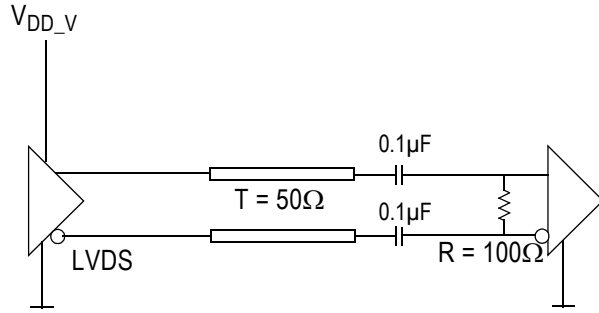


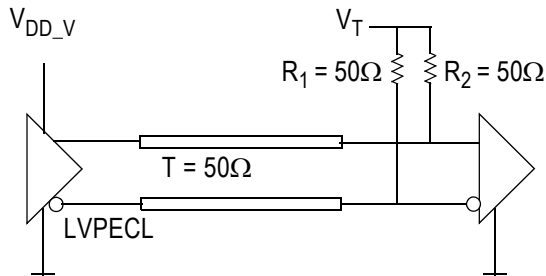
Figure 15. LVDS (STYLE = 0) AC Output Termination



### Termination for QCLK\_y, QREF\_r LVPECL Outputs (STYLE = 1)

Figure 16 shows an example termination for the QCLK\_y, QREF\_r LVPECL outputs. In this example, the characteristic transmission line impedance is  $50\Omega$ . The R1 ( $50\Omega$ ) and R2 ( $50\Omega$ ) resistors are matched load terminations. The output is terminated to the termination voltage  $V_T$ . The  $V_T$  must be set according to the output amplitude setting defined in Table 15. The termination resistors must be placed close to the end of the transmission line.

Figure 16. LVPECL (STYLE = 1) Output Termination



$$V_T = V_{DD\_V} - 1.50V \text{ (250mV Amplitude)}$$

$$V_T = V_{DD\_V} - 1.75V \text{ (500mV Amplitude)}$$

$$V_T = V_{DD\_V} - 2.00V \text{ (750mV Amplitude)}$$

$$V_T = V_{DD\_V} - 2.25V \text{ (1000mV Amplitude)}$$

# Thermal Characteristics

Table 55. Thermal Characteristics for the 100 CABGA package<sup>[a]</sup>

Multi-Layer PCB, JEDEC Standard Test Board				
Symbol	Thermal Parameter	Condition	Value	Unit
$\Theta_{JA}$	Junction-to-ambient	0 m/s air flow	24.06	°C/W
		1 m/s air flow	20.89	
		2 m/s air flow	19.07	
		3 m/s air flow	18.05	
		4 m/s air flow	17.46	
		5 m/s air flow	17.03	
$\Theta_{JC}$	Junction-to-case	—	8.54	
$\Theta_{JB}$	Junction-to-board <sup>[b]</sup>	—	6.43	
$\Psi_{JB}$	Junction-to-board <sup>[c]</sup>	—	4.15	

[a] Standard JEDEC 2S2P multilayer PCB.

[b] Thermal model where the heat dissipated in the component is conducted through the board.  $T_B$  is measured on or near the component lead.

[c] Thermal model where the majority of the heat dissipates through the board and a minority through the top of the package.  $T_B$  is measured on or near the component lead.

## Temperature Considerations

The device supports applications in a natural convection environment as long as the junction temperature does not exceed the specified junction temperature  $T_J$ . In applications where the heat dissipates through the PCB,  $\Theta_{JB}$  is the correct metric to calculate the junction temperature.  $\Psi_{JB}$  is the right metric in all other applications where the majority of the heat dissipates through the board (80%) and a minority (20%) through the top of the device. The following calculation uses the junction-to-board thermal characterization parameter  $\Theta_{JB}$  to calculate the junction temperature ( $T_J$ ). Care must be taken to not exceed the maximum allowed junction temperature  $T_J$  of 125 °C.

The junction temperature  $T_J$  is calculated using the following equation:  $T_J = T_B + P_{TOT} \times \Psi_{JB}$

where:

- $T_J$  is the junction temperature at steady state conditions in °C
- $T_B$  is the board temperature at steady state condition in °C, measured on or near the component lead
- $\Psi_{JB}$  is the thermal characterization parameter to report the difference between  $T_J$  and  $T_B$
- $P_{TOT}$  is the total device power dissipation

**The 8V19N490 maximum power dissipation scenario:** With the maximum allowed junction temperature and the maximum device power consumption and at the maximum supply voltage of 3.3V + 5%, the maximum supported board temperature can be determined. In the device configuration for the maximum power consumption,  $I_{DD\_V}$  is 1395mA (see [Table 45](#)). In this configuration, all outputs are active and configured to LVDS, the output amplitude is set to 1000mV (QOSC: 750,V amplitude) and outputs use a 100Ω termination:

- Total system power dissipation (including termination resistor power):  $P_{TOT} = V_{DD\_V, MAX} \times I_{DD\_V, MAX} = 3.465V \times 1395mA = 4.8336W$
- Total device power dissipation (excluding termination resistor power):  $P_{TOT} = 4.8336W$

In this scenario and with the  $\Psi_{JB}$  thermal model, the maximum supported board temperature is:

- $T_{B, MAX} = T_{J, MAX} - \Psi_{JB} \times P_{TOT}$
- $T_{B, MAX} = 125°C - 6.43°C/W \times 4.8336W$
- $T_{B, MAX} = 93.9°C$ .

Application using the device at the maximum power dissipation must keep the board temperature below 93.9°C. **Application power dissipation scenarios:** Applications may use device settings that result in a lower power dissipation than the maximum power scenario. The device is a multi-functional, high-speed device that targets a variety of applications. Since this device is highly programmable with a broad range of settings and configurations, the power consumption will vary as settings and configurations are changed. Table 45 shows the typical current consumption and total device power consumption along with the junction temperature for the 6 test cases shown in Table 46. The table also displays the maximum board temperature for the  $\Theta_{JB}$  model.

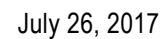
Table 56. Typical Device Power Dissipation and Junction Temperature

Test Case <sup>[a]</sup>	Output Configuration	Device		$\Theta_{JB}$ Thermal Model	
		$I_{DD\_TOT}$	$P_{TOT}$	$T_J^{[b]}$	$T_{B\_MAX}^{[c]}$
		mA	W	°C	°C
1	QCLK: LVPECL, 500mV QREF: LVDS, 500mV	984.1	2.76	102.8	107.2
2	QCLK: LVPECL, 750mV QREF: LVDS, 500mV	1036.7	2.87	103.5	106.5
3	QCLK: LVPECL, 1000mV QREF: LVDS (off)	802.7	2.06	98.3	111.7
4	QCLK: LVPECL, 250mV QREF: LVDS, 250mV	873.4 844.2	2.46	100.8	109.2
5	QCLK: LVDS, 500mV QREF: LVDS (off)	614.3	2.03	98.0	112.0
6	QCLK: LVDS, 750mV QREF: LVDS (off)	696.6	2.3	99.8	110.2

[a] For device settings (see Table 46).

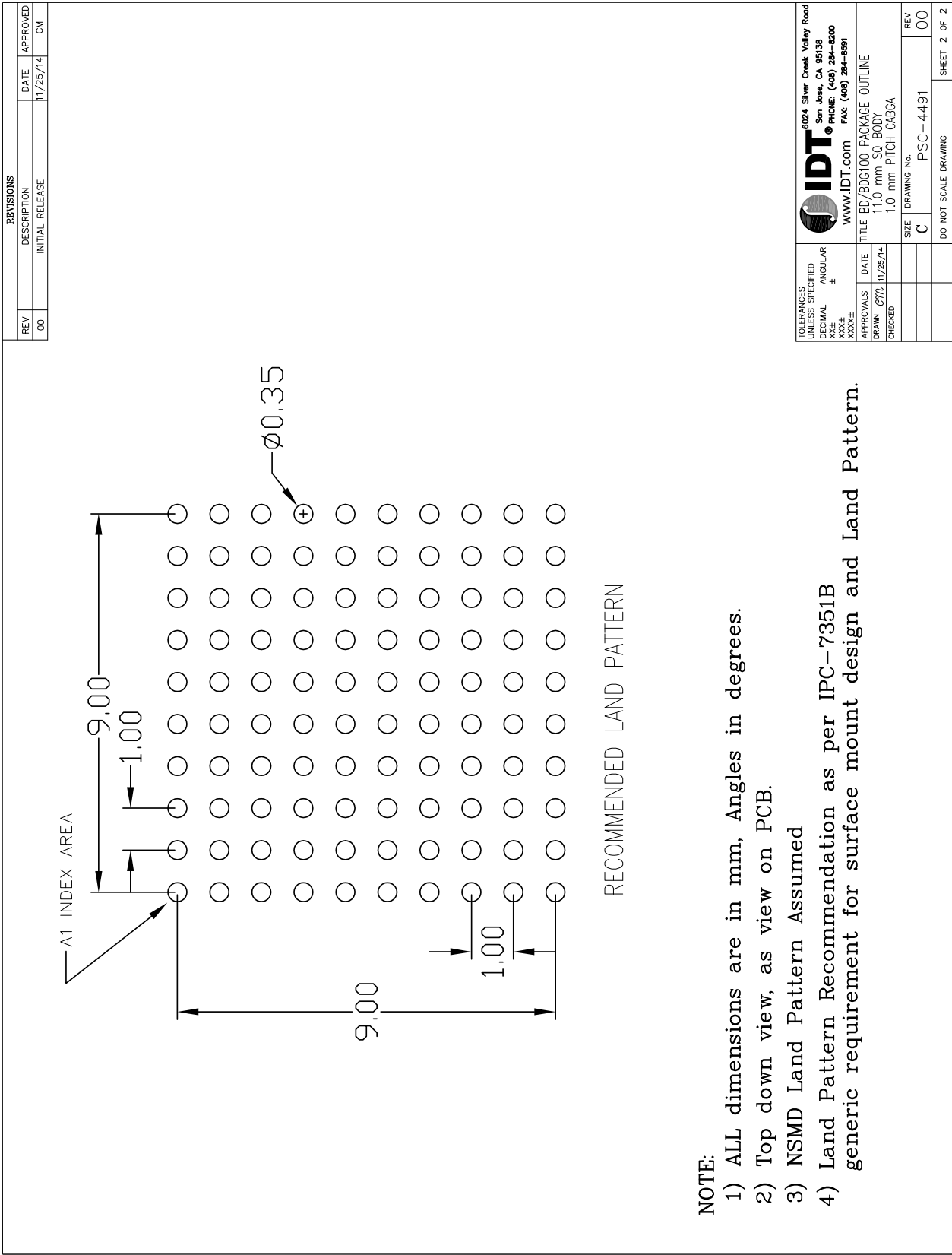
[b] Junction temperature at board temperature  $T_B = 85^\circ\text{C}$ .

[c] Maximum board temperature for junction temperature  $<125^\circ\text{C}$ .



Recommended Land Pattern

Figure 18. Recommended Land Pattern



## Marking Diagram

Figure 19. Marking Diagram



1. Line 1 indicates the part number.
2. Line 2 indicates the part number suffix
2. Line 3:
  - “YYWW” is the last digit of the year and week that the part was assembled.
  - #: denotes sequential lot number.
  - \$: denotes mark code.

## Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V19N490BDGI	IDT8V19N490BDGI	11 × 11 × 1.2 mm 100-CABGA	Tray	-40°C to +85°C
8V19N490BDGI8	IDT8V19N490BDGI		Tape & Reel	

## Revision History

Revision Date	Description of Change
July 26, 2017	Changed the definition of nBIAS_r in <a href="#">Table 18</a> Updated the definition of 0x76 in <a href="#">Table 29</a> Updated V <sub>DIFF_IN</sub> in <a href="#">Table 51</a>
June 6, 2017	Updated the description of 0x1D–0x1F in <a href="#">Table 26</a> .
April 24, 2017	<a href="#">Table 52</a> , swapped t <sub>jit</sub> (Ø) typical specs.
April 3, 2017	Initial release.



## Glossary

Abbreviation	Description
Index $n$	Denominates a clock input CLK_ $n$ . Range: 0 to 3.
Index $x$	Denominates a channel, channel frequency divider and the associated configuration bits. Range: A, B, C, D, E.
Index $y$	Denominates a QCLK output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1, D, E0, E1.
Index $r$	Denominates a QREF output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1, D.
$V_{DD\_V}$	Denominates voltage supply pins. Range: VDD_QCLKA, VDD_QREFA, VDD_QCLKB, VDD_QREFB, VDD_QCLKC, VDD_QREFC, VDD_QCLKD, VDD_QREFD, VDD_QCLKE, VDD_SPI, VDD_INP, VDD_LCV, VDD_LCF, VDD_CP, VDD_SYNC, VDD_CPF, VDD_OSC.
status_condition	Status conditions are: LOLV (Loss of VCXO-PLL lock), LOLF (Loss of FemtoClock NG-PLL lock) and LOS (Loss of input signal).
[...]	Index brackets describe a group associated with a logical function or a bank of outputs.
{...}	List of discrete values.
Suffix V	Denominates a function associated with the VCXO-PLL.
Suffix F	Denominates a function associated with the 2nd stage PLL (FemtoClock NG).

## IMPORTANT NOTICE AND DISCLAIMER

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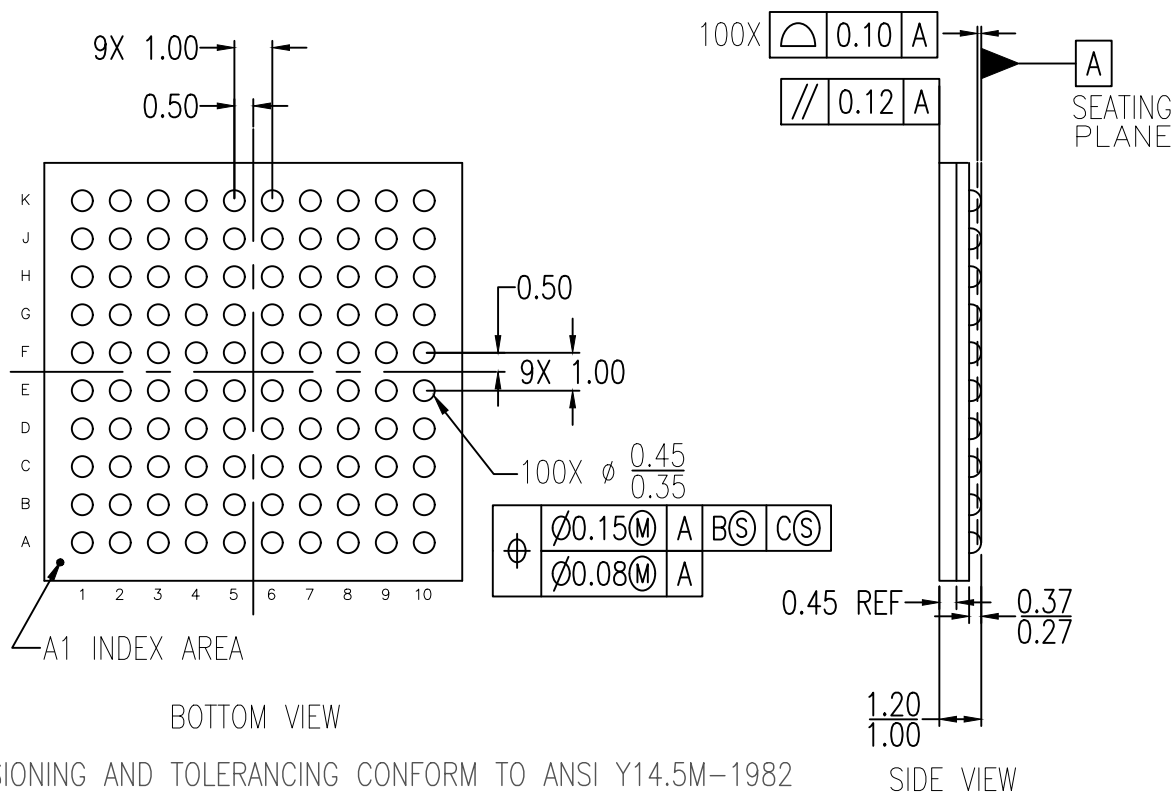
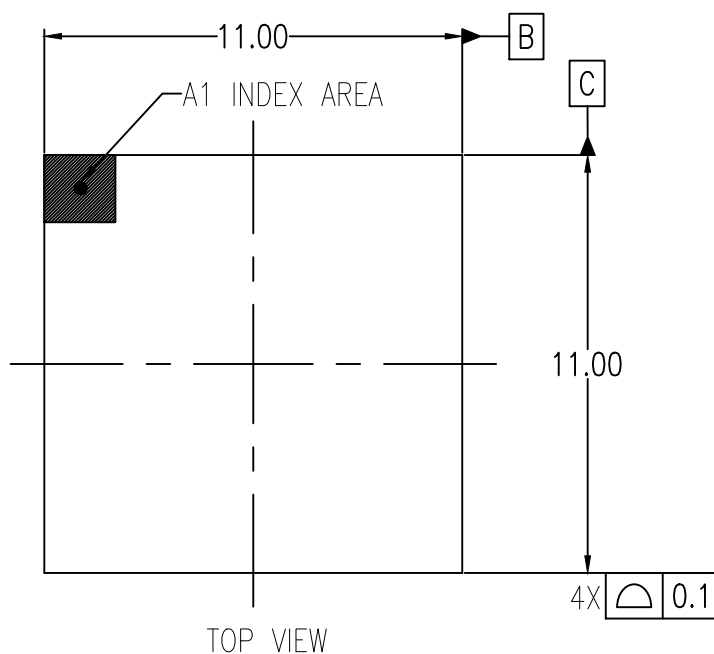
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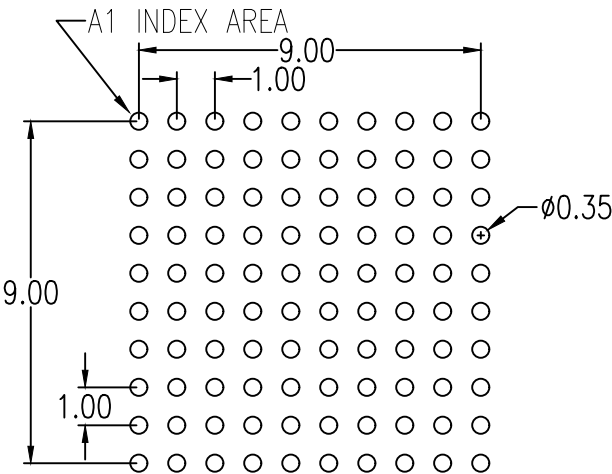
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NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982  
2. ALL DIMENSION ARE IN MILLIMETERS



RECOMMENDED LAND PATTERN DIMENSION

- NOTES:
- 1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES
  - 2. TOP DOWN VIEW ON PCB
  - 3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 23, 2018	Rev 00	Initial Release