

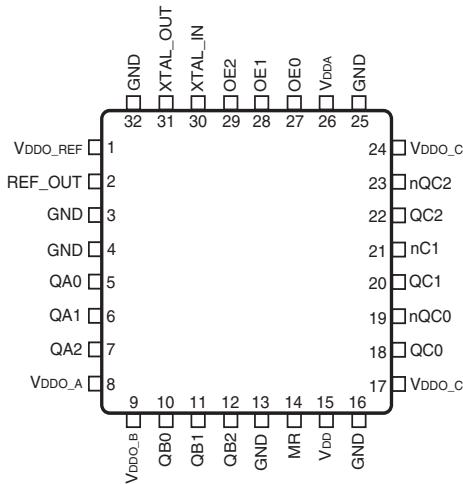
General Description

8402015 is a low phase noise Clock Synthesizer and is a member of the high performance clock solutions from IDT. The device provides three banks of outputs and a reference clock. Each bank can be enabled by using output enable pins. A 25MHz or 50MHz, 18pF parallel resonant crystal is used to generate 25MHz LVCMOS, 125MHz LVCMOS and 125MHz LVDS outputs. 8402015 is packaged in a small, 32-pin VFQFN package that is optimum for applications with space limitations.

Features

- Three banks of outputs:
 - Bank A: three single-ended LVCMOS/LVTTL outputs at 25MHz or 50MHz
 - Bank B: three single-ended LVCMOS/LVTTL outputs at 125MHz
 - Bank C: three differential LVDS outputs at 125MHz
 - Reference LVCMOS/LVTTL output at 25MHz
- Crystal input frequency: 25MHz
- Maximum output frequency: 125MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (637kHz - 62.5MHz): 0.373ps (typical) LVDS output
- RMS phase jitter @ 25MHz, using a 25MHz crystal (12kHz - 1MHz): 0.64ps (typical) LVCMOS output
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



8402015

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Block Diagram

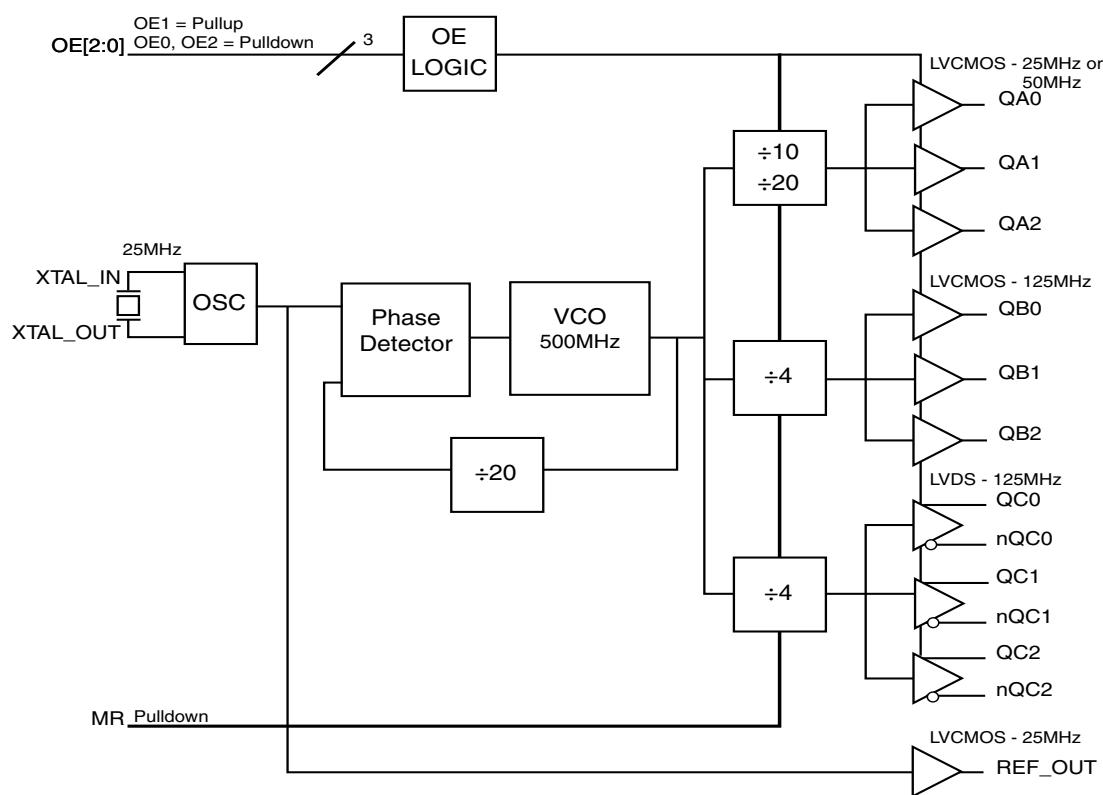


Table 1. Pin Descriptions

Number	Name	Type	Description			
1	V _{DDO_REF}	Power	Output supply pin for REF_OUT output.			
2	REF_OUT	Output	Reference clock output. LVCMOS/LVTTL interface levels.			
3, 4, 13, 16, 25, 32	GND	Power	Power supply ground.			
5, 6, 7	QA0, QA1, QA2	Output	Single-ended Bank A clock outputs. LVCMOS/LVTTL interface levels.			
8	V _{DDO_A}	Power	Power output supply pin for Bank A LVCMOS outputs.			
9	V _{DDO_B}	Power	Power output supply pin for Bank B LVCMOS outputs.			
10, 11, 12	QB0, QB1, QB2	Output	Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels.			
14	MR	Input	Pulldown	Master reset, resets the internal dividers. During reset, LVCMOS outputs are pulled LOW, and LVDS outputs are pulled LOW and HIGH (QCx pulled LOW, nQCx pulled HIGH). LVCMOS/LVTTL interface levels.		
15	V _{DD}	Power	Core supply pin.			
17, 24	V _{DDO_C}	Power	Power output supply pin for Bank C LVDS outputs.			
18, 19	QC0, nQC0	Output	Differential Bank C clock outputs. LVDS interface levels.			
20, 21	QC1, nQC1	Output	Differential Bank C clock outputs. LVDS interface levels.			
22, 23	QC2, nQC2	Output	Differential Bank C clock outputs. LVDS interface levels.			
26	V _{DDA}	Power	Analog supply pin.			
27, 29	OE0, OE2	Input	Pulldown	Output enable and configuration pins. See Table 3. LVCMOS/LVTTL interface levels.		
28	OE1	Input	Pullup	Output enable and configuration pin. See Table 3. LVCMOS/LVTTL interface levels.		
30, 31	XTAL_IN, XTAL_OUT	Input	Crystal oscillator interface. XTAL_OUT is the output, XTAL_IN is the input.			

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance				4		pF
C _{PD}	Power Dissipation Capacitance (per output)		V _{DD} , V _{DDO_A} , V _{DDO_B} , V _{DDO_C} = 3.465V		15		pF
R _{PULLUP}	Input Pullup Resistor				51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor				51		kΩ
R _{OUT}	Output Impedance	QA[0:2], QB[0:2], REF_OUT			20		Ω

Function Table

Table 3. OE Function and ConfigurationTable

Inputs			Output Frequency (MHz)								
OE2	OE1	OE0	Bank A			Bank B			Bank C		
			A0	A1	A2	B0	B1	B2	C0	C1	C2
0	0	0	25	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	125	Hi-Z	Hi-Z
0	0	1	25	Hi-Z	Hi-Z	125	Hi-Z	Hi-Z	125	Hi-Z	Hi-Z
0*	1*	0*	25	25	Hi-Z	Hi-Z	Hi-Z	Hi-Z	125	125	Hi-Z
0	1	1	25	25	25	125	125	125	125	125	125
1	0	0	50	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	125	Hi-Z	Hi-Z
1	0	1	25	25	Hi-Z	125	125	Hi-Z	125	125	Hi-Z
1	1	0	50	50	Hi-Z	Hi-Z	Hi-Z	Hi-Z	125	125	Hi-Z
1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

*Default

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, I_O (LVC MOS)	-0.5V to $V_{DD_LVC MOS} + 0.5V$
Outputs, I_O (LVDS) Continuos Current Surge Current	10mA 15mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO_A} = V_{DDO_B} = V_{DDO_C} = V_{DDO_REF} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - 0.36$	3.3	V_{DD}	V
V_{DDO_A} , V_{DDO_B} , V_{DDO_C} , V_{DDO_REF}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				30	mA
I_{DDA}	Analog Supply Current				36	mA
I_{DDO_A} , I_{DDO_B} , I_{DDO_C} , I_{DDO_REF}	Total Output Supply Current	Outputs Unused			26	mA

Table 4C. LVC MOS/LV TTL DC Characteristics, $V_{DD} = V_{DDO_A} = V_{DDO_B} = V_{DDO_REF} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE1	$V_{DD} = V_{IN} = 3.465V$			5	μA
		OE0, OE2, MR	$V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	OE1	$V_{DD} = 3.465V$	-150			μA
		OE0, OE2, MR	$V_{DD} = 3.465V$	-5			μA
V_{OH}	Output High Voltage	QA0:QA2, QB0:QB2, REF_OUT	$V_{DDO_REF} = 3.3V \pm 5\%$, $I_{OH} = -12mA$	2.6			V
V_{OL}	Output Low Voltage	QA0:QA2, QB0:QB2, REF_OUT	$V_{DDO_REF} = 3.3V \pm 5\%$, $I_{OL} = 12mA$			0.5	V

Table 4D. LVDS DC Characteristics, $V_{DD} = V_{DDO_C} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			300	450	575	mV
ΔV_{OD}	V_{OD} Magnitude Change					50	mV
V_{OS}	Offset Voltage			1.325	1.4	1.575	V
ΔV_{OS}	V_{OS} Magnitude Change					50	mV
I_{Oz}	High Impedance Leakage			-10		+10	μA
I_{OFF}	Power Off Leakage			-20		+20	μA
I_{OSD}	Differential Output Short Circuit Current				-3.5	-5	mA
I_{OS}	Output Short Circuit Current				-3.5	-5	mA

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance				50	Ω
Shunt Capacitance				7	pF

Table 6. AC Characteristics, $V_{DD} = V_{DDO_A} = V_{DDO_B} = V_{DDO_C} = V_{DDO_REF} = 3.3V \pm 5\%$, $T_A = -40^{\circ}\text{C}$ to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{out}	Output Frequency	QA[0:2]			25		MHz
		QA[0:1]			50		MHz
		QB[0:2]			125		MHz
		QC[0:2]/ nQC[0:2]			125		MHz
		REF_OUT			25		MHz
$\delta_{j\text{it}}(\emptyset)$	RMS Phase Noise Jitter; NOTE 1	QA0:QA2, REF_OUT	25MHz, Integration Range: 12kHz - 1MHz		0.642		ps
		QB0:QB2	125MHz, Integration Range: 637kHz - 62.5MHz		0.389		ps
		QC0:QC2	125MHz, Integration Range: 637kHz - 62.5MHz		0.373		ps
$t_{sk(b)}$	Bank Skew; NOTE 2, 3	QA[0:2], QB[0:2]				45	ps
		QC[0:2]/nQC[0:2]				35	ps
t_R / t_F	Output Rise/Fall Time	QA[0:2], QB[0:2], REF_OUT	20% to 80%	0.425		1.15	ns
		QC[0:2]/ nQC[0:2]	20% to 80%	145		415	ps
odc	Output Duty Cycle	QA[0:2], QB[0:2], REF_OUT		48		52	%
		QC[0:2]/ nQC[0:2]		48		52	%

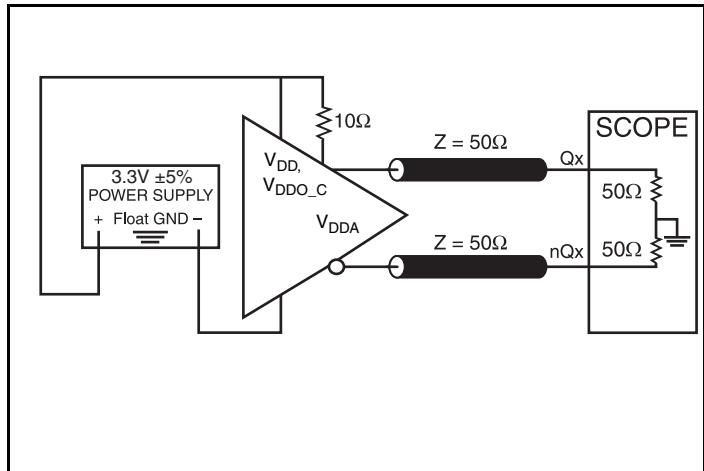
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 Ifpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Please refer to Phase Noise Plots.

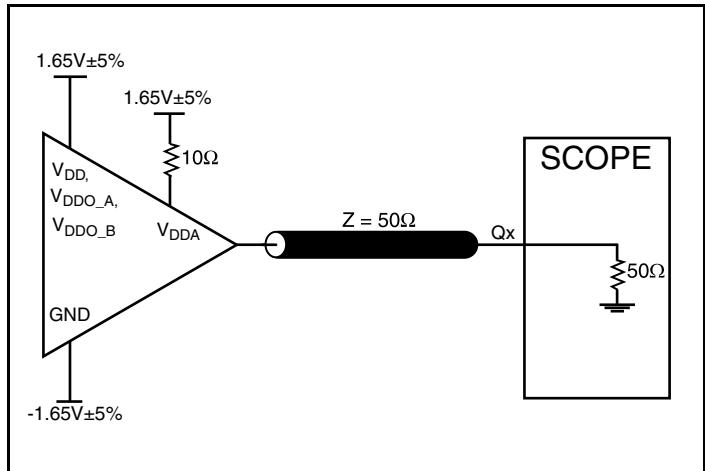
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

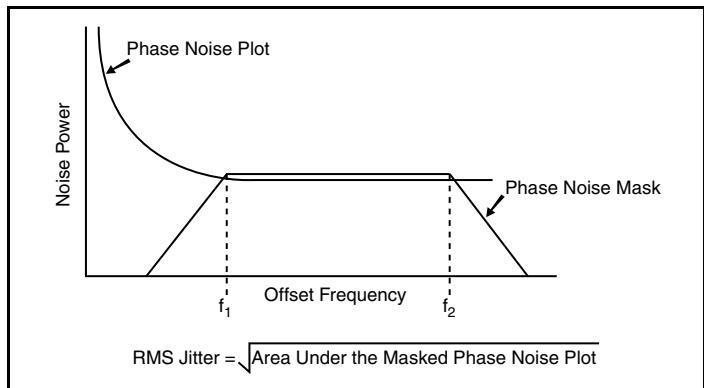
Parameter Measurement Information



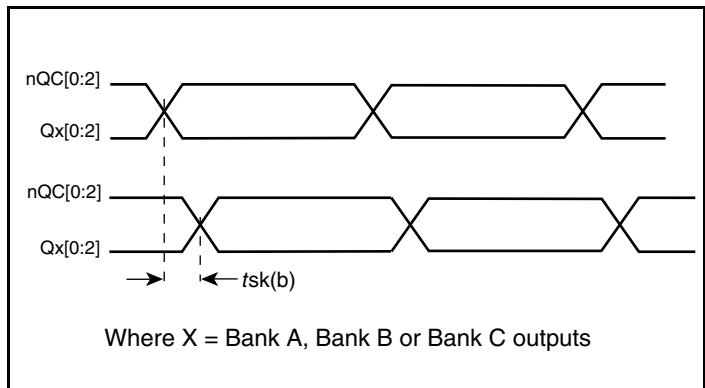
3.3V LVDS Output Load AC Test Circuit



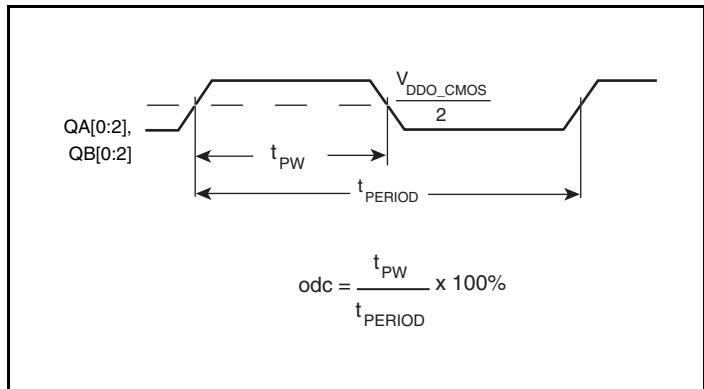
3.3V LVCMOS Output Load AC Test Circuit



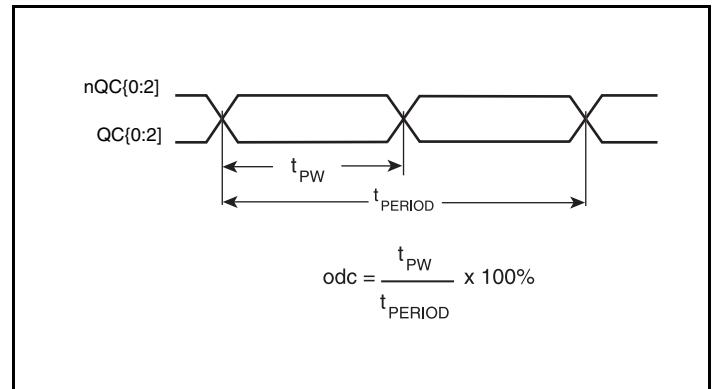
RMS Phase Jitter



Bank Skew

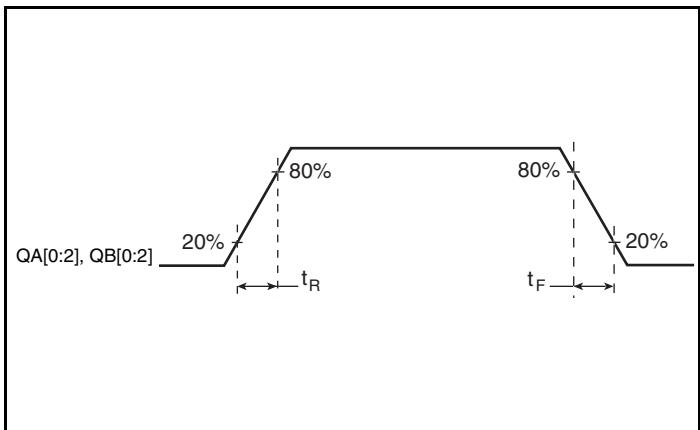


Single-Ended Output Duty Cycle/Pulse Width/Period

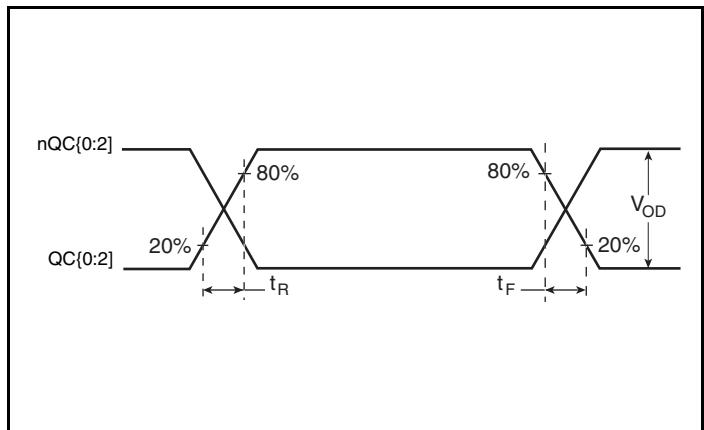


Differential Output Duty Cycle/Pulse Width/Period

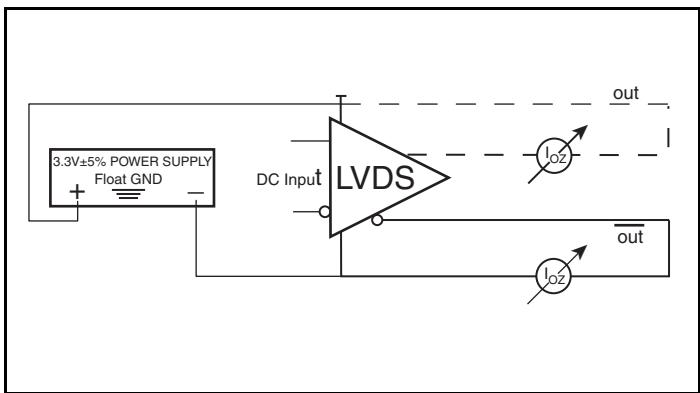
Parameter Measurement Information, continued



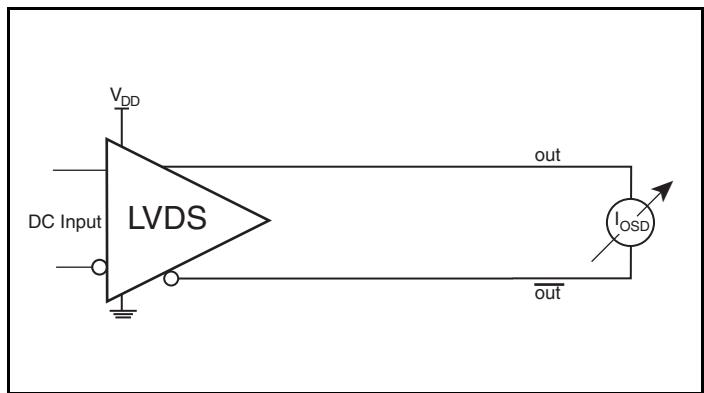
LVC MOS Output Rise/Fall Time



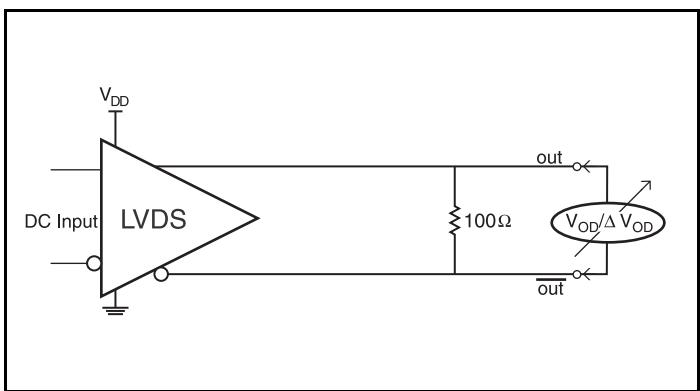
LVDS Output Rise/Fall Time



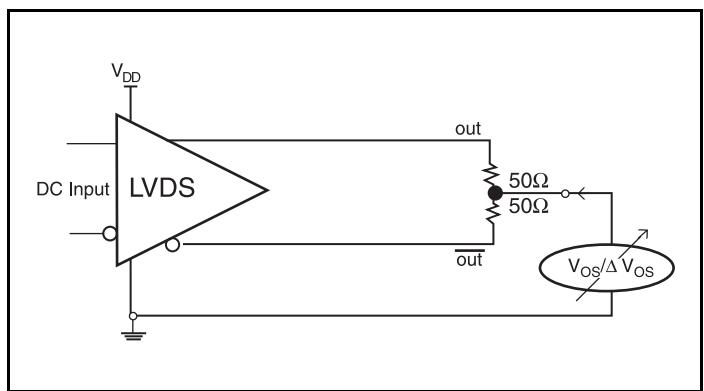
High Impedance Leakage Current Setup



Differential Output Short Circuit Setup

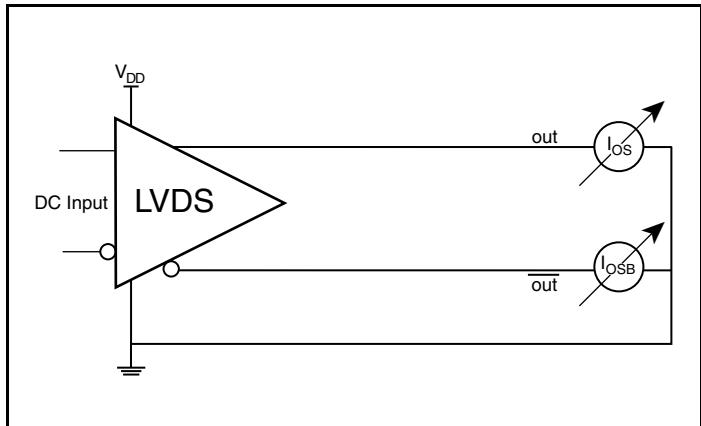


Differential Output Voltage Setup

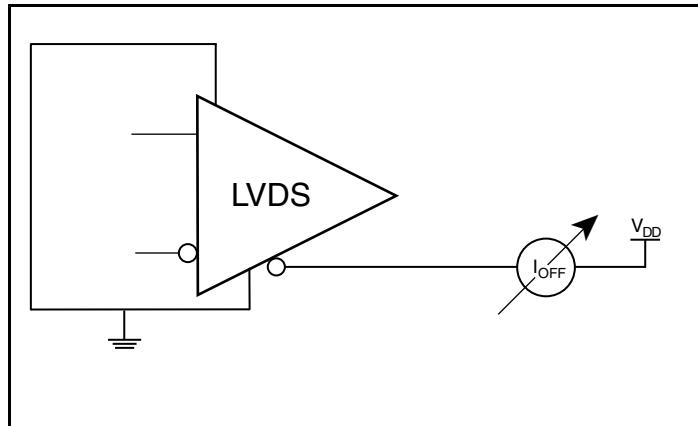


Offset Voltage Setup

Parameter Measurement Information, continued



Output Short Circuit Current Setup



Power Off Leakage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8402015 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , V_{DDO_A} , V_{DDO_B} , V_{DDO_C} , and V_{DDO_REF} should be individually connected to the power supply plane through vias, and $0.01\mu F$ bypass capacitors should be used for each pin. Figure 1 illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu F$ bypass capacitor be connected to the V_{DDA} pin.

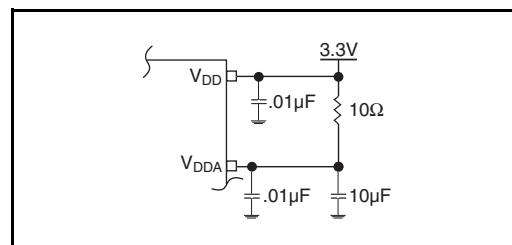


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A $1k\Omega$ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS outputs should be terminated with 100Ω resistor between the differential pair.

LVCMS Outputs

All unused LVCMS output can be left floating. There should be no trace attached.

Crystal Input Interface

The 8402015 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were

determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

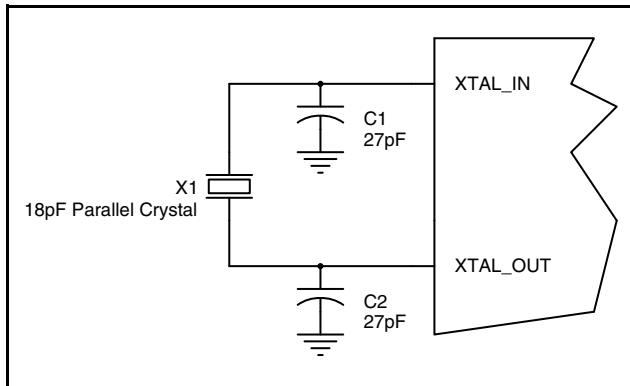


Figure 2. Crystal Input Interface

LVCMS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, $R1$ and $R2$ in parallel should equal the transmission line impedance. For most 50Ω applications, $R1$ and $R2$ can be 100Ω . This can also be accomplished by removing $R1$ and making $R2$ 50Ω .

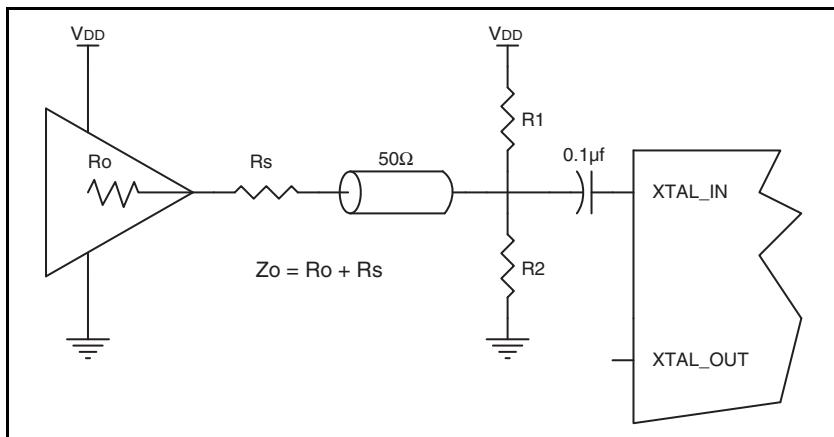


Figure 3. General Diagram for LVCMS Driver to XTAL Input Interface

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple

LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

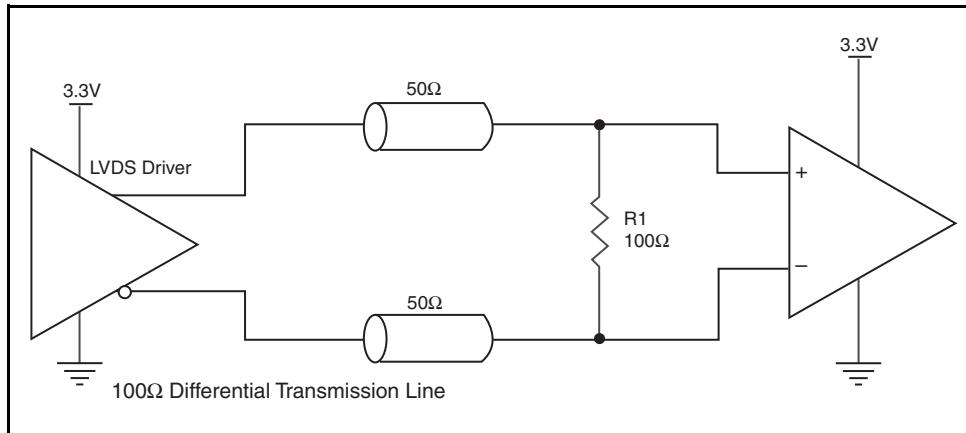


Figure 4. Typical LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

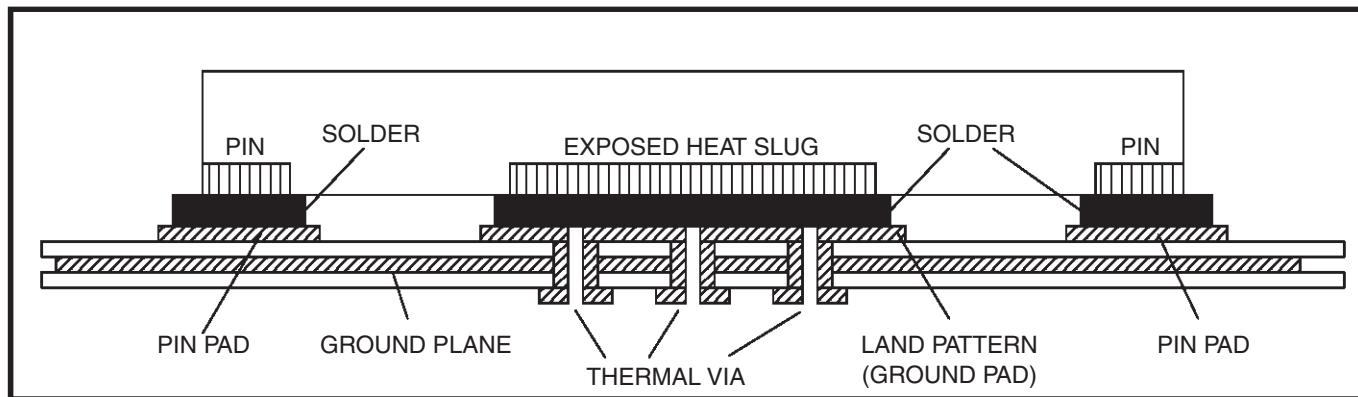


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 6 shows an example of 8402015 application schematic. In this example, the device is operated at $V_{DD} = V_{DDO_REF} = V_{DDO_A} = V_{DDO_B} = V_{DDO_C} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The $C1 = 27pF$ and $C2 = 27pF$ are recommended for

frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two example of LVDS for receiver without built-in termination and one example of LVCMOS are shown in this schematic.

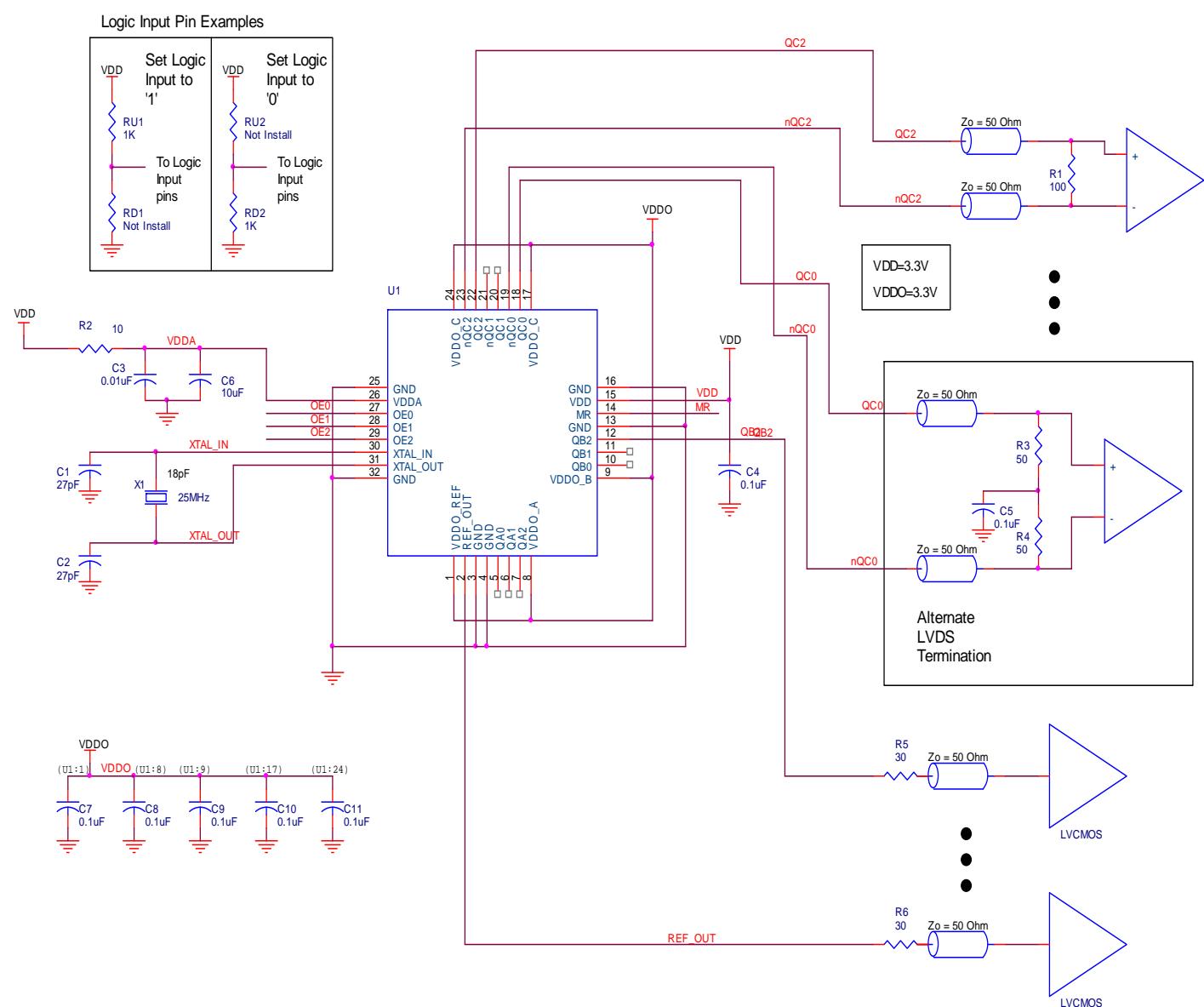


Figure 6.8402015 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8402015. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8402015 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = $V_{DD_MAX} * (I_{DD} + I_{DDO_X} + I_{DDA}) = 3.465V * (30mA + 26mA + 36mA) = 318.78mW$

LVCMS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
Output Current $I_{OUT} = V_{DD_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 20\Omega)] = 24.7mA$
- Power Dissipation on the R_{OUT} per LVCMS output
Power (R_{OUT}) = $R_{OUT} * (I_{OUT})^2 = 20\Omega * (24.7mA)^2 = 12.25mW$ per output
- Total Power Dissipation on the R_{OUT}
Total Power (R_{OUT}) = $12.25mW * 6 = 73.5mW$

Total Power Dissipation

- Total Power**
= Power (core, LVDS) + Total Power (R_{OUT})
= $318.78mW + 73.5mW$
= 392.28mW

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C .

The equation for T_j is as follows: $T_j = \theta_{JA} * P_{d_total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

P_{d_total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.392W * 37^\circ\text{C/W} = 99.5^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} Vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Transistor Count

The transistor count for 8402015 is: 2311

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN

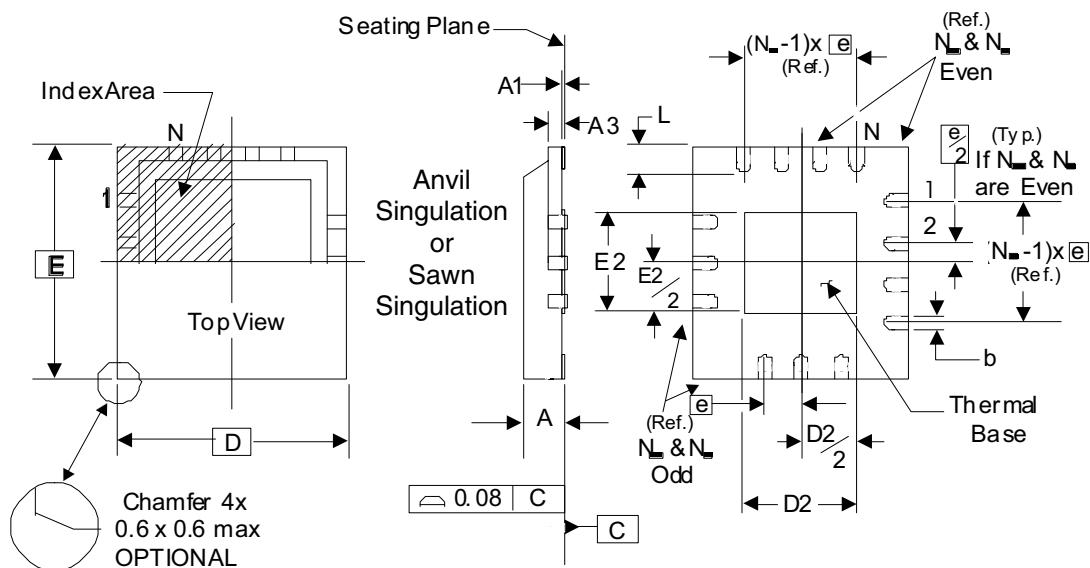


Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

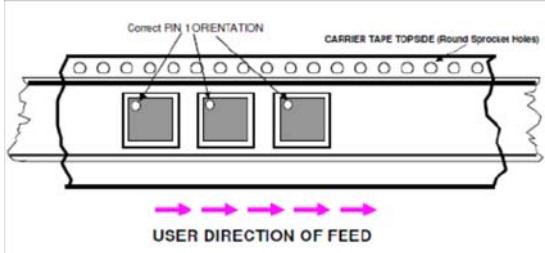
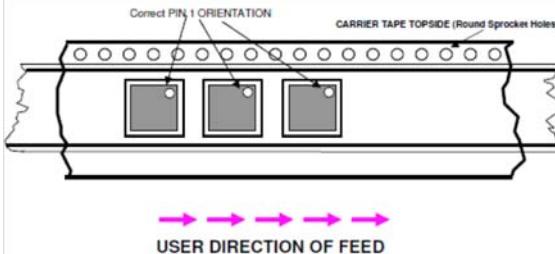
Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8402015AKILF	ICS02015AIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8402015AKILFT	ICS02015AIL	“Lead-Free” 32 Lead VFQFN	Tape & Reel, pin 1 orientation: EIA-481-C	-40°C to 85°C
8402015AKILF/W	ICS02015AIL	“Lead-Free” 32 Lead VFQFN	Tape & Reel, pin 1 orientation EIA-481-D	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Table 11. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	17	Ordering Information Table - added "I" in part/order number.	6/25/09
B	T10 T11	17	Ordering Information - Added W Part. Added Pin 1 Orientation in Tape and Reel table Updated data sheet format.	7/2/15

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