

### Description

The MK5811 device generates a low EMI output clock from a clock or crystal input. The device is designed to dither a high emissions clock to lower EMI in consumer applications. Using IDT's proprietary mix of analog and digital Phase Locked Loop (PLL) technology, the device spreads the frequency spectrum of the output and reduces the frequency amplitude peaks by several dB. The MK5811 offers both centered and down spread from a high-speed clock input.

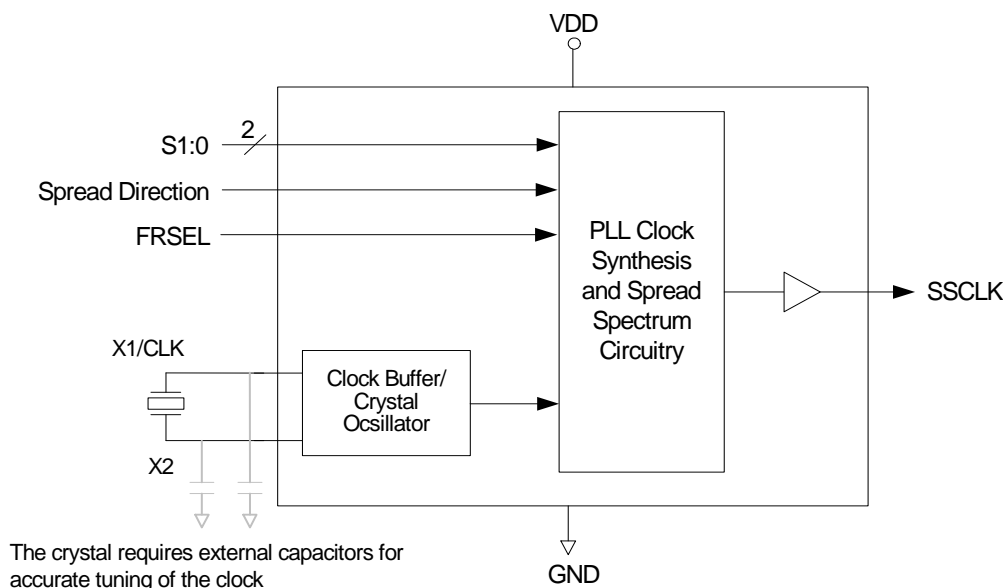
For different multiplier configurations, use the MK5812 (2x) or MK5814 (4x).

IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

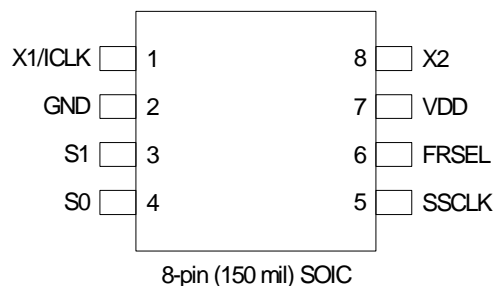
### Features

- Packaged in 8-pin SOIC
- Pb (lead) free package
- Provides a spread spectrum output clock
- Supports flat panel controllers
- Accepts a clock or crystal input (provides same frequency dithered output)
- Input frequency range of 4 to 32 MHz
- Output frequency range of 4 to 32 MHz
- 1X frequency multiplication
- Center and down spread
- Peak reduction by 8 dB to 16 dB typical on 3rd through 19th odd harmonics
- Low EMI feature can be disabled
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process
- ***The MK5811A is recommended for new designs.***

### Block Diagram



## Pin Assignment



## Spread Direction and Spread Percentage

S1 Pin 3	S0 Pin 4	Spread Direction	Spread Percentage
0	0	Center	±1.4
0	M	Center	±1.1
0	1	Center	±0.6
M	0	Center	±0.5
M	M	No Spread	-
M	1	Down	-1.6
1	0	Down	-2.0
1	M	Down	-0.7
1	1	Down	-3.0

0 = connect to GND

M = unconnected (floating)

1 = connect directly to VDD

## Frequency Selection

Product	FRSEL (pin 6)	Input Freq. Range	Multiplier	Output Freq. Range
MK5811	0	4.0 to 8.0 MHz	X1	4.0 to 8.0 MHz
	1	8.0 to 16.0MHz	X1	8.0 to 16.0MHz
	M	16.0 to 32.0MHz	X1	16.0 to 32.0MHz
MK5812 <sup>1</sup>	0	4.0 to 8.0 MHz	X2	8.0 to 16.0MHz
	1	8.0 to 16.0MHz	X2	16.0 to 32.0MHz
	M	16.0 to 32.0MHz	X2	32.0 to 64.0MHz
MK5814 <sup>1</sup>	0	4.0 to 8.0 MHz	X4	16.0 to 32.0MHz
	1	8.0 to 16.0MHz	X4	32.0 to 64.0MHz
	M	16.0 to 32.0MHz	X4	64.0 to 128MHz

0 = connect to GND

M = unconnected (floating)

1 = connect directly to VDD

Note 1: The information in this datasheet does not apply to the MK5812 and MK5814 as each have independent datasheets available at [www.idt.com](http://www.idt.com).

## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	Input	Connect to 4-32 MHz crystal or clock.
2	GND	Power	Connect to ground.
3	S1	Input	Function select 1 input. Selects spread amount and direction per table above. (default-internal mid-level).
4	S0	Input	Function select 0 input. Selects spread amount and direction per table above. (default-internal mid-level).
5	SSCLK	Output	Clock output with Spread spectrum
6	FRSEL	Input	Function select for input frequency range. Default to mid level "M".
7	VDD	Power	Connect to +3.3 V.
8	X2	XO	Crystal connection to 4-32 MHz crystal. Leave unconnected for clock

## External Components

The MK5811 requires a minimum number of external components for proper operation.

### Decoupling Capacitor

A decoupling capacitor of 0.01μF must be connected between VDD and GND on pins 7 and 2. Connect the capacitor as close to these pins as possible. For optimum device performance, mount the decoupling capacitor on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

### Series Termination Resistor

Use series termination when the PCB trace between the clock output and the load is over 1 inch. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line. Place the resistor as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

### Tri-level Select Pin Operation

The S1 and S0 select pins are tri-level, meaning that they have three separate states to make the selections shown in the table on page 2. To select the M (mid) level, the connection to these pins must be eliminated by either floating them originally, or tri-stating the GPIO pins which drive the select pins.

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, observe the following guidelines:

- 1) Mount the 0.01μF decoupling capacitor on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to the VDD pin and the PCB trace to the ground via should be kept as short as possible.
- 2) To minimize EMI, place the 33Ω series-termination resistor (if needed) close to the clock output.
- 3) An optimum layout is one with all components on the same side of the board, thus minimizing vias through other signal layers. Other signal traces should be routed away from the MK5811 device. This includes signal traces located underneath the device, or on layers adjacent to the ground plane layer used by the device.

## Crystal Information

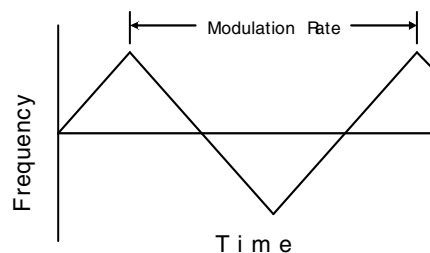
The crystal used should be a fundamental mode (do not use third overtone), parallel resonant crystal. To optimize the initial accuracy, connect crystal capacitors from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation,  $C_L$  is the crystal load capacitance. For example, a crystal with a 16 pF load capacitance uses two 20 pF  $[(16 \times 2)]$  capacitors.

## Spread Spectrum Profile

The MK5811 is a low EMI clock generator using an optimized frequency slew rate algorithm to facilitate downstream tracking of zero delay buffers and other PLL devices.



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK5811. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device, at these or any other conditions, above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.0		3.63	V

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0	3.3	3.63	V
Supply Current	IDD	No load, at 3.3 V, Fin=12 MHz		23	25	mA
		No load, at 3.3 V, Fin=24 MHz			30	mA
		No load, at 3.3 V, Fin=32 MHz			35	mA
Input High Voltage	V <sub>IH</sub>		0.85VDD	VDD	VDD	V
Input middle Voltage	V <sub>IHM</sub>		0.4VDD	0.5VDD	0.6VDD	V
Input Low Voltage	V <sub>IL</sub>		0.0	0.0	0.15VDD	V
Output High Voltage	V <sub>OH</sub>	CMOS, I <sub>OH</sub> = -4 mA	2.4			V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -6 mA	2.0			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = -4 mA			0.4	V
		I <sub>OL</sub> = -10 mA			1.2	V
Input Capacitance	C <sub>IN1</sub>	S0, S1, FRSEL pins		4	6	pF
	C <sub>IN2</sub>	X1, X2 pins		6	9	pF

## AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +85° C, C<sub>L</sub> = 15 pF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency			4		32	MHz
Output Clock Frequency			4		32	MHz
Input Clock Duty Cycle		Time above VDD/2	40		60	%
Output Clock Duty Cycle		Time above 1.5 V	45	50	55	%
Cycle-to-cycle Jitter <sup>1</sup>		Fin=4 MHz, Fout=4 MHz		350	800	ps
Cycle-to-cycle Jitter <sup>1</sup>		Fin=8 MHz, Fout=8 MHz		250	450	ps
Output Rise Time	t <sub>R</sub>	0.4 to 2.4 V	1.6		5.0	ns
Output Fall Time	t <sub>F</sub>	2.4 to 0.4 V	1.6		4.4	ns
EMI Peak Frequency Reduction				8 to 16		dB

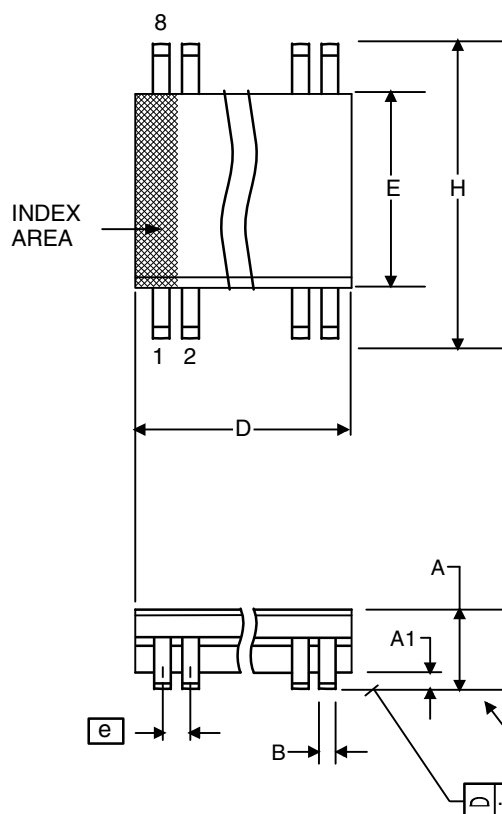
Note 1: Spread is enabled.

## Thermal Characteristics

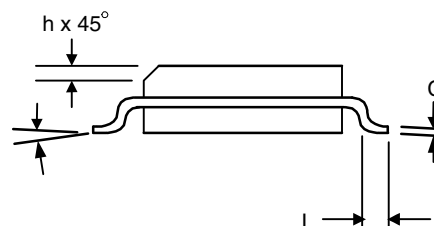
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ <sub>JA</sub>	Still air		150		°C/W
	θ <sub>JA</sub>	1 m/s air flow		140		°C/W
	θ <sub>JA</sub>	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ <sub>JC</sub>			40		°C/W

## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
$\alpha$	0°	8°	0°	8°



## Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK5811SLF	5811SL	Tubes	8-pin SOIC	0 to +85° C
MK5811SLFTR	5811SL	Tape and Reel	8-pin SOIC	0 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology, Inc. (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.