

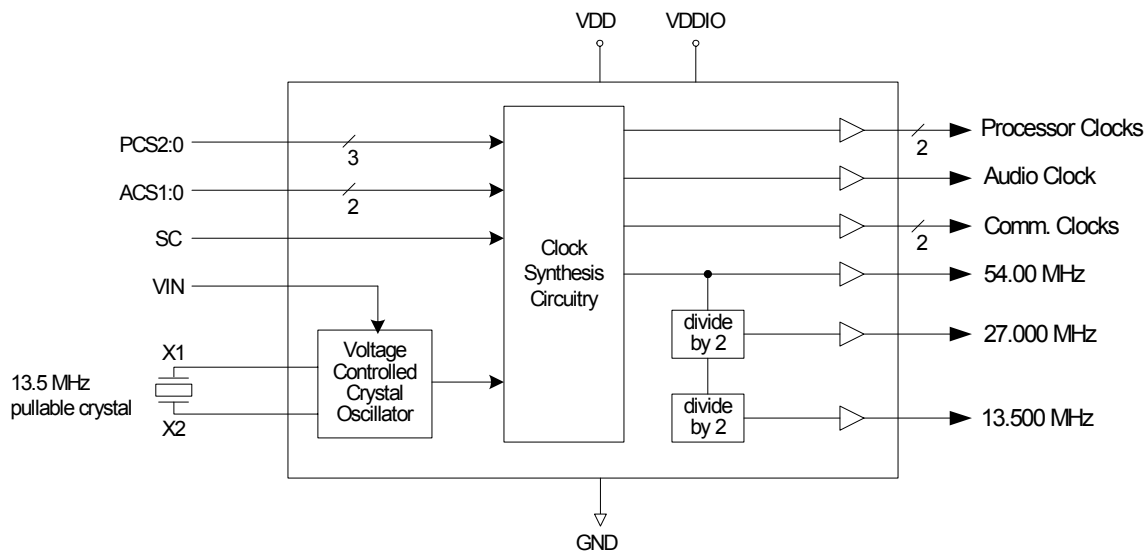
Description

The MK2771-15 is a low-cost, low-jitter, high-performance VCXO and clock synthesizer designed for set-top boxes. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3 V input voltage to cause the output clocks to vary by ± 100 ppm. Using IDT's patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 13.5 MHz pullable crystal input to produce multiple output clocks including two selectable processor clocks, a selectable audio clock, two communications clocks, and three fixed clocks. All clocks are frequency locked to the 27.00 MHz output (and to each other) with zero ppm error, so any output can be used as the VCXO output.

Features

- Packaged in 28 pin SSOP
- Pb-free package
- Ideal for systems using Oak's MPEG decoders
- On-chip patented VCXO with pull range of 200 ppm
- VCXO tuning voltage of 0 to 3 V
- Processor frequencies include 33.3, 40, 50, 66.6, 81, and 100 MHz
- Audio clocks of 8.192 MHz, 11.2896 MHz, 12.288 MHz and 18.432 MHz
- Zero ppm synthesis error in all clocks (all exactly track 27 MHz VCXO)
- Uses an inexpensive 13.5 MHz pullable crystal
- Full CMOS output swings with 25 mA output drive capability at TTL levels
- Advanced, low-power, sub-micron CMOS process
- 5 V operating voltage with 3.3 V capable I/O

Block Diagram



Pin Assignment

PCS0	☐	1	28	☐	ACS1
X2	☐	2	27	☐	ACS0
X1	☐	3	26	☐	54M
VDD	☐	4	25	☐	27M
VDD	☐	5	24	☐	GND
VIN	☐	6	23	☐	CCLK1
VDDIO	☐	7	22	☐	VDD
VDD	☐	8	21	☐	VDD
SC	☐	9	20	☐	PCS2
GND	☐	10	19	☐	GND
PCLK1	☐	11	18	☐	GND
PCLK2	☐	12	17	☐	CCLK2
PCS1	☐	13	16	☐	13.5M
ACLK	☐	14	15	☐	DC

Processor Clock Select Table (MHz)

PCS2	PCS1	PCS0	PCLK1	PCLK2
0	0	0	27.500	OFF
0	0	1	33.333	66.666
0	1	0	33.326	83.314
0	1	1	50.000	100.000
1	0	0	32.400	81.000
1	0	1	40.000	33.333
1	1	0	TEST	TEST
1	1	1	TEST	TEST

Audio Clock Table

ACS1	ACS0	ACLK (MHz)
0	0	8.192
0	1	11.2896
1	0	12.288
1	1	18.432

Comm Clock Table (MHz)

SC	CCLK1	CCLK2
0	18.432	24.576
M	11.0592	18.432
1	11.0592	24.576

0 = connect directly to ground

1 = connect directly to VDDIO

M = leave floating or unconnected

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	PCS0	Input	Processor clock select 0. Selects PCLKs on pins 11 and 12. See table above. Internal pull-up resistor.
2	X2	XO	Crystal connection. Connect to a pullable 13.5 MHz crystal.
3	X1	XI	Crystal connection. Connect to a pullable 13.5 MHz crystal.
4, 5, 8	VDD	Power	Connect to +5 V.
6	VIN	Input	Voltage input to VCXO. Zero to 3 V signal which controls the frequency of the VCXO.
7	VDDIO	Power	Connect to +3.3 V or +5 V. Amplitude of inputs must, and outputs will, match this.
9	SC	Tri-level input	Communications clock select pin. Biased to M level if floating
10, 18, 19, 24	GND	Power	Connect to ground.
11	PCLK1	Output	Processor clock output number 1. Determined by status of PCS2:0.
12	PCLK2	Output	Processor clock output number 2. Determined by status of PCS2:0.
13	PCS1	Input	Processor clock select 1. Selects PCLKs on pins 11 and 12. See table above. Internal pull-up resistor.
14	ACLK	Output	Audio clock output. Determined by status of ACS1, ACS0 per table above.
15	DC	—	Don't Connect anything to this pin.
16	13.5M	Output	13.50 MHz VCXO clock output.
17	CCLK2	Output	Communications clock output 2 determined by status of SC per table above.
20	PCS2	Input	Processor clock select 2. Selects PCLKs on pins 11 and 12. See table above. Internal pull-up resistor.
21, 22	VDD	Power	Connect to +5 V.
23	CCLK1	Output	Communications clock output 1 determined by status of SC per table above.
25	27M	Output	27.00 MHz VCXO clock output.
26	54M	Output	54.00 MHz VCXO clock output.
27	ACS0	Input	Audio clock select 0. Selects ACLK on pin 14. See table above. Internal pull-up resistor.
28	ACS1	Input	Audio clock select 1. Selects ACLK on pin 14. See table above. Internal pull-up resistor.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2771-15. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD (referenced to GND)	7 V
Inputs and Clock Outputs (referenced to GND)	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

DC Electrical Characteristics

Unless stated otherwise, **VDD = 5 V**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.75		5.25	V
Operating Voltage	VDDIO	All inputs/outputs	3.15		5.25	V
Input High Voltage, X1 pin only	V _{IH}		3.5	2.5		V
Input Low Voltage, X1 pin only	V _{IL}			2.5	1.5	V
Input High Voltage, except SC and PCS2	V _{IH}		2			V
Input Low Voltage, except SC and PCS2	V _{IL}				0.8	V
Input High Voltage, SC and PCS2 only	V _{IH}		VDDIO-0.5			V
Input Low Voltage, SC and PCS2 only	V _{IL}				0.5	V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA	–	–	0.4	V
Output High Voltage, CMOS Level	V _{OH}	I _{OH} = -8 mA	VDDIO-0.4			V
Operating Supply Current	IDD + IDDIO (3.3 V)	No load, Note 1		46+27		mA
Short Circuit Current	I _{OS}	Each output		±100		mA
Input Capacitance, except X1	C _{IN}	Except X1, X2		7		pF
Frequency Synthesis Error		All clocks			0	ppm
VIN, VCXO Control Voltage			0		3	V

AC Electrical Characteristics

Unless stated otherwise, **VDD = 5 V**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			13.500000			MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V, no load		1.5		ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V, no load		1.5		ns
Output Clock Duty Cycle	t_{OD}	At VDDIO/2	40	50	60	%
Maximum Absolute Jitter, short term	t_{ja}			300		ps
VCXO Pullability	t_{ja}	Note 2	-100		100	ppm

Note 1: With PCLK at 100 MHz.

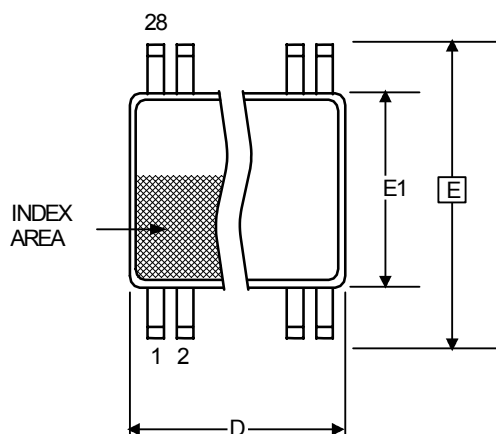
Note 2: With a pullable crystal that conforms to IDT's specifications.

Pullable Crystal Specifications

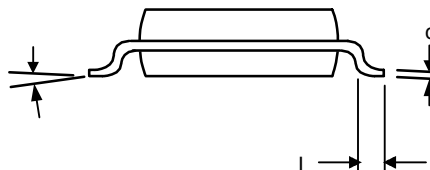
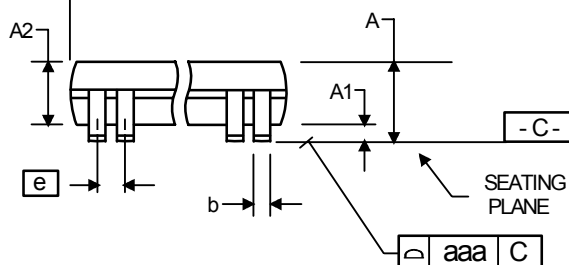
Frequency	13.500000 MHz
Correlation (load) Capacitance	14 pF
CO/C1	240 max.
ESR	35 Ω max.
Operating Temperature	0 to 70°C
Initial Accuracy	±20 ppm
Temperature plus Aging Stability	±50 ppm

Package Outline and Package Dimensions (28-pin SSOP)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.102	0.254	0.004	0.010
A2	--	1.50	--	.059
b	0.203	0.305	0.008	0.012
c	0.191	0.254	0.007	0.010
D	9.804	10.008	0.386	0.394
E	5.791	6.198	0.228	0.244
E1	3.810	3.988	0.150	0.157
e	.635 Basic		.025 Basic	
L	0.406	1.270	0.016	0.050
α	0°	8°	0°	8°



Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
MK2771-15RLF	MK2771-15LF	Tubes	28-pin SSOP	0 to +70° C
MK2771-15RLFTR	MK2771-15LF	Tape and Reel	28-pin SSOP	0 to +70° C

Note: "LF" denotes Pb (lead) free package.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.