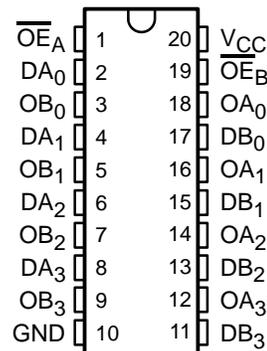


CY54FCT244T, CY74FCT244T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

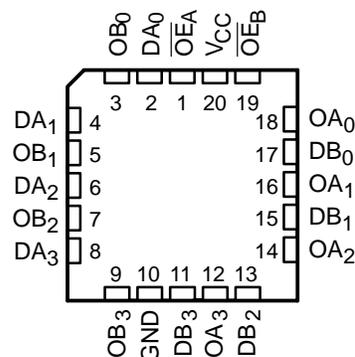
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- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT244T
 - 48-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT244T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

CY54FCT244T . . . D PACKAGE
CY74FCT244T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



CY54FCT244T . . . L PACKAGE
(TOP VIEW)



description

The 'FCT244T devices are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts, while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT244T, CY74FCT244T
8-BIT BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QSOP – Q	Tape and reel	3.6	CY74FCT244DTQCT	FCT244D
	SOIC – SO	Tube	3.6	CY74FCT244DTSOC	FCT244D
		Tape and reel	3.6	CY74FCT244DTSOCT	
–40°C to 85°C	SOIC – SO	Tube	4.1	CY74FCT244CTSOC	FCT244C
		Tape and reel	4.1	CY74FCT244CTSOCT	
	QSOP – Q	Tape and reel	4.1	CY74FCT244CTQCT	FCT244C
	DIP – P	Tube	4.6	CY74FCT244ATPC	CY74FCT244ATPC
	SOIC – SO	Tube	4.6	CY74FCT244ATSOC	FCT244A
		Tape and reel	4.6	CY74FCT244ATSOCT	
	QSOP – Q	Tape and reel	4.6	CY74FCT244ATQCT	FCT244A
	SOIC – SO	Tube	6.5	CY74FCT244TSOC	FCT244
		Tape and reel	6.5	CY74FCT244TSOCT	
	QSOP – Q	Tape and reel	6.5	CY74FCT244TQCT	FCT244
	–55°C to 125°C	CDIP – D	Tube	4.6	CY54FCT244CTDMB
LCC – L		Tube	4.6	CY54FCT244CTLMB	
CDIP – D		Tube	5.1	CY54FCT244ATDMB	
LCC – L		Tube	5.1	CY54FCT244ATLMB	
CDIP – D		Tube	7	CY54FCT244TDMB	
LCC – L		Tube	7	CY54FCT244TLMB	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

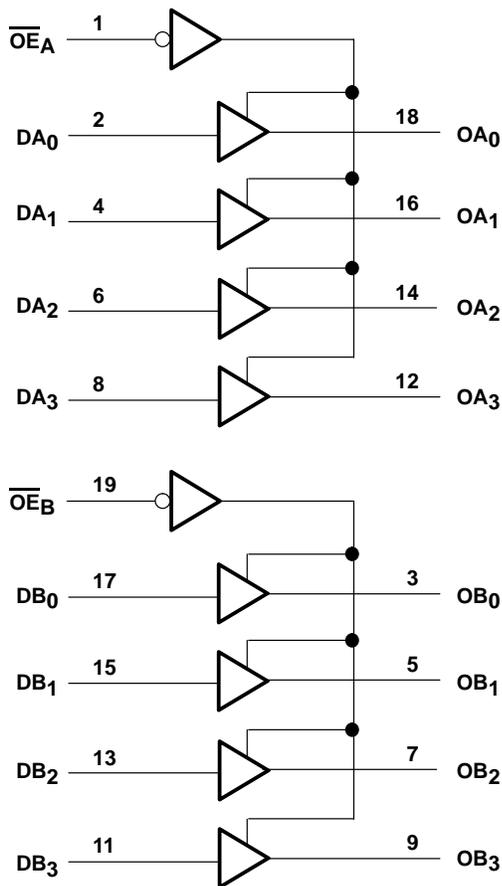
FUNCTION TABLE

INPUTS			OUTPUT
\overline{OE}_A	\overline{OE}_B	D	O
L	L	L	L
L	L	H	H
H	H	X	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state



logic diagram (positive logic)



absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	-0.5 V to 7 V
DC input voltage range	-0.5 V to 7 V
DC output voltage range	-0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package	69°C/W
Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, T_A	-65°C to 135°C
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

CY54FCT244T, CY74FCT244T
8-BIT BUFFERS/LINE DRIVERS
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recommended operating conditions (see Note 2)

	CY54FCT244T			CY74FCT244DT			CY74FCT244T			UNIT			
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX				
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V			
V _{IH} High-level input voltage	2			2			2			V			
V _{IL} Low-level input voltage	0.8			0.8			0.8			V			
I _{OH} High-level output current	-12			-32			-32			mA			
I _{OL} Low-level output current	48			64			64			mA			
T _A Operating free-air temperature	-55			125			0			70	-40	85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



CY54FCT244T, CY74FCT244T
8-BIT BUFFERS/LINE DRIVERS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT244T		CY74FCT244T		UNIT
		MIN	TYP†	MAX	MIN	
V _{IK}	V _{CC} = 4.5 V, I _{IN} = -18 mA	-0.7	-1.2			V
	V _{CC} = 4.75 V, I _{IN} = -18 mA			-0.7	-1.2	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.3			V
	V _{CC} = 4.75 V	I _{OH} = -32 mA		2		
		I _{OH} = -15 mA		2.4	3.3	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA	0.3	0.55			V
	V _{CC} = 4.75 V, I _{OL} = 64 mA			0.3	0.55	
V _{hys}	All inputs	0.2		0.2		V
I _I	V _{CC} = 5.5 V, V _{IN} = V _{CC}			5		μA
	V _{CC} = 5.25 V, V _{IN} = V _{CC}				5	
I _{IH}	V _{CC} = 5.5 V, V _{IN} = 2.7 V			±1		μA
	V _{CC} = 5.25 V, V _{IN} = 2.7 V				±1	
I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V			±1		μA
	V _{CC} = 5.25 V, V _{IN} = 0.5 V				±1	
I _{OZH}	V _{CC} = 5.5 V, V _{OUT} = 2.7 V			10		μA
	V _{CC} = 5.25 V, V _{OUT} = 2.7 V				10	
I _{OZL}	V _{CC} = 5.5 V, V _{OUT} = 0.5 V			-10		μA
	V _{CC} = 5.25 V, V _{OUT} = 0.5 V				-10	
I _{OS} ‡	V _{CC} = 5.5 V, V _{OUT} = 0 V	-60	-120	-225		mA
	V _{CC} = 5.25 V, V _{OUT} = 0 V				-60 -120 -225	
I _{off}	V _{CC} = 0 V, V _{OUT} = 4.5 V			±1		μA
I _{CC}	V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V	0.1	0.2			mA
	V _{CC} = 5.25 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V				0.1 0.2	
ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open	0.5	2			mA
	V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open				0.5 2	
I _{CCD} ¶	V _{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	0.06	0.12			mA/ MHz
	V _{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V				0.06 0.12	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.



CY54FCT244T, CY74FCT244T
8-BIT BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS		CY54FCT244T		CY74FCT244T		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
I _C #	V _{CC} = 5.5 V, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	0.7	1.4		mA	
			V _{IN} = 3.4 V or GND	1	2.4			
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} = 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	1.3	2.6			
			V _{IN} = 3.4 V or GND	3.3	10.6			
	V _{CC} = 5.25 V, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V			0.7		1.4
			V _{IN} = 3.4 V or GND			1		2.4
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} = 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V			1.3	2.6	
			V _{IN} = 3.4 V or GND			3.3	10.6	
C _i				5	10	5	10	pF
C _o				9	12	9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

I_C = I_{CC} + ΔI_{CC} × D_H × N_T + I_{CCD} (f₀/2 + f₁ × N₁)

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



CY54FCT244T, CY74FCT244T
8-BIT BUFFERS/LINE DRIVERS
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switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT244T		CY54FCT244AT		CY54FCT244CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	O	1.5	7	1.5	5.1	1.5	4.6	ns
t _{PHL}			1.5	7	1.5	5.1	1.5	4.6	
t _{PZH}	\overline{OE}	O	1.5	8.5	1.5	6.5	1.5	6.5	ns
t _{PZL}			1.5	8.5	1.5	6.5	1.5	6.5	
t _{PHZ}	\overline{OE}	O	1.5	7.5	1.5	5.9	1.5	5.7	ns
t _{PLZ}			1.5	7.5	1.5	5.9	1.5	5.7	

switching characteristics over operating free-air temperature range (see Figure 1)

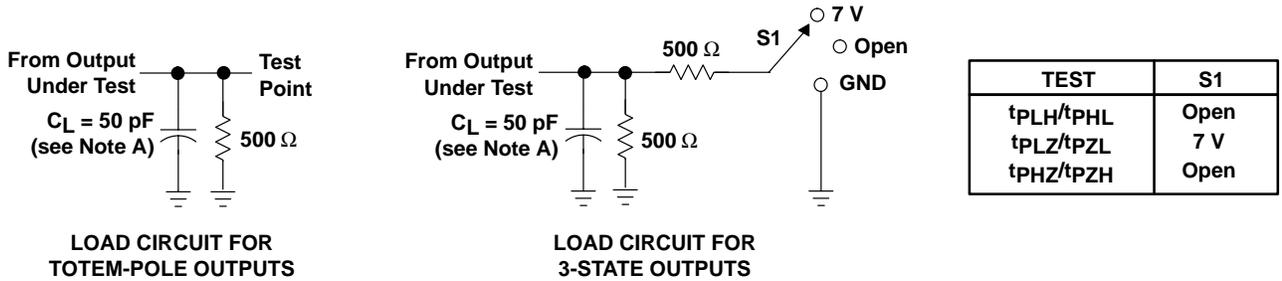
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT244T		CY74FCT244AT		CY74FCT244CT		CY74FCT244DT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	O	1.5	6.5	1.5	4.6	1.5	4.1	1.5	3.6	ns
t _{PHL}			1.5	6.5	1.5	4.6	1.5	4.1	1.5	3.6	
t _{PZH}	\overline{OE}	O	1.5	8	1.5	6.2	1.5	5.8	1.5	4.8	ns
t _{PZL}			1.5	8	1.5	6.2	1.5	5.8	1.5	4.8	
t _{PHZ}	\overline{OE}	O	1.5	7	1.5	5.6	1.5	5.2	1.5	4	ns
t _{PLZ}			1.5	7	1.5	5.6	1.5	5.2	1.5	4	



CY54FCT244T, CY74FCT244T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

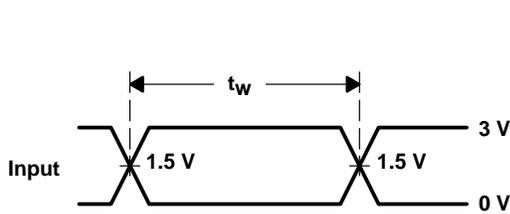
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PARAMETER MEASUREMENT INFORMATION

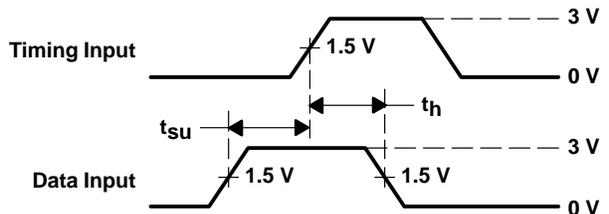


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

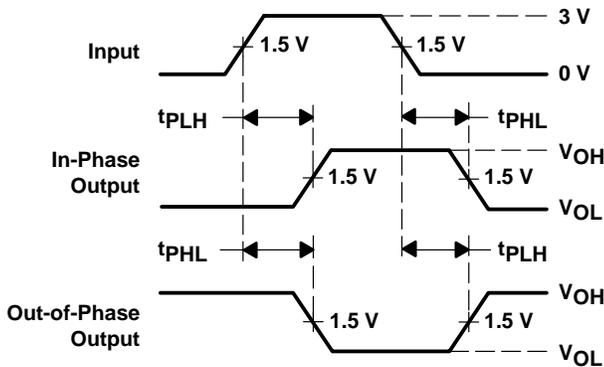
LOAD CIRCUIT FOR 3-STATE OUTPUTS



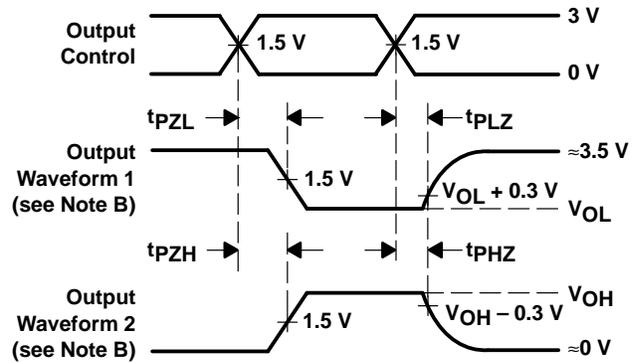
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9220301M2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9220301MRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9220301MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
5962-9220302M2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9220302MRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9220302MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
5962-9220303M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
5962-9220303MRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9220303MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
CY54FCT244ATDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
CY54FCT244ATLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
CY54FCT244ATW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
CY54FCT244CTDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
CY54FCT244CTW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
CY54FCT244TDMB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
CY54FCT244TLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
CY54FCT244TW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
CY74FCT244ATPC	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CY74FCT244ATPCE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CY74FCT244ATQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244ATQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244ATQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244ATSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244ATSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CY74FCT244ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244ATSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244ATSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244CTQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244CTQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244CTQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244CTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244CTSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244CTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244CTSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244DTQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244DTQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244DTQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244DTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244DTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244DTSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244DTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CY74FCT244DTSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244DTSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244TQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244TQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT244TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244TSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244TSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244TSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT244TSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

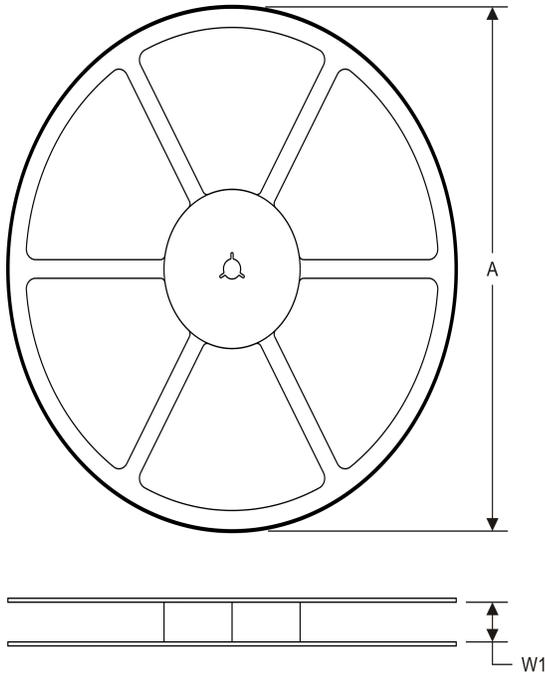
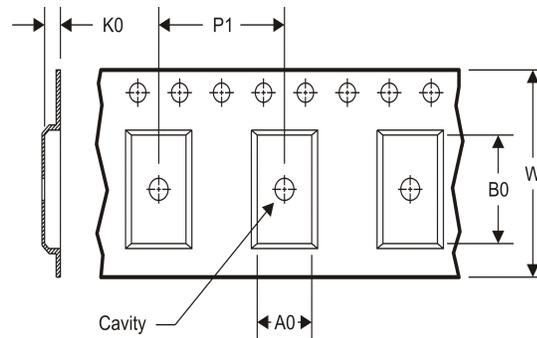
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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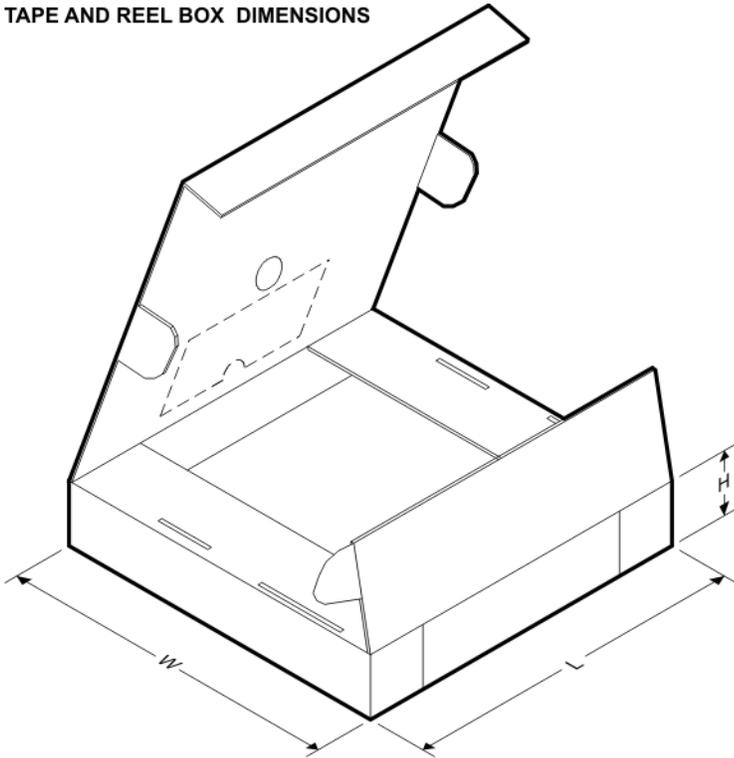
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT244ATQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT244CTQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244CTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT244DTQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244DTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT244TQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


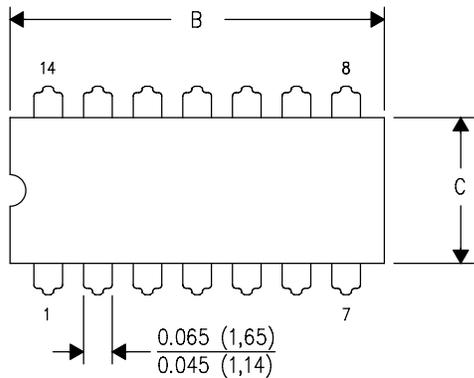
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT244ATQCT	SSOP/QSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT244ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT244CTQCT	SSOP/QSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT244CTSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT244DTQCT	SSOP/QSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT244DTSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT244TQCT	SSOP/QSOP	DBQ	20	2500	367.0	367.0	38.0
CY74FCT244TSOCT	SOIC	DW	20	2000	367.0	367.0	45.0

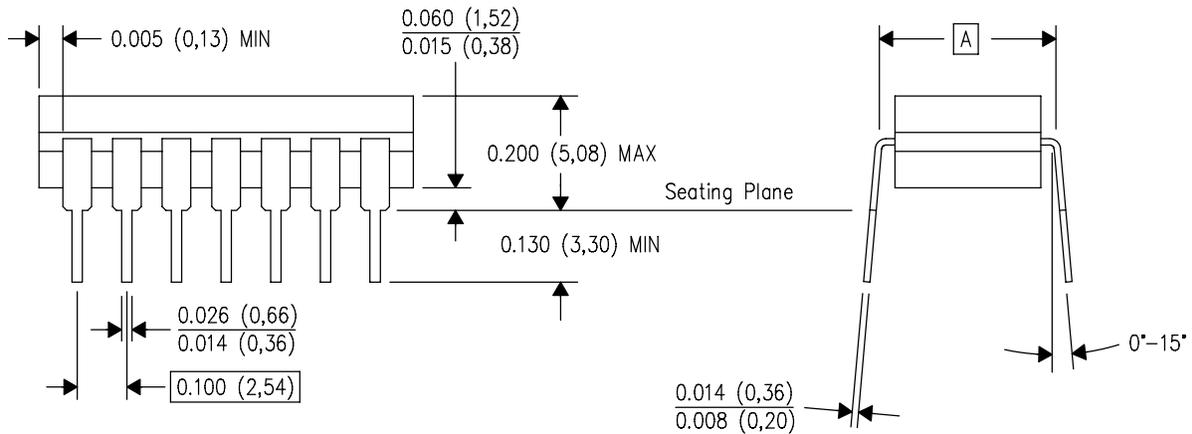
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

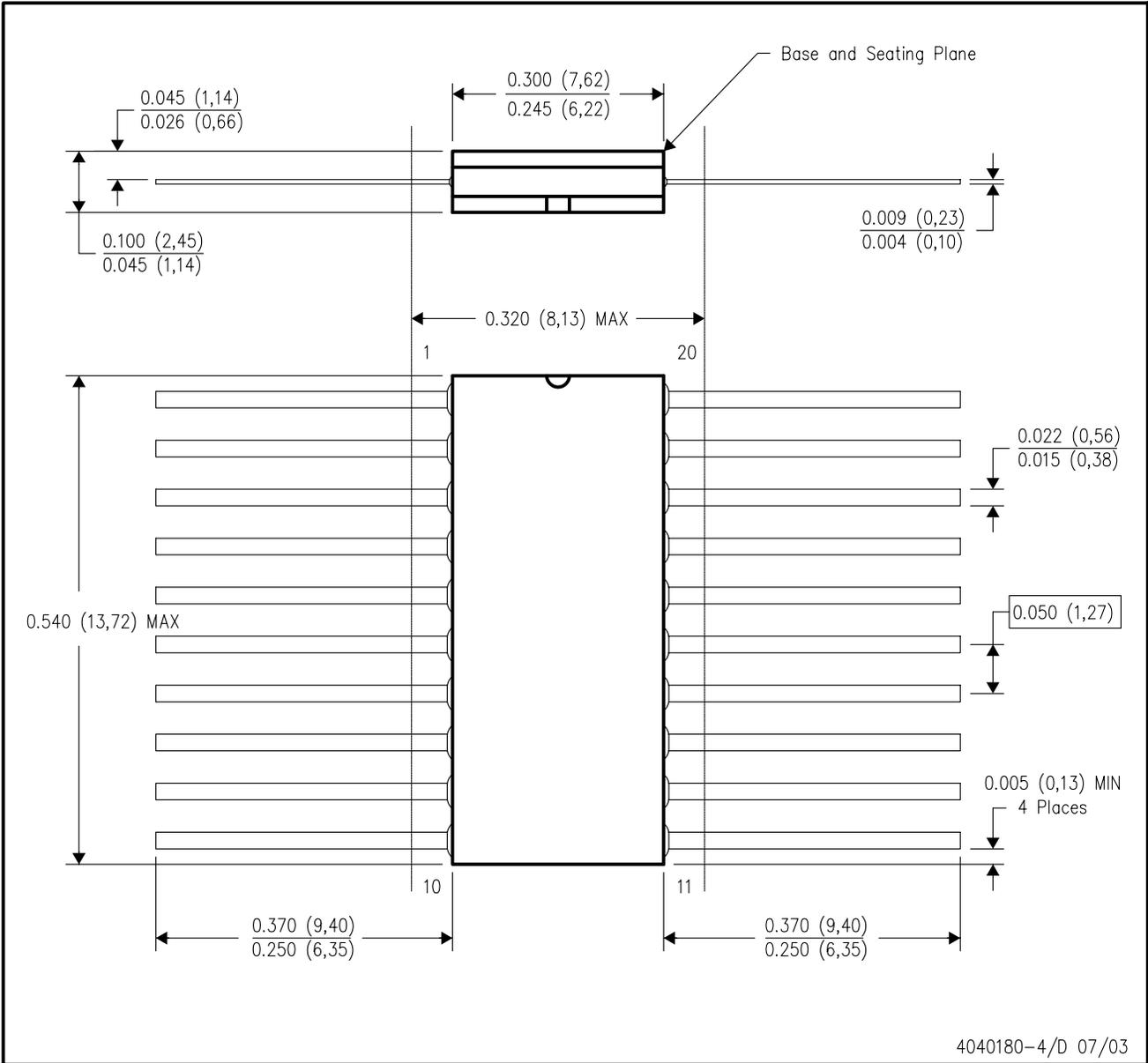


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

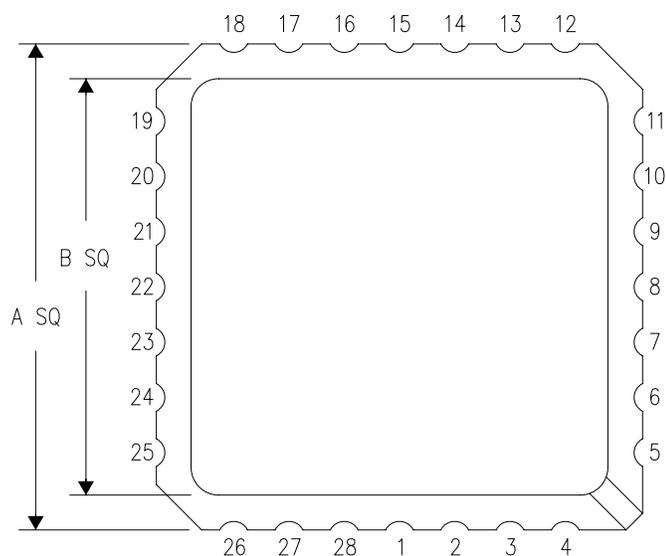


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

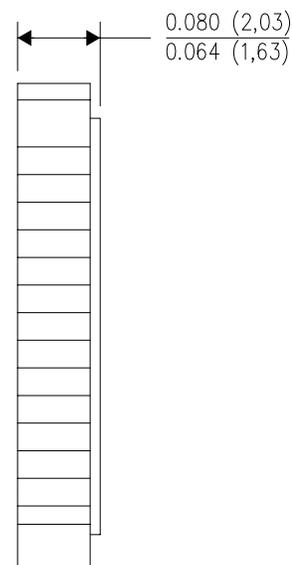
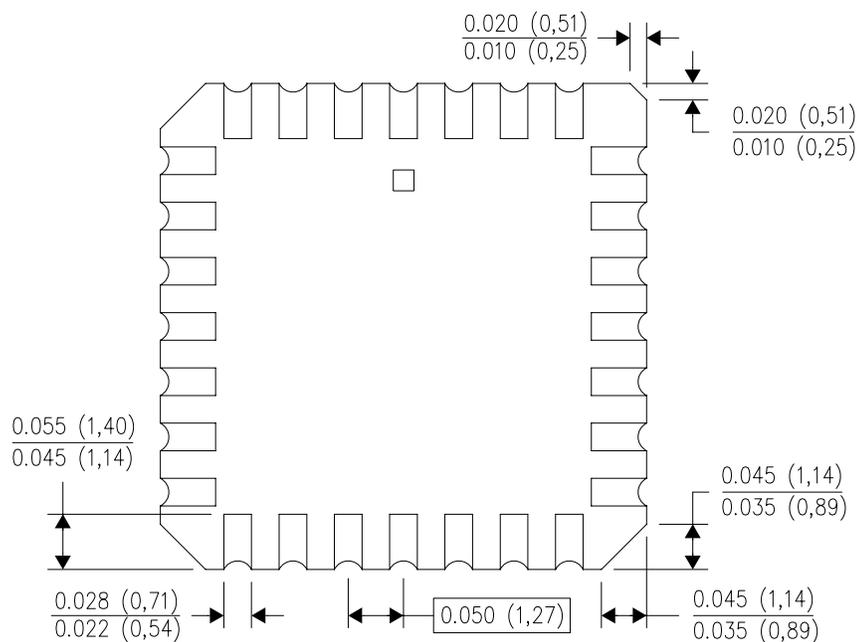
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



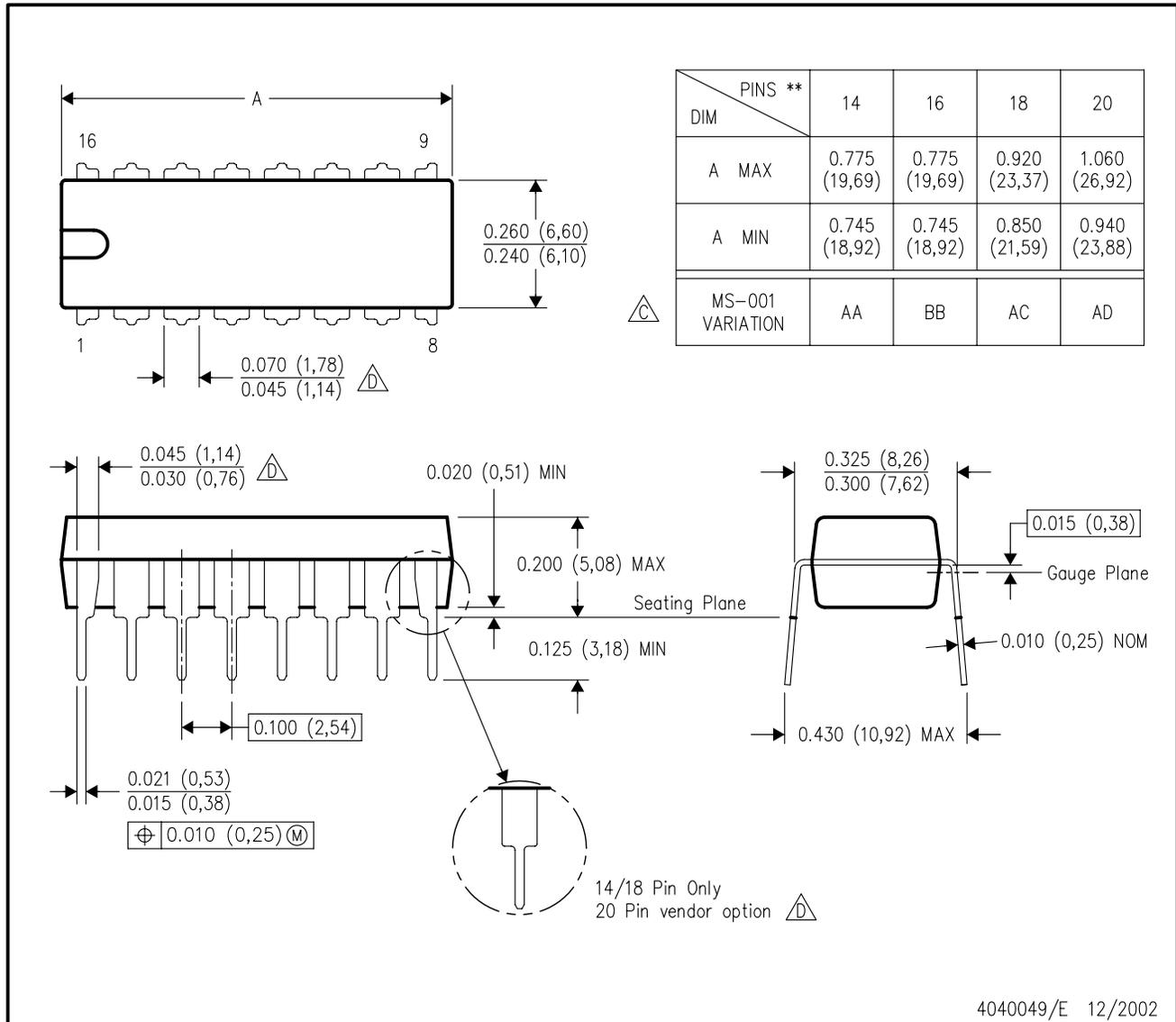
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

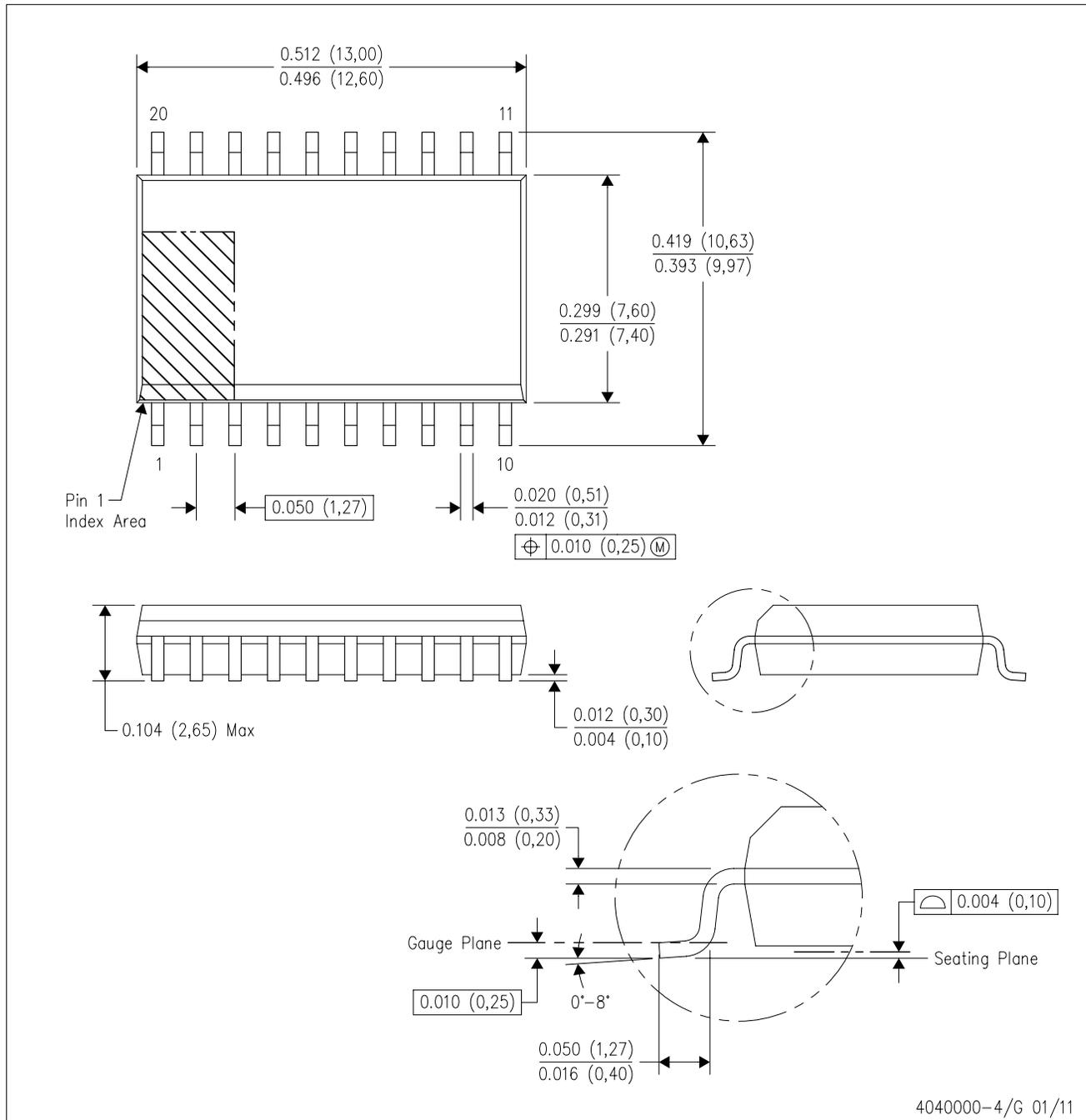
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

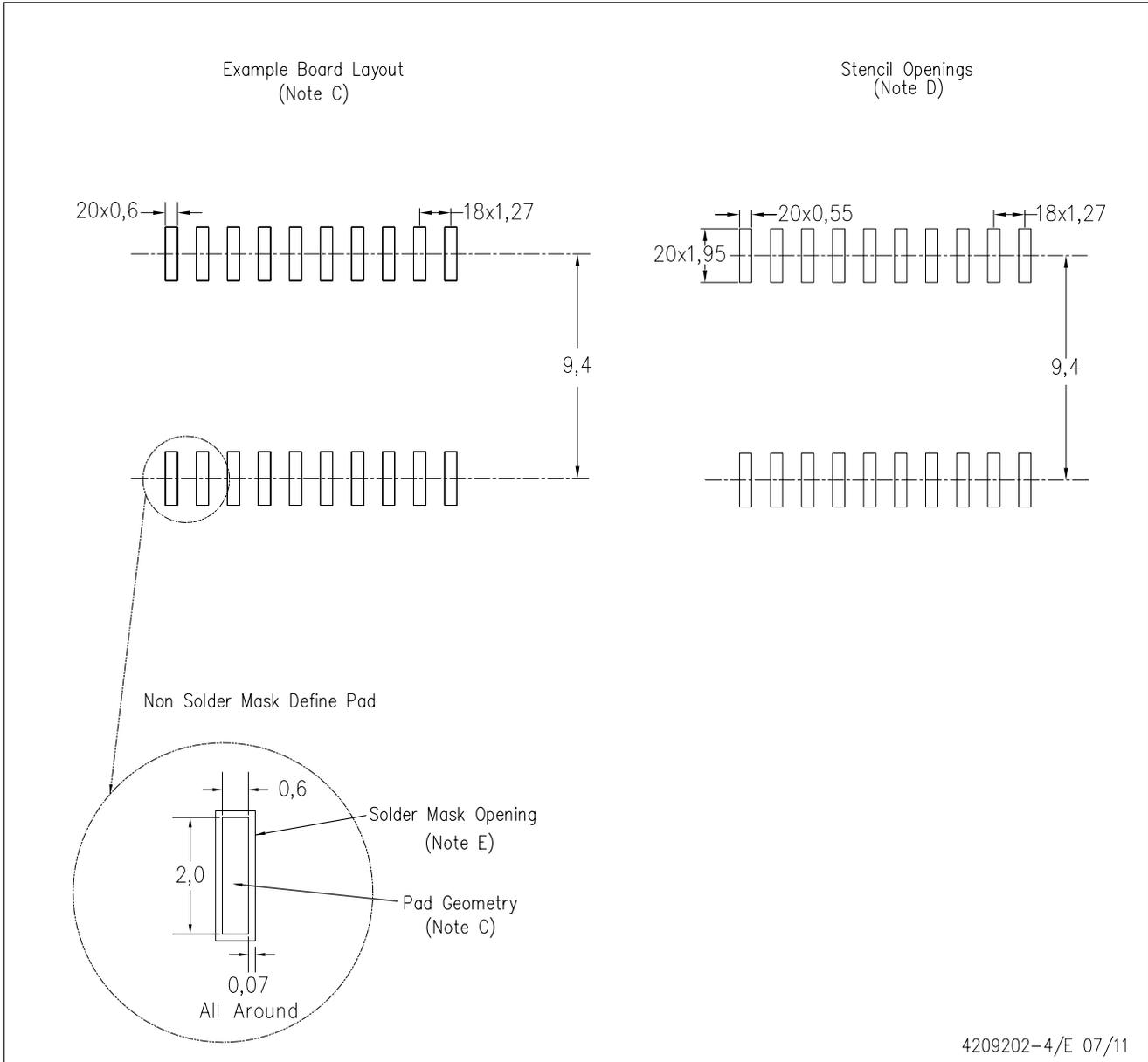
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

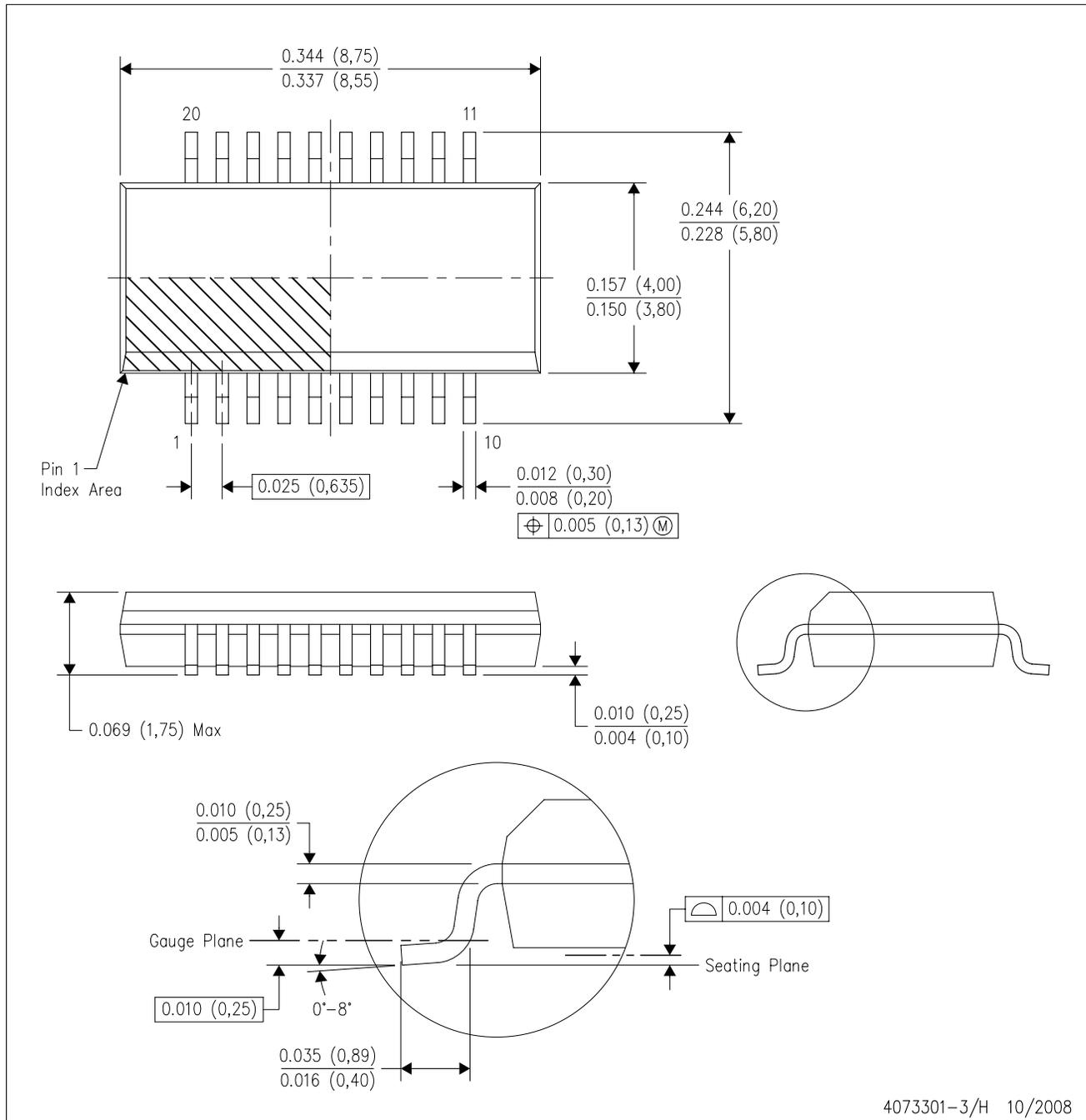


4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AD.

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