MOST® CLOCK INTERFACE

IDT5V80001

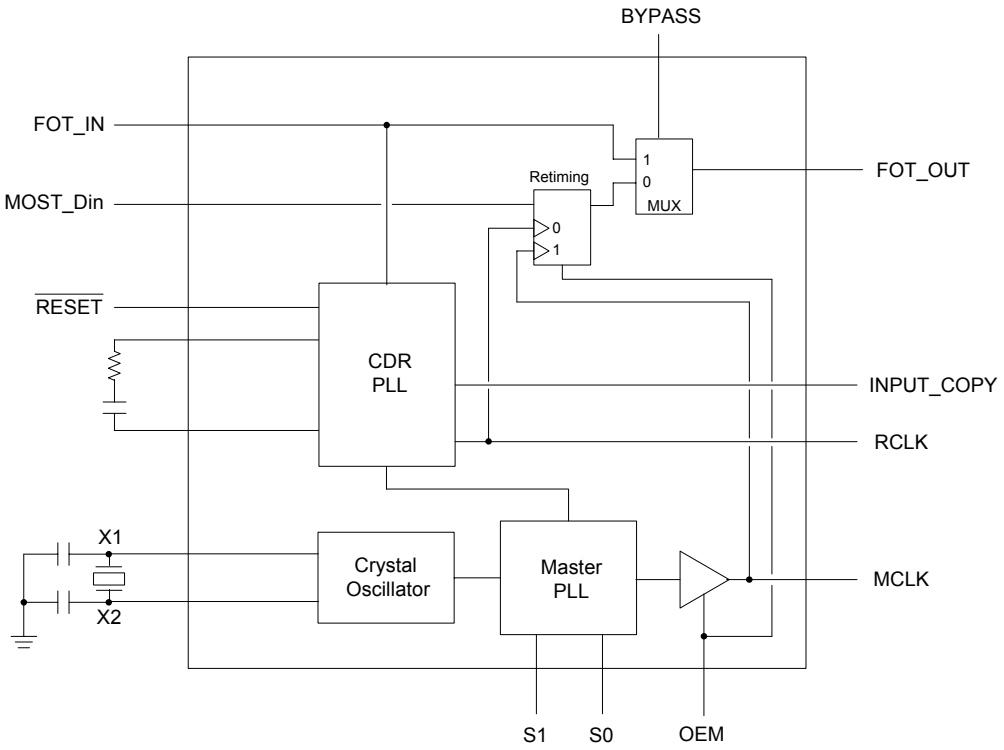
Description

The IDT5V80001 is a high performance clock interface for use in MOST® (Media Oriented Systems Transport) enabled systems. It can be used in two modes: generating a master clock for the ring, or performing clock/data recovery in a slave node.

Features

- Packaged in 20-pin TSSOP
- -40 to +85°C temperature range (industrial)
- Compliant to AEC Q100
- Operating voltage of 3.3 V
- 5 volt tolerant input for FOT
- Low jitter generation
- Power-down tri-state mode
- Advanced, low-power CMOS process

Block Diagram



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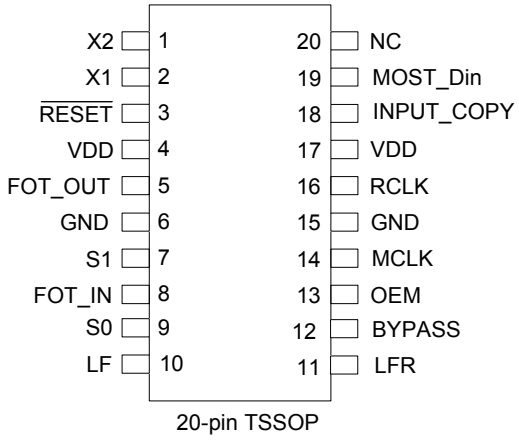
Pin Assignment



20-pin TSSOP

Frequency Selection Tables

S1	S0	Operating Frequency (RCLK)	Mode	Sampling Frequency
0	0	45.1584 MHz	MOST 25	44.1 kHz
0	1	49.152 MHz	MOST 25	48 kHz
1	0	90.3168 MHz	MOST 50	44.1 kHz
1	1	98.304 MHz	MOST 50	48 kHz

OEM	MCLK Output	Source for Retiming Block
0	LOW	RCLK (slave node)
1	Running	MCLK (master node)

OEM	Node	Bypass	FOT_OUT
0	Slave	0	Retimed (RCLK) MOST_Din*
		1	FOT_IN
1	Master	0	Retimed (MCLK) MOST_Din
		1	FOT_IN

* FOT_IN must be present in order to generate RCLK and Retimed (RCLK) MOST_Din.

Pin Descriptions

Pin	Name	Type	Pin Description
1	X2	Input	Connect to 21.504 MHz crystal.
2	X1	Input	Connect to 21.504 MHz crystal.
3	$\overline{\text{RESET}}$	Input	Low to reset CDR PLL. Internal pull-up resistor.
4	VDD	Power	Connect to 3.3 V supply.
5	FOT_OUT	Output	Output for fiber optic MOST transceiver. 3.3 V LVTTL levels.
6	GND	Power	Connect to ground.
7	S1	Input	Frequency select input pin. See table above. No internal pull-up or pull-down resistor.
8	FOT_IN	Input	Input to device from fiber optic MOST transceiver. 3.3 V LVTTL levels, 5 V tolerant.
9	S0	Input	Frequency select input pin. See table above. No internal pull-up or pull-down resistor.

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Pin	Name	Type	Pin Description
10	LF	Input	Loop filter connection for CDR PLL.
11	LFR	Input	Loop filter return. Connected to ground internally.
12	BYPASS	Input	MUX control to bypass CDR PLL. Active high. No internal pull-up or pull-down resistor.
13	OEM	Input	High to enable MCLK. See table above. No internal pull-up or pull-down resistor.
14	MCLK	Output	Master clock output. Clean clock derived from crystal. See table above. Weak pull-down when OEM = 0.
15	GND	Power	Connect to ground.
16	RCLK	Output	Recovered clock out. See table above.
17	VDD	Power	Connect to 3.3 V supply.
18	INPUT_COPY	Output	Retimed copy of FOT_IN input.
19	MOST_Din	Input	MOST data input.
20	NC	—	No Connect. Do not connect this pin to anything.

Operation

The IDT5V80001 performs clock generation and recovery for either a master or slave node in a MOST ring. It provides a interface between a controller (typically implemented in an ASIC or FPGA) and the fiber optic transceiver (FOT).

When used in a Master node (OEM = High), the Master PLL synthesizes a frequency of twice the MOST data rate as the MCLK output, and also reclocks the data from the controller that is input on the FOT_IN pin to the INPUT_COPY output. The output data on FOT_OUT is the MOST_Din data retimed to MCLK if BYPASS is driven low, or the FOT_IN data if BYPASS is driven high. Simultaneously, the device recovers the clock from data on the FOT_IN pin and outputs a 2x clock on RCLK.

In a slave node, OEM is set low and the MCLK output is disabled. Data from the controller (FOT_IN) is retimed using the recovered clock and output on the INPUT_COPY. If BYPASS is driven high, the controller data (FOT_IN) is also transmitted on the FOT_OUT output but is not retimed to RCLK. If BYPASS is driven low, the MOST_Din data is retimed and transmitted on the FOT_OUT output.

To recover the clock from the data stream, the two PLLs work together. The lock sequence from power on is:

1. Crystal oscillator starts and stabilizes.
2. Master (frequency synthesis) PLL starts and locks to the crystal.
3. CDR PLL starts and locks to the master PLL to obtain a frequency operation point.
4. Activity is detected on FOT_IN.
5. CDR PLL phase-locks to incoming data.

Extreme conditions, such as electrical transients, phase steps or brief dropouts on the FOT_IN pin may cause the CDR PLL to unlock. If this occurs and the controller begins to experience data errors, it should set $\overline{\text{RESET}}$ low for at least 50 ns to restart the data lock sequence from step 3.

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External Components

The IDT5V80001 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between each VDD pins and the ground plane, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB.

Crystal

The IDT5V80001 requires a 21.504 MHz parallel resonant crystal. Recommended devices are:

Manufacturer	Package	Part #
Abracon	5x7 mm ceramic	AAH-363-21.504MHz
NDK	3.2x5 mm ceramic	EXS00A-CG00294

Crystal Load Capacitors

The device crystal connections should include pads for capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance.

The value (in pF) of these crystal caps should equal (C_L -12 pF)*2. In this equation, C_L= crystal load capacitance in pF. For the specified 16 pF load capacitance, each crystal capacitor would be 8 pF [(16-12) x 2 = 8].

External Loop Filter

An external loop filter is required for operation of the CDR PLL. Recommended components are:

R_S = 1210 Ω, 1% tolerance
C_S = 10 nF, use capacitor with a non-piezoelectric dielectric. Recommended type is Panasonic ECH-U01103GX5 or equivalent.

Series Termination Resistor

Termination should be used on the FOT_OUT, MCLK, RCLK, and INPUT_COPY output (pins 5, 14, 16, and 18 respectively). To series terminate a 50 Ω trace (a commonly used trace impedance) place a 33 Ω resistor in series with the clock line, as close to the clock output pin as possible.

The nominal impedance of the clock output is 20 Ω

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

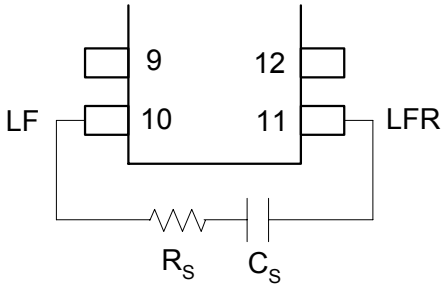
2) The external crystal should be mounted just next to the device with short traces.

3) The external loop filter components should be mounted close to the IDT5V80001 and away from digital signals, switching power supply components, and other sources of noise.

4) To minimize EMI, 33 Ω series termination resistors should be placed close to the clock outputs.

5) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDT5V80001. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

External Loop Filter



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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V80001. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
Inputs and Outputs	-0.5 V to VDD+0.5 V
Input (FOT_IN only)	7 V
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured with respect to GND)	+3.0	+3.3V	+3.6	V
Power Supply Ramp Time			4	ms

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DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	IDD	No load, F_{RCLK} = 49.152 MHz		35		mA
High Level Input Voltage	V_{IH}	FOT_IN, MOST_Din	2		5.5	V
		$\overline{RESET}$, BYPASS, OEM, S0, S1	2.0		VDD+0.3	
Low Level Input Voltage	V_{IL}	FOT_IN, MOST_Din	-0.3		0.8	V
		$\overline{RESET}$, BYPASS, OEM, S0, S1	-0.3		0.8	
High Level Output Voltage	V_{OH}	FOT_OUT only, I_{OH} = -2 mA	2.4			V
		MCLK, RCLK, INPUT_COPY I_{OH} = -100 µA	VDD-0.2			
Low Level Output Voltage	V_{OL}	FOT_OUT only, I_{OH} = 2 mA			0.4	V
		MCLK, RCLK, INPUT_COPY I_{OH} = 100 µA			0.2	
Short Circuit Current	I_{OS}	FOT_OUT		35		mA
Input Capacitance	C_{IN}	FOT_IN, MOST_Din, $\overline{RESET}$, BYPASS, OEM, S0, S1		5	10	pF
Nominal Output Impedance	Z_{OUT}	FOT_OUT, MCLK, RCLK, INPUT_COPY		20		Ω
On-Chip Pull-up or Pull-down Resistor	R_P	$\overline{RESET}$		500		kΩ

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Timing Requirements

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Crystal Frequency	F_{IN}			21.504		MHz
Input Rise Time	t_R	S1=0, S0=0 (See Fig. 1)			10.0	ns
		S1=0, S0=1 (See Fig. 1)			9.2	
		S1=1, S0=0 (See Fig. 1)			5.0	
		S1=1, S0=1 (See Fig. 1)			4.6	
Input Fall Time	t_F	S1=0, S0=0 (See Fig. 1)			10.0	ns
		S1=0, S0=1 (See Fig. 1)			9.2	
		S1=1, S0=0 (See Fig. 1)			5.0	
		S1=1, S0=1 (See Fig. 1)			4.6	
Input Pulse Width Variation (FOT_IN and MOST_Din)	t_{PWV}	S1=0, S0=0 (See Fig. 2)	16.4		31.1	ns
		S1=0, S0=1 (See Fig. 2)	15.1		28.5	
		S1=1, S0=0 (See Fig. 2)	8.2		15.6	
		S1=1, S0=1 (See Fig. 2)	7.5		14.3	
Average Input Pulse Width Distortion (FOT_IN and MOST_Din)	t_{APWD}	S1=0, S0=0 (See Fig. 2)	-3.4		+7.0	ns
		S1=0, S0=1 (See Fig. 2)	-3.1		+6.5	
		S1=1, S0=0 (See Fig. 2)	-1.7		+3.5	
		S1=1, S0=1 (See Fig. 2)	-1.6		+3.3	
One-Sigma Data Dependent Jitter (FOT_IN)	t_{DDJ}	S1=0, S0=0 (See Fig. 3)	0		3.4	ns
		S1=0, S0=1 (See Fig. 3)	0		3.1	
		S1=1, S0=0 (See Fig. 3)	0		1.7	
		S1=1, S0=1 (See Fig. 3)	0		1.6	
One-Sigma Uncorrelated Jitter	t_{UJ}	S1=0, S0=0 (See Fig. 4)	0		1000	ps
		S1=0, S0=1 (See Fig. 4)	0		920	
		S1=1, S0=0 (See Fig. 4)	0		500	
		S1=1, S0=1 (See Fig. 4)	0		460	
CDR Reset Time	t_{RESET}	(see Fig. 5)	50			ns

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Timing Diagrams

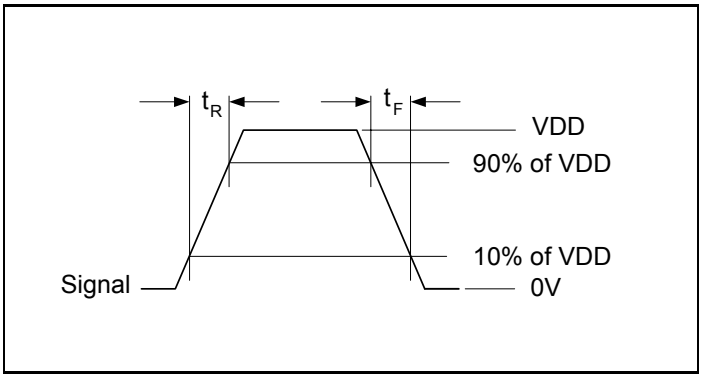

Figure 1: Rise and Fall Time Definitions

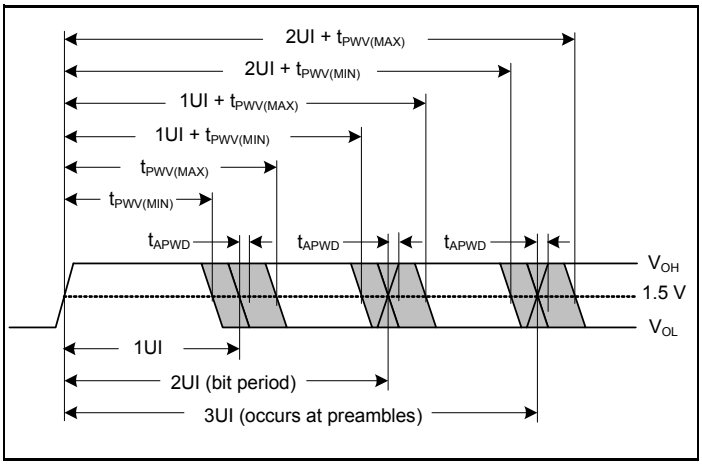

Figure 2: Pulse Width Variation and Average Pulse Width Distortion

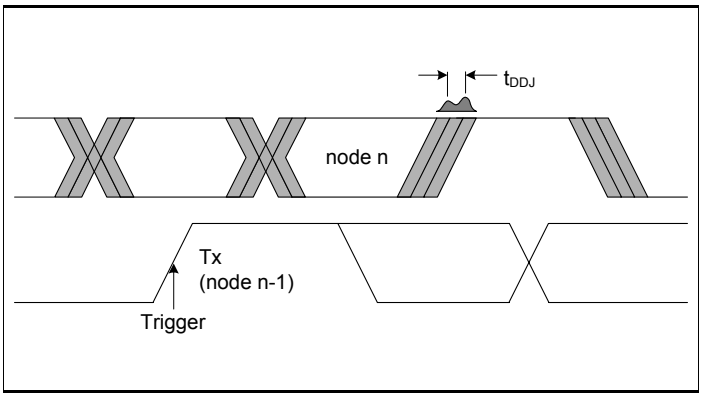

Figure 3: Data Dependent Jitter

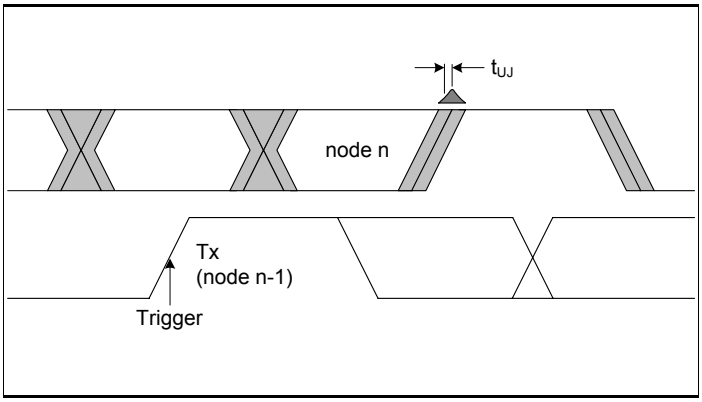

Figure 4: Uncorrelated Jitter

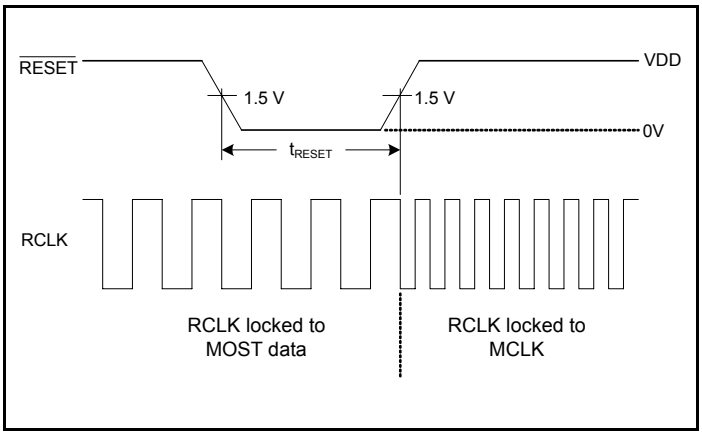

Figure 5: $\overline{\text{RESET}}$ Timing Definition

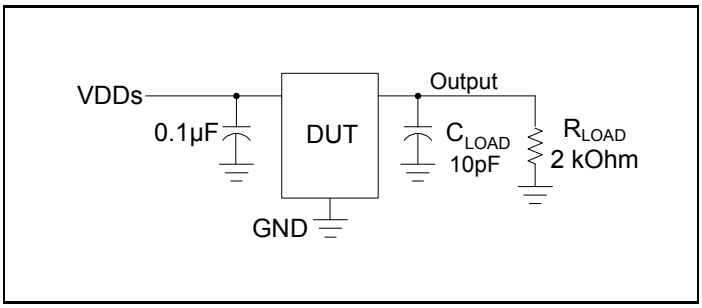

Figure 6: Test and Measurement Setup

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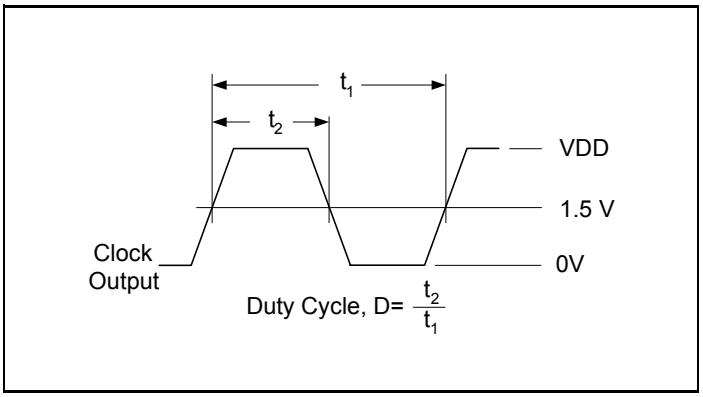

Figure 7: Duty Cycle Definitions

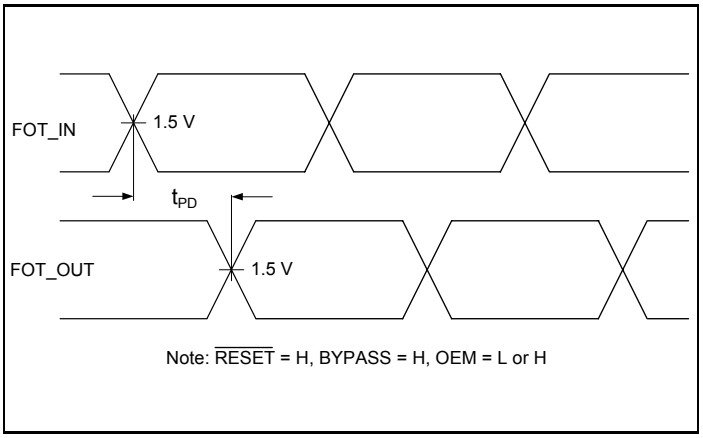

Figure 9: Propagation Delay

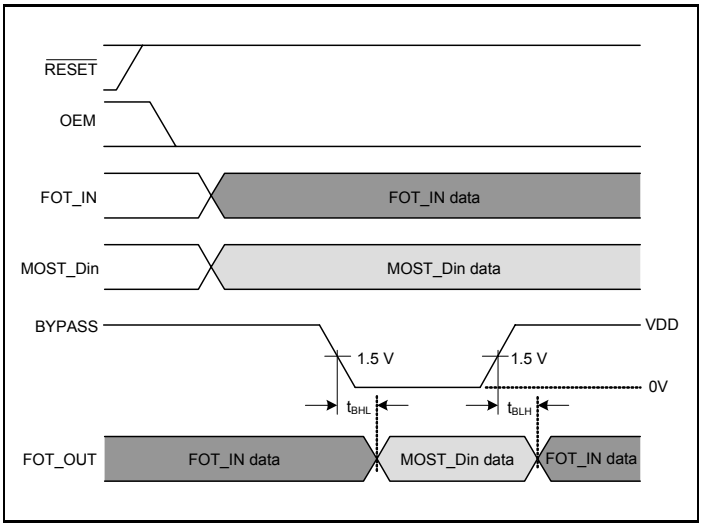

Figure 11: BYPASS Timing Definition

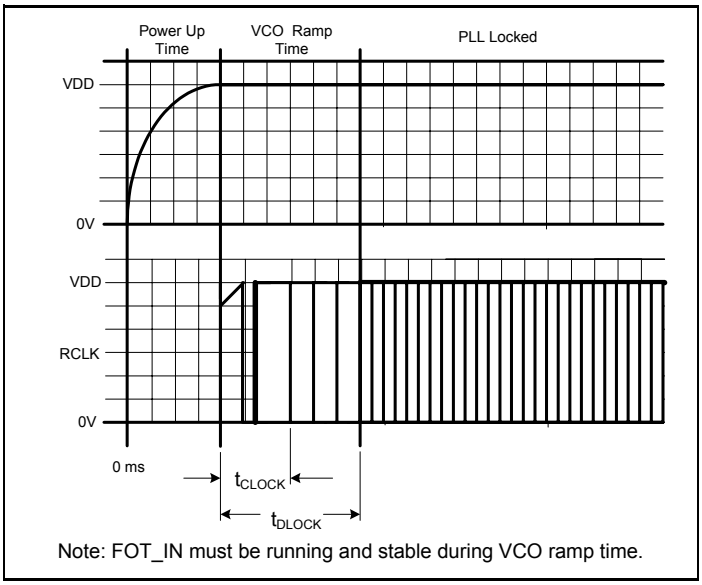

Figure 8: Power Up and PLL Lock Timing

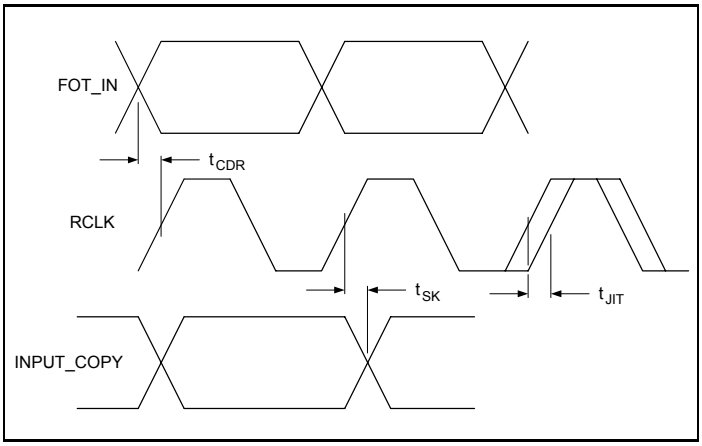

Figure 10: Clock Timing

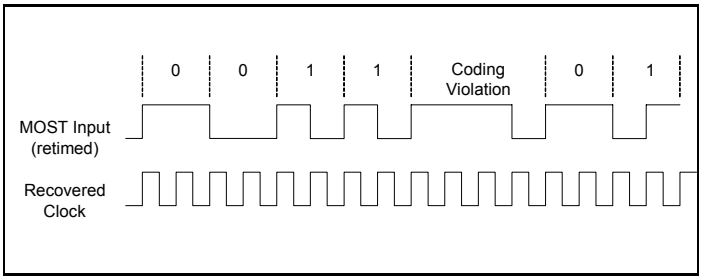

Figure 12: MOST Data–Clock Example

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AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Crystal Frequency	F_{IN}			21.504		MHz
Output Frequency Error		Due to frequency synthesis		0		ppm
Output Clock Duty Cycle	D	Figures 6 and 7	45	50	55	%
Output Rise Time	t_R	S1=0, S0=0 (See Fig. 1)			5.0	ns
		S1=0, S0=1 (See Fig. 1)			4.6	
		S1=1, S0=0 (See Fig. 1)			2.5	
		S1=1, S0=1 (See Fig. 1)			2.3	
Output Fall Time	t_F	S1=0, S0=0 (See Fig. 1)			5.0	ns
		S1=0, S0=1 (See Fig. 1)			4.6	
		S1=1, S0=0 (See Fig. 1)			2.5	
		S1=1, S0=1 (See Fig. 1)			2.3	
Output Pulse Width Variation (FOT_OUT)	t_{PWV}	S1=0, S0=0 (See Fig. 2)	21.2		23.1	ns
		S1=0, S0=1 (See Fig. 2)	19.5		21.2	
		S1=1, S0=0 (See Fig. 2)	10.6		11.5	
		S1=1, S0=1 (See Fig. 2)	9.8		10.6	
Average Output Pulse Width Distortion (FOT_OUT)	t_{APWD}	S1=0, S0=0 (See Fig. 2)	-500		+500	ps
		S1=0, S0=1 (See Fig. 2)	-460		+460	
		S1=1, S0=0 (See Fig. 2)	-250		+250	
		S1=1, S0=1 (See Fig. 2)	-230		+230	
One-Sigma Data dependent Jitter (RCLK)	t_{DDJ}	S1=0, S0=0 (See Fig. 3)	0		220	ps
		S1=0, S0=1 (See Fig. 3)	0		200	
		S1=1, S0=0 (See Fig. 3)	0		110	
		S1=1, S0=1 (See Fig. 3)	0		100	
One-Sigma Uncorrelated Jitter (RCLK)	t_{UJ}	S1=0, S0=0 (See Fig. 4)	0		95	ps
		S1=0, S0=1 (See Fig. 4)	0		90	
		S1=1, S0=0 (See Fig. 4)	0		45	
		S1=1, S0=1 (See Fig. 4)	0		45	
Power-up Time	t_{CLOCK}	PLL lock-time from 90% VDD to RCLK = MCLK, (see Fig. 8)			200	µs
	t_{DLOCK}	PLL lock-time from beginning of FOT_IN input to stable RCLK output, (see Fig. 8)			400	µs
Propagation Delay (FOT_IN to FOT_OUT)	t_{PD}	(see Fig. 9)	3	4	5	ns
Propagation Delay (FOT_IN to RCLK)	t_{CDR}	(see Fig. 10)	TBD	TBD	TBD	ns
Skew, recovered clock to retimed input	t_{SK}	(see Fig. 10)	-250	0	+250	ps
One-Sigma Clock Period Jitter		MCLK	0		50	ps

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
RCLK Peak-to-peak Jitter with respect to FOT_IN	t_{JIT}		-500	0	+500	ps
BYPASS High-to-Low to FOT_OUT	t_{BHL}	(see Fig. 11)	TBD		TBD	ns
BYPASS Low-to-High to FOT_OUT	t_{BLH}	(see Fig. 11)	TBD		TBD	ns

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		93		°C/W
	θ_{JA}	1 m/s air flow		78		°C/W
	θ_{JA}	3 m/s air flow		65		°C/W
Thermal Resistance Junction to Case	θ_{JC}			20		°C/W

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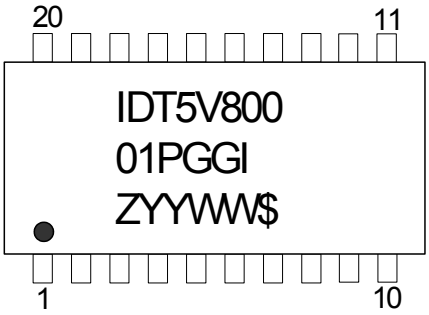
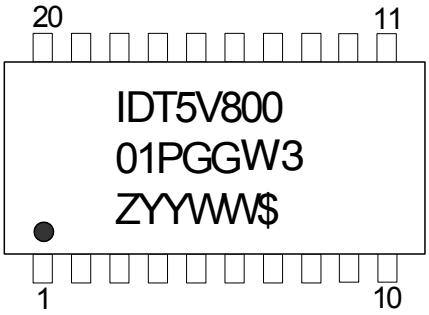
Marking Diagrams





Notes:
1. “Z” is the device step (1 to 2 characters).
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “$” is the assembly mark code.
4. “G” after the two-letter package code designates RoHS compliant package.
5. “I” at the end of part number indicates industrial temperature range.
6. ‘W3’ denotes automotive grade.
7. Bottom marking: country of origin if not USA.

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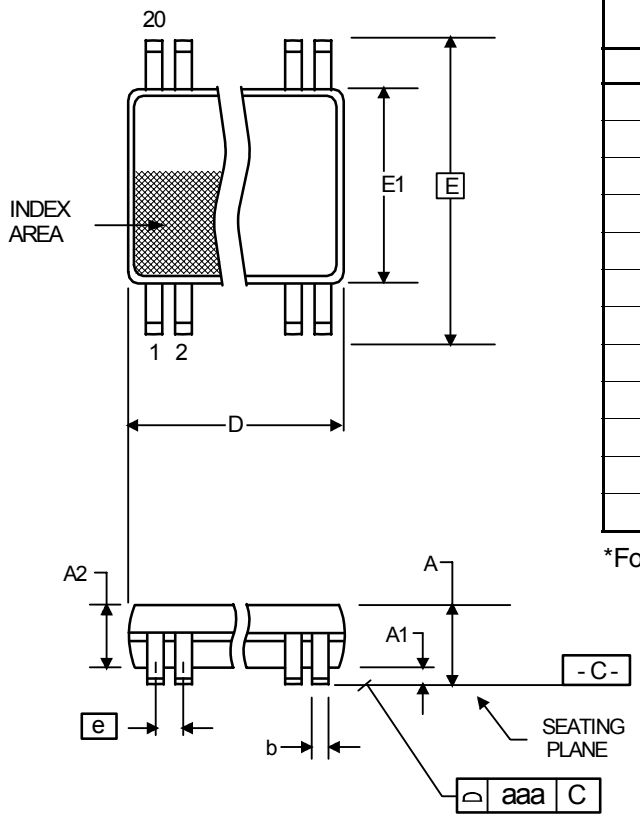
Package Outline and Package Dimensions (20-pin TSSOP, 4.4mm Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	6.40	6.60	0.252	0.260
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5V80001PGGI	see page 8	Tubes	20-pin TSSOP	-40 to +85° C
5V80001PGGI8		Tape and Reel	20-pin TSSOP	-40 to +85° C
5V80001PGGW3	see page 8	Tubes	20-pin TSSOP	-40 to +85° C
5V80001PGGW38		Tape and Reel	20-pin TSSOP	-40 to +85° C

Parts that are ordered with a "G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant. 'W3' denotes automotive grade.

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Revision History

Rev.	Originator	Date	Description of Change
A	J. Gazda	08/29/06	Preliminary datasheet.
B	J. Gazda	09/19/06	Changed block diagram and pinout;
C	J. Gazda	09/25/06	Changed from 16-pin TSSOP to 20-pin TSSOP; added timing diagrams; changed pinout and block diagrams.
D	J. Gazda	09/27/06	New block diagram; changed pinout; added Propagation Delay, Skew, and Clock Jitter specs; changed High/Low Input/Output level specs.
E	J. Gazda	11/02/06	Changed temperature rating from -40/+85 to -40/+105 °C; added “Mode” and “Sampling Frequency” to Frequency Selection Table.
F	J. Gazda	12/14/06	Added “Operation” section; added “External Loop Filter” diagram; added RESET# pin; various modifications to “External Components” text.
G	J. Gazda	02/15/07	Added Feature bullet of “5 V tolerant input for FOT”; add crystal caps and ground to block diagram; added “Weak pull-down when OEM=0” statement to MCLK pin description.
H	J. Gazda	03/22/07	Added NDK crystal part number; changed “MCLK” to “RCLK” in the conditions for “Data to clock jitter” spec.
J	J. Gazda	05/31/07	Removed C_P reference on External Loop Filter descriptions; removed one capacitor from “CDR PLL” in Block Diagram.
K	J. Gazda	06/22/07	Reversed ’1’ and ‘0’ on the MUX in the block diagram; removed the bar from “BYPASS”; added the text “No pull-up” to pin descriptions 7, 9, 12, and 13; removed “Data to clock jitter” spec from AC char table.
L	J. Gazda	10/09/07	Removed “Lock” pin.
M	T. Nana	12/17/07	Updates to timing diagrams; added “Timing Requiremnets” table; updates to pin descriptions; multiple updates to AC/DC char tables; added Figure 7.
N	T. Nana	12/26/07	Updates to Block Diagram and Timing diagrams; added new “Operation” information; added another OEM table for BYPASS and FOT_OUT; updates to AC/DC char tables and “Timing Requirementts” table; added “Reset Timing Definition” (Fig. 8) and “BYPASS Timing Definition” (Fig. 9) diagrams.
P	T. Nana	01/08/08	Updates to DC Electrical Char table; One-Sigma Jitter specs added to “Timing Requirements” table; updates to Timing Diagrams; added jitter and propagation delay timing diagrams; added One-Sigma Jitter specs to AC Electrical Char table;
Q	T. Nana	02/06/08	Removed OEM and MUX from Block Diagram; updates to "Operation" text; updated "Propagation Delay" diagram; added additional “Propagation Delay” spec to AC char table.
R		11/14/08	Moved from Preliminary to Released.
S	D.L.	08/31/09	Added automotive grade ordering info and marking diagram

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