12-Bit, 6 GSPS, JESD204B/JESD204C Dual ADC

FEATURES

- Flexible reconfigurable common platform design
  - Supports single, dual, and quad band per channel
  - Datapaths and DSP blocks are fully bypassable
  - On-chip PLL with multichip synchronization
  - External RFCLK input option for off-chip PLL
- Support clock input frequencies up to 12 GHz
  - Maximum ADC sample rate up to 6 GSPS
  - Useable analog bandwidth to 8 GHz
- Maximum data rate up to 6 GSPS using JESD204C
- Noise density: −153 dBFS/Hz
- ADC AC performance at 6 GSPS, input at 2.7 GHz, −1 dBFS
  - Full-scale sine wave input voltage: 1.475 V p-p
  - Noise figure: 25.3 dB
  - HD2: −70 dBFS
  - HD3: −68 dBFS
  - Worst other (excluding HD2 and HD3): −84 dBFS
- Versatile digital features
  - Selectable decimation filters
  - Configurable DDC
    - 8 fine complex DDCs and 4 coarse complex DDCs
    - 48-bit NCO per DDC
    - Option to bypass fine and coarse DDC
  - Programmable 192-tap PFIR filter for receive equalization
- Supports 4 different profile settings loaded via the GPIOx pins
- Programmable delay per datapath
  - Receive AGC support
    - Fast detect with low latency for fast AGC control
  - Signal monitor for slow AGC control
  - Dedicated AGC support pins
- Auxiliary features
  - Fast frequency hopping
  - ADC clock driver with selectable divide ratios
  - On-chip temperature monitoring unit
  - Flexible GPIOx pins
- SERDES JESD204B/JESD204C interface, 8 lanes up to 24.75 Gbps
  - 8 lanes JESD204B/JESD204C transmitter (JTx)
  - JESD204B compliance with the maximum 15.5 Gbps
  - JESD204C compliance with the maximum 24.75 Gbps
  - Supports real or complex digital data (8 bit, 12 bit, 16 bit, or 24 bit)
  - Outline Dimensions

APPLICATIONS

- Wireless communications infrastructure
- Microwave point to point, E-band, and 5G mmWave
- Broadband communications systems, satellite communications
- DOCSIS 3.1 and 4.0 CMTS
- Electronic warfare
- Electronic test and measurement systems

GENERAL DESCRIPTION

The AD9207 is a dual, 12-bit, 6 GSPS analog-to-digital converter (ADC). The ADC input features an on-chip wideband buffer with overload protection. This device is designed to support applications capable of direct sampling wideband signals up to 8 GHz. An on-chip, low phase noise, phase-locked loop (PLL) clock synthesizer is available to generate the ADC sampling clock, which simplifies the printed circuit board (PCB) distribution of a high frequency clock signal. A clock output buffer is available to transmit the ADC sampling clock to other devices.

The dual ADC cores have code error rates (CER) better than 2×10^{-15}. Low latency fast detection and signal monitoring are available for automatic gain control (AGC) purposes. A flexible 192-tap programmable finite impulse response filter (PFIR) is available for digital filtering and/or equalization. Programmable integer and fractional delay blocks support compensation for analog delay mismatches.

The digital signal processing (DSP) block consists of two coarse digital downconverters (DDCs) and four fine DDCs per ADC pair. Each ADC can operate with one or two main DDC stages in support of multiband applications. The four additional fine DDC stages are available to support up to four bands per ADC. The 48-bit numerically controlled oscillators (NCOs) associated with each DDC support fast frequency hopping (FFH) while maintaining synchronization with up to 16 unique frequency assignments selected via the general-purpose input and output (GPIOx) pins or the serial port interface (SPI).

The AD9207 supports one or two JTx links that can be configured for either JESD204B or JESD204C subclass operation, which allows different datapath configurations for each ADC. Multidevice synchronization is supported through the SYSREF± input pins.

See the Outline Dimensions section and the Ordering Guide section for more information.

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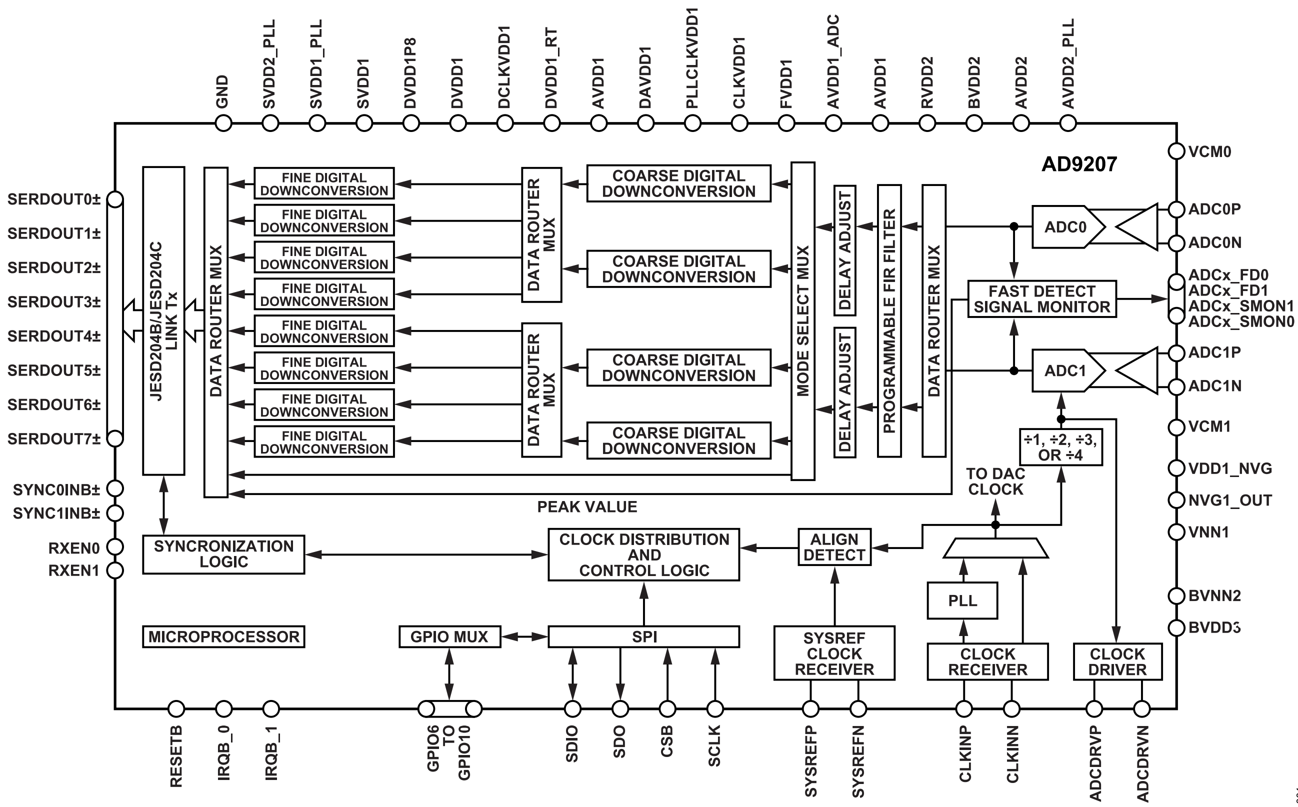
REVISION HISTORY

9/2021—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Refer to the UG-1578 user guide for more information on device initialization.

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING JUNCTION TEMPERATURE (T_J)	−40		+120	°C
ANALOG SUPPLY VOLTAGE RANGE				
AVDD2, BVDD2, and RVDD2	1.9	2.0	2.1	V
AVDD1, AVDD1_ADC, CLKVDD1, FVDD1, and VDD1_NVG1	0.95	1.0	1.05	V
DIGITAL SUPPLY VOLTAGE RANGE				
DVDD1, DVDD1_RT, DCLKVDD1, and DAVDD1	0.95	1.0	1.05	V
DVDD1P8	1.7	1.8	2.1	V
SERIALIZER/DESERIALIZER (SERDES) SUPPLY VOLTAGE RANGE				
SVDD2_PLL	1.9	2.0	2.1	V
SVDD1 and SVDD1_PLL	0.95	1.0	1.05	V

POWER CONSUMPTION

Typical at nominal supplies and maximum at 5% supplies. For the minimum and maximum values, T_J was varied between −40°C and +120°C. For the typical values, T_A = 25°C, unless otherwise noted.

ADC datapath with DDCs bypassed (no decimation) and ADC frequency (f_{ADC}) = 6 GSPS, and JESD204C mode of 19C (L = 8, M = 2, F = 1, S = 2, K = 256, E = 1, N = 16, NP = 16).

See the UG-1578 user guide for further information on the JESD204B and JESD204C mode configurations and a detailed description of the settings referenced throughout this data sheet.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		10	10.7	mA
BVDD2 (I_{BVDD2}) + RVDD2 (I_{RVDD2})	2.0 V supply		291.4	350.1	mA
AVDD2_PLL (I_{AVDD2_PLL}) + SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		44.6	55.3	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		0.7	0.9	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		8.4	14.5	mA
AVDD1 (I_{AVDD1}) + DCLKVDD1 ($I_{DCLKVDD1}$)	1.0 V supply		154.5	285.2	mA
AVDD1_ADC (I_{AVDD1_ADC})	1.0 V supply		1726	2120	mA
CLKVDD1 ($I_{CLKVDD1}$)	1.0 V supply		88.7	148.6	mA
FVDD1 (I_{FVDD1})	1.0 V supply		47.9	81.7	mA
VDD1_NVG (I_{VDD1_NVG})	1.0 V supply		290.9	379.4	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		67.6	192.3	mA
DVDD1 (I_{DVDD1})	1.0 V supply		1102.7	1977.5	mA
DVDD1_RT (I_{DVDD1_RT})	1.0 V supply		460.3	568.2	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		909.8	1323.2	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		4.9	7.1	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		1.8	3.1	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		5.6	7.8	W

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ADC DC SPECIFICATIONS

Nominal supplies with ADC setup in 6 GSPS, full bandwidth mode (all digital downconverters bypassed). For the minimum and maximum values, T_J = −40°C to +120°C, and for the typical values, T_A = 25°C, which corresponds to T_J = 80°C, unless otherwise noted.

Table 3. ADC DC Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC RESOLUTION		12			Bit
ADC ACCURACY					
No Missing Codes			Guaranteed		
Offset Error			0.04		% FSR
Offset Matching			0.03		% FSR
Gain Error			1.5		% FSR
Gain Matching			0.6		% FSR
DNL			0.32		LSB
INL			1.38		LSB
ADC ANALOG INPUTS	ADCxP and ADCxN				
Differential Input Voltage			1.475		V p-p
Full-Scale Sine Wave Input Power	Input power level resulting 0 dBFS tone level on fast Fourier transform (FFT)		3.9		dBm
Common-Mode Input Voltage (VCM_{IN})	AC-coupled, equal to voltage at VCMx for ADCx input		1		V
Differential Input Resistance			100		Ω
Differential Input Capacitance			0.4		pF
Return Loss	<2.7 GHz		−4.3		dB
	2.7 GHz to 3.8 GHz		−3.6		dB
	3.8 GHz to 5.4 GHz		−2.9		dB

CLOCK INPUTS AND OUTPUTS

For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted. For the typical values, T_A = 25°C, which corresponds to T_J = 80°C, unless otherwise noted.

Table 4. Clock Inputs and Outputs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK INPUTS	CLKINP and CLKINN				
Differential Input Power	Direct RF clock				
Minimum				0	dBm
Maximum				6	dBm
Common-Mode Voltage	AC-coupled			0.5	V
Differential Input Resistance				100	Ω
Differential Input Capacitance				0.3	pF
CLOCK OUTPUTS (ADC CLOCK DRIVER)	ADCDRVP and ADCDRVN				
Differential Output Voltage Magnitude[1]	1.5 GHz			740	mV p-p
	2.0 GHz			690	mV p-p
	3 GHz			640	mV p-p
	6 GHz			490	mV p-p
Differential Output Resistance				100	Ω
Common-Mode Voltage	AC-coupled			0.5	V

[1] Measured with a differential 100 Ω load and less than 2 mm of PCB trace from the package ball.

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CLOCK INPUT AND PHASE-LOCKED LOOP (PLL) FREQUENCY SPECIFICATIONS

For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted. For the typical values, T_A = 25°C, which corresponds to T_J = 80°C, unless otherwise noted.

Table 5. Clock Input and PLL Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK INPUTS (CLKINP AND CLKINN) FREQUENCY RANGES		25		12000	MHz
PHASE FREQUENCY DETECTOR (PFD) INPUT FREQUENCY RANGES		25		750	MHz
FREQUENCY RANGES ACCORDING TO CLOCK PATH CONFIGURATION					
Direct Clock (PLL Off)		2900		12000	MHz
PLL Reference Clock (PLL On)[1]	M divider set to divide by 1	25		750	MHz
	M divider set to divide by 2	50		1500	MHz
	M divider set to divide by 3	75		2250	MHz
	M divider set to divide by 4	100		3000	MHz
PLL VOLTAGE CONTROLLED OSCILLATOR (VCO) FREQUENCY RANGES					
VCO Output	D divider set to divide by 1	5.8		12	GHz
	D divider set to divide by 2	2.9		6	GHz
	D divider set to divide by 3	1.93333		4	GHz
	D divider set to divide by 4	1.45		3	GHz

[1] Refer to the UG-1578 user guide for information on the M divider and the D divider.

ADC SAMPLE RATE SPECIFICATIONS

Nominal supplies. For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply. For the typical values, T_A = 25°C, unless otherwise noted.

Table 6. ADC Sample Rate Specifications

Parameter	Min	Typ	Max	Unit
ADC SAMPLE RATE[1]				
Minimum			1.45	GSPS
Maximum	6			GSPS
Aperture Jitter[2]		65		fs rms

[1] Pertains to the update rate of the ADC core independent of the datapath and JESD204 mode configuration.

[2] Measured using a signal-to-noise ratio (SNR) degradation method with the DAC disabled, clock divider = 1, f_{ADC} = 6 GSPS, and input frequency (f_{IN}) = 5.55 GHz.

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JESD204B AND JESD204C INTERFACE ELECTRICAL AND SPEED SPECIFICATIONS

Nominal supplies. For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, and for the typical values, T_A = 25°C, unless otherwise noted.

Table 7. Serial Interface Rate Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B SERIAL INTERFACE RATE	Serial lane rate	1.0		15.5	Gbps
Unit Interval		64.5		1000.0	ps
JESD204C SERIAL INTERFACE RATE	Serial lane rate	6.0		24.75	Gbps
Unit Interval		40.4		166.67	ps

Table 8. JESD204 Transmitter (JTx) Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204 DATA OUTPUTS	SERDOUTx±, where x = 0 to 7				
Standards Compliance			JESD204B and JESD204C		
Differential Output Voltage	Maximum strength		675		mV p-p
Differential Termination Impedance		80	108	120	Ω
Rise Time, t_R	20% to 80% into 100 Ω load		18		ps
Fall Time, t_F	20% to 80% into 100 Ω load		18		ps
SYNCxINB± INPUTS[1]	Where x = 0 or 1				
Logic Compliance			LVDS		
Differential Input Voltage		0.24	0.7	1.9	V p-p
Input Common-Mode Voltage	DC-coupled		0.675	2	V
R_{IN} (Differential)			18		kΩ
Input Capacitance (Differential)			1		pF
SYNCxINB+ AND SYNCxINB−	CMOS input option		Refer to the CMOS Pin Specifications section		

[1] IEEE 1596.3 Standard low voltage differential signaling (LVDS) compatible.

Table 9. SYSREF Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREFP AND SYSREFN INPUTS					
Logic Compliance			LVDS/LVPECL[1]		
Differential Input Voltage			0.7	1.9	V p-p
Input Common-Mode Voltage Range	DC-coupled		0.675	2	V
Input Reference, R_{IN} (Differential)			100		Ω
Input Capacitance (Differential)			1		pF

[1] LVPECL means low voltage positive/pseudo emitter-coupled logic.

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CMOS PIN SPECIFICATIONS

For the minimum and maximum values, T_J = −40°C to +120°C, 1.7 V ≤ DVDD1P8 ≤ 2.1 V, other supplies nominal, unless otherwise noted.

Table 10.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUTS		SDIO, SCLK, CSB, RESETB, RXEN0, RXEN1, SYNC0INB±, SYNC1INB±, and GPIOx				
Logic 1 Voltage	V_{IH}		0.70 × DVDD1P8			V
Logic 0 Voltage	V_{IL}				0.3 × DVDD1P8	V
Input Resistance			40			kΩ
OUTPUTS		SDIO, SDO, GPIOx, ADCx_FDx, and ADCx_SMONx, 4 mA load				
Logic 1 Voltage	V_{OH}		DVDD1P8 − 0.45			V
Logic 0 Voltage	V_{OL}				0.45	V
INTERRUPT OUTPUTS		IRQB_0 and IRQB_1, pull-up resistor of 5 kΩ to DVDD1P8				
Logic 1 Voltage	V_{OH}		1.35			V
Logic 0 Voltage	V_{OL}				0.48	V

ADC AC SPECIFICATIONS

Nominal supplies with T_A = 25°C. Input amplitude (A_{IN}) = −1 dBFS, with full bandwidth (no decimation). For the minimum and maximum values, T_J = −40°C to +120°C. Specifications represent the average of two ADC channels. See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

Table 11.

Parameter	Min	Typ	Max	Unit
NOISE DENSITY[1]		−153		dBFS/Hz
NOISE FIGURE[2]		25.3		dB
CODE ERROR RATE		1.6×10^{-20}		Errors
SIGNAL-TO-NOISE RATIO				
f_{IN} = 450 MHz		56.7		dBFS
f_{IN} = 900 MHz		56.4		dBFS
f_{IN} = 1800 MHz		55.3		dBFS
f_{IN} = 2700 MHz	47.7	53.4		dBFS
f_{IN} = 3600 MHz		52.8		dBFS
f_{IN} = 4500 MHz		51.5		dBFS
f_{IN} = 5400 MHz		51.8		dBFS
f_{IN} = 6300 MHz		50.5		dBFS
f_{IN} = 7200 MHz		49.8		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)				
f_{IN} = 450 MHz		56.5		dBFS
f_{IN} = 900 MHz		56.3		dBFS
f_{IN} = 1800 MHz		54.8		dBFS
f_{IN} = 2700 MHz	48.3	53.0		dBFS
f_{IN} = 3600 MHz		51.6		dBFS
f_{IN} = 4500 MHz		48.7		dBFS
f_{IN} = 5400 MHz		49.1		dBFS
f_{IN} = 6300 MHz		46.6		dBFS
f_{IN} = 7200 MHz		43.7		dBFS

SPECIFICATIONS

Table 11.

Parameter	Min	Typ	Max	Unit
EFFECTIVE NUMBER OF BITS (ENOB)				
f_{IN} = 450 MHz		9.1		Bits
f_{IN} = 900 MHz		9.1		Bits
f_{IN} = 1800 MHz		8.8		Bits
f_{IN} = 2700 MHz	7.7	8.5		Bits
f_{IN} = 3600 MHz		8.3		Bits
f_{IN} = 4500 MHz		7.8		Bits
f_{IN} = 5400 MHz		7.9		Bits
f_{IN} = 6300 MHz		7.4		Bits
f_{IN} = 7200 MHz		7.0		Bits
SECOND-ORDER HARMONIC DISTORTION (HD2)				
f_{IN} = 450 MHz		−70		dBFS
f_{IN} = 900 MHz		−71		dBFS
f_{IN} = 1800 MHz		−73		dBFS
f_{IN} = 2700 MHz		−70	−56	dBFS
f_{IN} = 3600 MHz		−58		dBFS
f_{IN} = 4500 MHz		−52		dBFS
f_{IN} = 5400 MHz		−53		dBFS
f_{IN} = 6300 MHz		−49		dBFS
f_{IN} = 7200 MHz		−45		dBFS
THIRD-ORDER HARMONIC DISTORTION (HD3)				
f_{IN} = 450 MHz		−87		dBFS
f_{IN} = 900 MHz		−77		dBFS
f_{IN} = 1800 MHz		−66		dBFS
f_{IN} = 2700 MHz		−68	−61	dBFS
f_{IN} = 3600 MHz		−73		dBFS
f_{IN} = 4500 MHz		−66		dBFS
f_{IN} = 5400 MHz		−62		dBFS
f_{IN} = 6300 MHz		−62		dBFS
f_{IN} = 7200 MHz		−60		dBFS
WORST OTHER, EXCLUDING HD2 OR HD3 HARMONIC				
f_{IN} = 450 MHz		−92		dBFS
f_{IN} = 900 MHz		−93		dBFS
f_{IN} = 1800 MHz		−89		dBFS
f_{IN} = 2700 MHz		−84	−72	dBFS
f_{IN} = 3600 MHz		−82		dBFS
f_{IN} = 4500 MHz		−81		dBFS
f_{IN} = 5400 MHz		−78		dBFS
f_{IN} = 6300 MHz		−78		dBFS
f_{IN} = 7200 MHz		−75		dBFS
DIGITAL COUPLING SPUR ($f_{IN} \pm f_S/4$)				
f_{IN} = 450 MHz		−95		dBFS
f_{IN} = 900 MHz		−87		dBFS
f_{IN} = 1800 MHz		−80		dBFS
f_{IN} = 2700 MHz		−76	−72	dBFS
f_{IN} = 3600 MHz		−75		dBFS
f_{IN} = 4500 MHz		−73		dBFS
f_{IN} = 5400 MHz		−71		dBFS

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Table 11.

Parameter	Min	Typ	Max	Unit
f_{IN} = 6300 MHz		−69		dBFS
f_{IN} = 7200 MHz		−68		dBFS
TWO-TONE IMD3, INPUT AMPLITUDE 1 (A_{IN1}) = INPUT AMPLITUDE 2 (A_{IN2}) = −7 dBFS				
Input Frequency 1 (f_{IN1}) = 1775 MHz and Input Frequency 2 (f_{IN2}) = 1825 MHz		−84		dBFS
f_{IN1} = 2675 MHz, f_{IN2} = 2725 MHz		−86		dBFS
f_{IN1} = 3575 MHz, f_{IN2} = 3625 MHz		−75		dBFS
f_{IN1} = 5375 MHz, f_{IN2} = 5425 MHz		−67		dBFS
ANALOG BANDWIDTH[3]		8		GHz

[1] Noise density is measured at a low analog amplitude and/or frequency where the timing jitter does not degrade the noise floor.

[2] Noise figure is based on a nominal full-scale input power of 4.5 dBm with an input span of 1.475 V p-p and R_{IN} = 100 Ω.

[3] Analog input bandwidth is the bandwidth of operation in which the full-scale input frequency response rolls off by −3 dB based on a de-embedded model of the ADC extracted from the measured frequency response on the evaluation board. This bandwidth requires an optimized matching network to achieve this upper bandwidth.

TIMING SPECIFICATIONS

For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted.

Table 12.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SPI WRITE OPERATION						
Maximum SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$		33			MHz
SCLK Clock High	t_{PWH}	SCLK = 33 MHz	8			ns
SCLK Clock Low	t_{PWL}	SCLK = 33 MHz	8			ns
SDIO to SCLK Setup Time	t_{DS}		4			ns
SCLK to SDIO Hold Time	t_{DH}		4			ns
CSB to SCLK Setup Time	t_S		4			ns
SCLK to CSB Hold Time	t_H		4			ps
SPI READ OPERATION						
LSB First Data Format						
Maximum SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$		33			MHz
SCLK Clock High	t_{PWH}		8			ns
SCLK Clock Low	t_{PWL}		8			ns
MSB First Data Format						
Maximum SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$		15			MHz
SCLK Clock High	t_{PWH}		30			ns
SCLK Clock Low	t_{PWL}		30			ns
SDIO to SCLK Setup Time	t_{DS}		4			ns
SCLK to SDIO Hold Time	t_{DH}		4			ns
CSB to SCLK Setup Time	t_S		4			ns
SCLK to SDIO Data Valid Time	t_{DV}		20			ns
SCLK to SDO Data Valid Time	t_{DV_SDO}		20			ns
CSB to SDIO Output Valid to High-Z	t_Z		20			ns
CSB to SDO Output Valid to High-Z	t_{Z_SDO}		20			ns
RESETB		Minimum hold time to trigger a device reset	40			ns

SPECIFICATIONS

Timing Diagrams

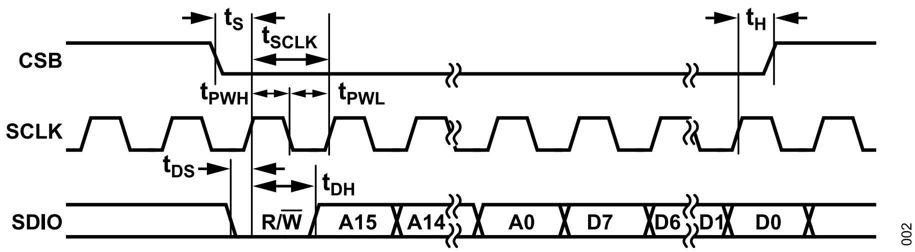


Figure 1. Timing Diagram for 3-Wire Write Operation

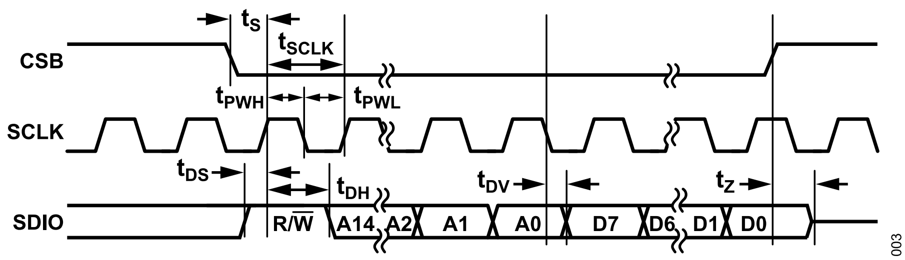


Figure 2. Timing Diagram for 3-Wire Read Operation

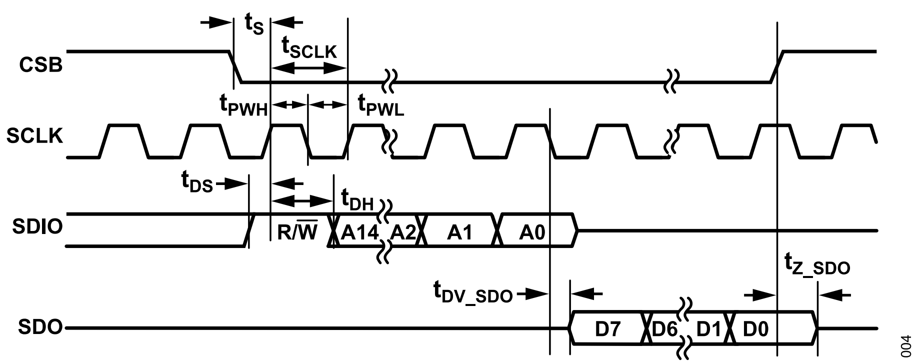


Figure 3. Timing Diagram for 4-Wire Read Operation

ABSOLUTE MAXIMUM RATINGS

Table 13.

Parameter	Rating
ISET, TDP, TDN	−0.3 V to AVDD2 + 0.3 V
VCO_COARSE, VCO_FINE, VCO_VCM, and VCO_VREG	−0.3 V to AVDD2_PLL + 0.3 V
Rx Input Power (ADC0P, ADC0N, ADC1P, and ADC1N)[1]	22 dBm
VCM0 and VCM1	−0.3 V to RVDD2 + 0.3 V
CLKINP and CLKINN	−0.2 V to PLLCLKVDD1 + 0.2 V
ADCDRVN and ADCDRVP	−0.2 V to CLKVDD1 + 0.2 V
SERDOUTx±	−0.2 V to SVDD1 + 0.2 V
SYSREFP, SYSREFN, and SYNCxINB±	−0.2 V to +2.5 V
RESETB, RXENx, IRQB_x, CSB, SCLK, SDIO, SDO, TMU_REFN, TMU_REFP, ADCx_SMON0, ADCx_SMON1, ADCx_FD0, ADCx_FD1, and GPIOx	−0.3 V to DVDD1P8 + 0.3 V
AVDD2, AVDD2_PLL, BVDD2, RVDD2, SVDD2_PLL, and DVDD1P8	−0.3 V to +2.2 V
PLLCLKVDD1, AVDD1, AVDD1_ADC, CLKVDD1, FVDD1, DAVDD1, DVDD1_RT, DCLKVDD1, SVDD1, and SVDD1_PLL	−0.2 V to +1.2 V
VNN1	−1.1 V to +0.2 V
Temperature	
Junction (T_J)[2]	120°C
Storage Range	−40°C to +150°C

1 Tested continuously for 1000 hours with f_{IN} = 4.7 GHz pulsed and continuous tone at maximum allowed T_J. Refer to the UG-1578 user guide, for more information.

2 Tested continuously for 1000 hours with f_{IN} = 4.7 GHz pulsed and continuous tone at maximum allowed T_J. Refer to the UG-1578 user guide, for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. The use of appropriate thermal management techniques is recommended to ensure that the maximum T_J does not exceed the limits shown in Table 13.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC_TOP} is the junction to case, thermal resistance.

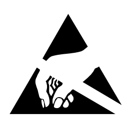
θ_{JB} is the junction to board, thermal resistance.

Table 14. Simulated Thermal Resistance[1]

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_TOP}	θ_{JB}	Unit
JEDEC 2s2p Board	0.0	14.9	0.7	1.8	°C/W

1 Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD51-12 with the device power equal to 9 W.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

AD9207
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	AVDD2	GND	GND	NC	NC	GND	GND	ADC0N	ADC0P	GND	SYNC1INB–	SYNC0INB–	SERDOUT0–	SERDOUT0+	SVDD1	GND	GND
B	DNC	GND	GND	GND	GND	GND	DNC	VCM0	GND	GND	RVDD2	SYNC1INB+	SYNC0INB+	GND	GND	SVDD1	SERDOUT7–	SERDOUT7+
C	DNC	GND	ADCDRVN	ADCDRVP	GND	GND	GND	GND	BVNN2	BVDD3	GND	RESETB	DVDD1P8	SERDOUT1–	SERDOUT1+	SVDD1	GND	GND
D	GND	AVDD1	AVDD1	AVDD1	GND	FVDD1	BVDD2	VNN1	GND	VDD1_NVG	ADC0_SMON1	ADC0_SMON0	RXEN1	GND	GND	SVDD1	SERDOUT6–	SERDOUT6+
E	GND	AVDD2	AVDD1	GND	DAVDD1	GND	BVDD2	VNN1	NVG1_OUT	VNN1	ADC0_FD1	ADC0_FD0	RXEN0	SERDOUT2–	SERDOUT2+	SVDD1	GND	GND
F	DNC	GND	AVDD1	GND	DAVDD1	GND	GND	GND	DVDD1P8	DVDD1	ADC1_SMON1	ADC1_SMON0	SDIO	GND	GND	SVDD1	SERDOUT5–	SERDOUT5+
G	DNC	GND	GND	GND	GND	CLKVDD1	AVDD1_ADC	AVDD1_ADC	TMU_REFN	TMU_REFP	ADC1_FD1	ADC1_FD0	CSB	SERDOUT3–	SERDOUT3+	SVDD1	GND	GND
H	GND	AVDD2	ISET	DNC	GND	GND	GND	GND	DVDD1	GND	DVDD1	GND	SCLK	GND	GND	SVDD1	SERDOUT4–	SERDOUT4+
J	CLKINP	GND	VCO_FINE	VCO_COARSE	PLLCLKVDD1	DVDD1_RT	DVDD1_RT	GND	DVDD1	GND	DVDD1	GND	SDO	GND	GND	SVDD1_PLL	GND	GND
K	CLKINN	GND	VCO_VREG	VCO_VCM	DCLKVDD1	DVDD1_RT	DVDD1_RT	GND	DVDD1	GND	DVDD1	GND	GPIO9	GND	SVDD2_PLL	SVDD1_PLL	GND	GND
L	GND	AVDD2	AVDD2_PLL	DNC	GND	GND	GND	GND	DVDD1	GND	DVDD1	GND	GPIO8	GND	DNC	DNC	DNC	DNC
M	DNC	GND	GND	GND	GND	CLKVDD1	AVDD1_ADC	AVDD1_ADC	DVDD1	GND	DNC	DNC	GPIO7	DNC	DNC	SVDD1	GND	GND
N	DNC	GND	AVDD1	GND	DAVDD1	GND	GND	GND	TDP	TDN	DNC	DNC	GPIO6	GND	GND	SVDD1	DNC	DNC
P	GND	AVDD2	AVDD1	GND	DAVDD1	GND	BVDD2	VNN1	NVG1_OUT	VNN1	DNC	IRQB_0	DNC	DNC	DNC	SVDD1	GND	GND
R	GND	AVDD1	AVDD1	AVDD1	GND	FVDD1	BVDD2	VNN1	GND	VDD1_NVG	DNC	IRQB_1	DNC	GND	GND	SVDD1	DNC	DNC
T	DNC	GND	SYSREFN	SYSREFP	GND	GND	GND	GND	BVNN2	BVDD3	GND	GPIO10	DVDD1P8	DNC	DNC	SVDD1	GND	GND
U	DNC	GND	GND	GND	GND	GND	DNC	VCM1	GND	GND	RVDD2	DNC	DNC	GND	GND	SVDD1	DNC	DNC
V	GND	AVDD2	GND	GND	NC	NC	GND	GND	ADC1N	ADC1P	GND	DNC	DNC	DNC	DNC	SVDD1	GND	GND

GND ANALOG GROUND; GND DIGITAL GROUND; GND SERDES GROUND

005

Figure 4. 324-Ball Pin Configuration

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 15. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
POWER SUPPLIES			
A2, E2, H2, L2, P2, V2	AVDD2	Input	Analog 2.0 V Supply Inputs for ADC.
L3	AVDD2_PLL	Input	Analog 2.0 V Supply Input for Clock PLL Linear Dropout Regulator (LDO).
D7, E7, P7, R7	BVDD2	Input	Analog 2.0 V Supply Inputs for ADC Buffer.
B11, U11	RVDD2	Input	Analog 2.0 V Supply Inputs for ADC Reference.
J5	PLLCLKVDD1	Input	Analog 1.0 V Supply Input for Clock PLL.
D2 to D4, E3, F3, N3, P3, R2 to R4	AVDD1	Input	Analog 1.0 V Supply Inputs for ADC Clock.
G7, G8, M7, M8	AVDD1_ADC	Input	Analog 1.0 V Supply Inputs for ADC.
G6, M6	CLKVDD1	Input	Analog 1.0 V Supply Inputs for ADC Clock.
D6, R6	FVDD1	Input	Analog 1.0 V Supply Inputs for ADC Reference.
D10, R10	VDD1_NVG	Input	Analog 1.0 V Supply Inputs for Negative Voltage Generator (NVG) Used to Generate −1 V Output.
E9, P9	NVG1_OUT	Output	Analog −1 V Supply Outputs from NVG. Decouple NVG1_OUT to GND with a 0.1 μF capacitor.
D8, E8, E10, P8, P10, R8	VNN1	Input	Analog −1 V Supply Inputs for ADC Buffer and Reference. Connect these pins to the adjacent, NVG1_OUT pins.
C9, T9,	BVNN2	Output	Analog −2 V Supply Outputs for ADC Buffer. Decouple each BVNN2 pin to GND with a 0.1 μF capacitor.
C10, T10	BVDD3	Output	Analog 3 V Supply Output for ADC Buffer. Decouple BVDD3 to GND with 0.1 μF capacitor.
E5, F5, N5, P5	DAVDD1	Input	Digital Analog 1.0 V Supply Inputs.
F10, H9, H11, J9, J11, K9, K11, L9, L11, M9	DVDD1	Input	Digital 1.0 V Supply Inputs.
J6, J7, K6, K7	DVDD1_RT	Input	Digital 1.0 Supply Inputs for Retimer Block.
K5	DCLKVDD1	Input	Digital 1.0 V Clock Generation Supply.
A16, B16, C16, D16, E16, F16, G16, H16, M16, N16, P16, R16, T16, U16, V16	SVDD1	Input	Digital 1.0 V Supply Inputs for SERDES Deserializer and Serializer.
K15	SVDD2_PLL	Input	Digital 2.0 V Supply Input for SERDES LDO.
J16, K16	SVDD1_PLL	Input	Digital 1.0 V Supply Inputs for SERDES Clock Generation and PLL.
C13, F9, T13	DVDD1P8	Input	Digital Interface and Temperature Monitoring Unit (TMU) Supply Inputs (Nominal 1.8 V).
A1, A3, A4, A7, A8, A11, A17, A18, B2 to B6, B9, B10, B14, B15, C2, C5 to C8, C11, C17, C18, D1, D5, D9, D14, D15, E1, E4, E6, E17, E18, F2, F4, F6 to F8, F14, F15, G2 to G5, G17, G18, H1, H5 to H8, H10, H12, H14, H15, J2, J8, J10, J12, J14, J15, J17, J18, K2, K8, K10, K12, K14, K17, K18, L1, L5 to L8, L10, L12, L14, M2 to M5, M10, M17, M18, N2, N4, N6 to N8, N14, N15, P1, P4, P6, P17, P18, R1, R5, R9, R14, R15, T2, T5 to T8, T11, T17, T18, U2 to U6, U9, U10, U14, U15, V1, V3, V4, V7, V8, V11, V17, V18	GND	Input/ output	Ground References.
ANALOG OUTPUTS			
H3	ISET	Output	Bias Current Setting Pin. Connect this pin with a 5 kΩ resistor to GND.
C4, C3	ADCDRVP, ADCDRVN	Output	ADC Clock Output Options. These pins are disabled by default.
B8, U8	VCM0, VCM1	Output	ADC Buffer Common-Mode Output Voltage. Decouple this pin to GND with a 0.1 μF capacitor.
K3	VCO_VREG	Output	PLL LDO Regulator Output. Decouple this pin to GND with a 2.2 μF capacitor.
G9	TMU_REFN	Output	TMU ADC Negative Reference. Connect this pin to GND.
G10	TMU_REFP	Output	TMU ADC Positive Reference. Connect this pin to DVDD1P8.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 15. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ANALOG INPUTS			
A10, A9	ADC0P, ADC0N	Input	ADC0 Differential Inputs with Internal 100 Ω Differential Resistor.
V10, V9	ADC1P, ADC1N	Input	ADC1 Differential Inputs with Internal 100 Ω Differential Resistor.
J3	VCO_FINE	Input	On-Chip Clock Multiplier and PLL Fine Loop Filter Input.
J4	VCO_COARSE	Input	On-Chip DAC Clock Multiplier and PLL Coarse Loop Filter Input.
K4	VCO_VCM	Input	On-Chip Clock Multiplier and VCO Common-Mode Input.
N9, N10	TDP, TDN	Input	Anode and Cathode of Temperature Diodes. This feature is not supported. Tie TDP and TDN to GND.
J1, K1	CLKINP, CLKINN	Input	Differential Clock Inputs with Nominal 100 Ω Termination. Self bias input requiring ac coupling. When the on-chip clock multiplier PLL is enabled, this input is the reference clock input. If the PLL is disabled, an RF clock equal to the DAC output sample rate is required.
CMOS INPUTS AND OUTPUTS[1]			
G13	CSB	Input	Serial Port Enable Input. Active low.
H13	SCLK	Input	Serial Plot Clock Input.
F13	SDIO	Input/ output	Serial Port Bidirectional Data Input/Output.
J13	SDO	Output	Serial Port Data Output.
C12	RESETB	Input	Active Low Reset Input. RESETB places digital logic and SPI registers in a known default state. RESETB must be connected to a digital IC that is capable of issuing a reset signal for the first step in the device initialization process.
E13, D13	RXEN0, RXEN1	Input	Active High ADC and Receive Datapath Enable Inputs. RXENx is also SPI configurable.
D12, D11	ADC0_SMON0, ADC0_SMON1	Output	ADC0 Signal Monitoring Outputs by Default. Do not connect if unused.
F12, F11	ADC1_SMON0, ADC1_SMON1	Output	ADC1 Signal Monitoring Outputs by Default. Do not connect if unused.
E12, E11	ADC0_FD0, ADC0_FD1	Output	ADC0 Fast Detect Outputs by Default. Do not connect if unused.
G12, G11	ADC1_FD0, ADC1_FD1	Output	ADC1 Fast Detect Outputs by Default. Do not connect if unused.
P12, R12	IRQB_0, IRQB_1	Outputs	Interrupt Request 0 and Interrupt Request 1 Outputs. These pins are an open-drain, active low output (CMOS levels with respect to DVDD1P8). Connect a 10 kΩ pull-up resistor to DVDD1P8 to prevent these pins from floating when unused.
K13, L13, M13, N13, T12	GPIO6 to GPIO10	Input/ output	General-Purpose Input or Output Pins. These pins control auxiliary functions related to the Rx datapaths and ADCs.
JESD204B or JESD204C COMPATIBLE SERDES DATA LANES AND CONTROL SIGNALS[2]			
A15, A14	SERDOUT0+, SERDOUT0−	Output	JTx Lane 0 Outputs, Data True/Complement.
C15, C14	SERDOUT1+, SERDOUT1−	Output	JTx Lane 1 Outputs, Data True/Complement.
E15, E14	SERDOUT2+, SERDOUT2−	Output	JTx Lane 2 Outputs, Data True/Complement.
G15, G14	SERDOUT3+, SERDOUT3−	Output	JTx Lane 3 Outputs, Data True/Complement.
H18, H17	SERDOUT4+, SERDOUT4−	Output	JTx Lane 4 Outputs, Data True/Complement.
F18, F17	SERDOUT5+, SERDOUT5−	Output	JTx Lane 5 Outputs, Data True/Complement.
D18, D17	SERDOUT6+, SERDOUT6−	Output	JTx Lane 6 Outputs, Data True/Complement.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 15. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
B18, B17	SERDOUT7+, SERDOUT7−	Output	JTx Lane 7 Outputs, Data True/Complement.
B13, A13	SYNC0INB+, SYNC0INB−	Input	JTx Link 0 Synchronization Inputs for JESD204B Interface. These pins are LVDS or CMOS configurable. These pins are LVDS or CMOS configurable and have selectable internal 100 Ω input impedance for LVDS operation
B12, A12	SYNC1INB+, SYNC1INB−	Input	JTx Link 1 Synchronization Inputs for JESD204B Interface or CMOS Inputs for Receive FFH via GPIOx Pins. These pins are LVDS or CMOS configurable and have selectable internal 100 Ω input impedance for LVDS operation.
T4, T3	SYSREFP, SYSREFN	Input	Active High JESD204 System Reference Inputs. These pins are configurable for differential current mode logic (CML), PECL, and LVDS with internal 100 Ω termination or single-ended CMOS.
NO CONNECTS AND DO NOT CONNECTS			
A5, A6, V5, V6	NC		No Connect. These pins can be left open or connected.
B1, B7, C1, F1, G1, H4, L4, L15 to L18, M1, M11, M12, M14, M15, N1, N11, N12, N17, N18, P11, P13 to P15, R11, R13, R17, R18, T1, T14, T15, U1, U7, U12, U13, U17, U18, V12 to V15	DNC	DNC	Do Not Connect. The pins must be kept open.

[1] CMOS inputs do not have pull-up or pull-down resistors.

[2] SERDOUTx± include 100 Ω internal termination resistors.

TYPICAL PERFORMANCE CHARACTERISTICS

ADC

Nominal supplies, sampling rate = 6 GSPS with DAC clock frequency (f_{CLK}) = 12 GHz direct RF clock, full bandwidth mode operation (no decimation), T_J = 80°C (T_A = 25°C), 128k FFT sample with five averages, and A_{IN} = −1 dBFS, unless otherwise noted.

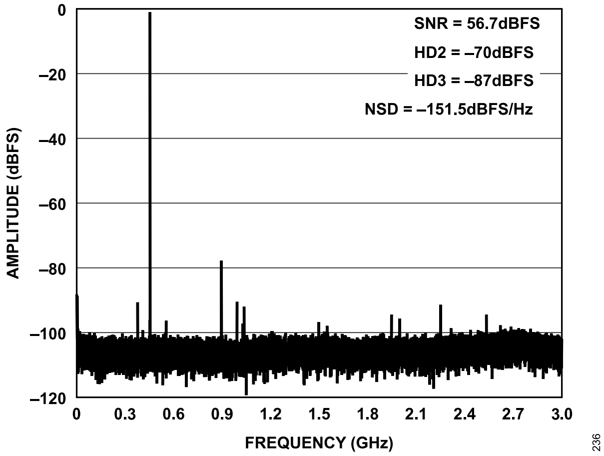


Figure 5. Single-Tone FFT at f_{IN} = 450 MHz

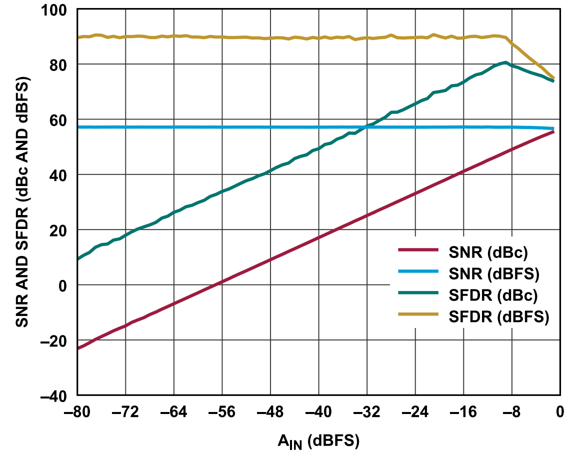


Figure 8. Single-Tone SNR and SFDR vs. A_{IN} at f_{IN} = 450 MHz

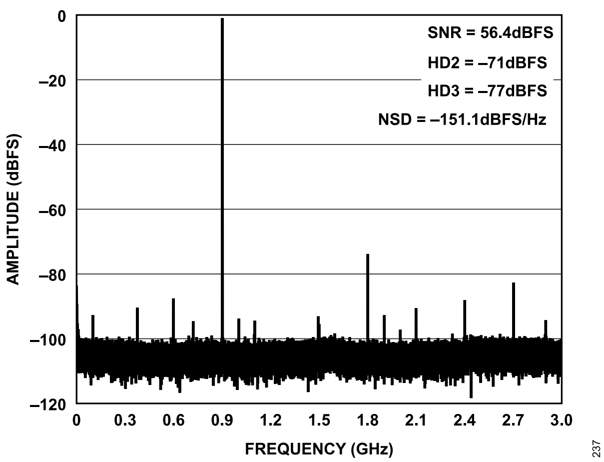


Figure 6. Single-Tone FFT at f_{IN} = 900 MHz

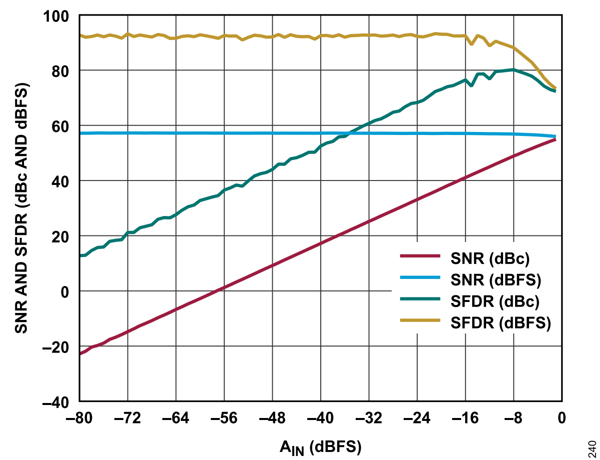


Figure 9. Single-Tone SNR and SFDR vs. A_{IN} at f_{IN} = 900 MHz

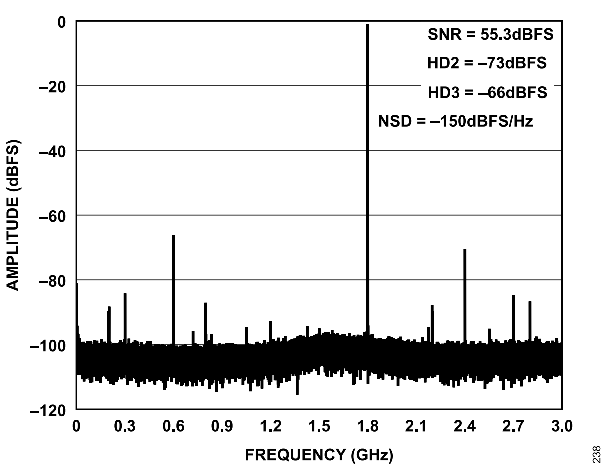


Figure 7. Single-Tone FFT at f_{IN} = 1.8 GHz

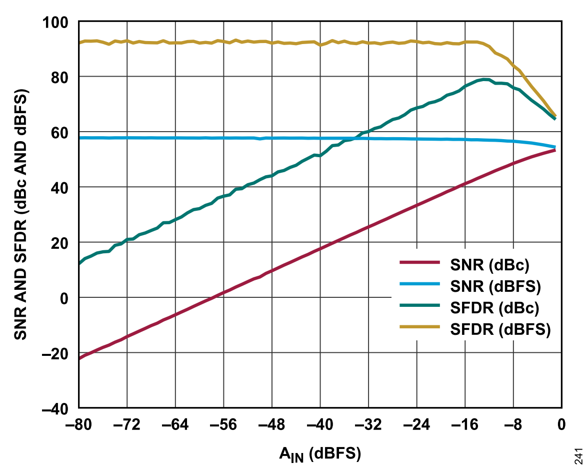


Figure 10. Single-Tone SNR and SFDR vs. A_{IN} at f_{IN} = 1.8 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

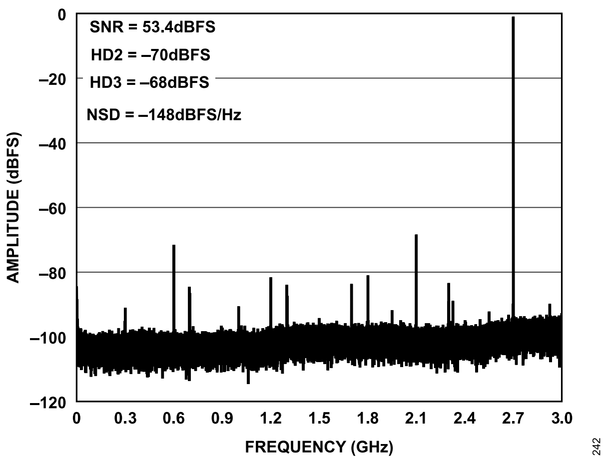


Figure 11. Single-Tone FFT at f_{IN} = 2.7 GHz

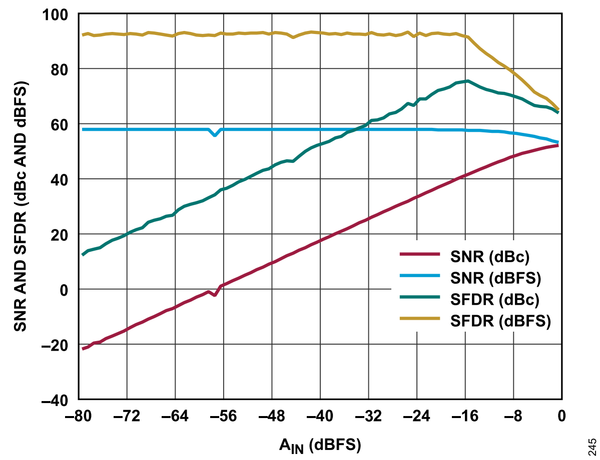


Figure 14. Single-Tone SNR and SFDR vs. A_{IN} at f_{IN} = 2.7 GHz

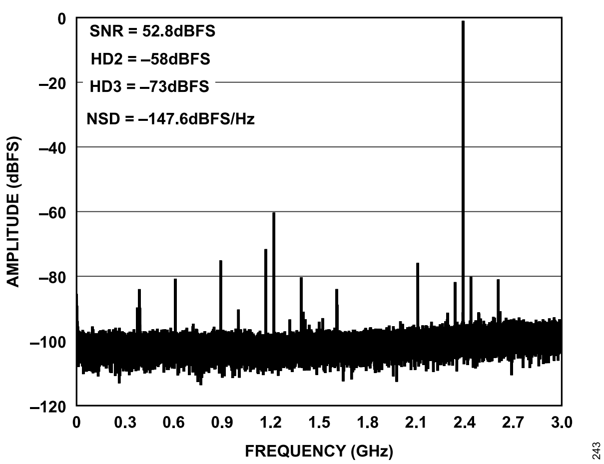


Figure 12. Single-Tone FFT at f_{IN} = 3.6 GHz

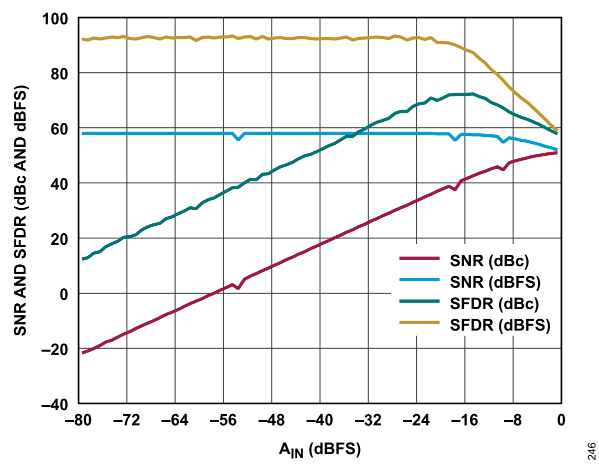


Figure 15. Single-Tone SNR and SFDR vs. A_{IN} at f_{IN} = 3.6 GHz

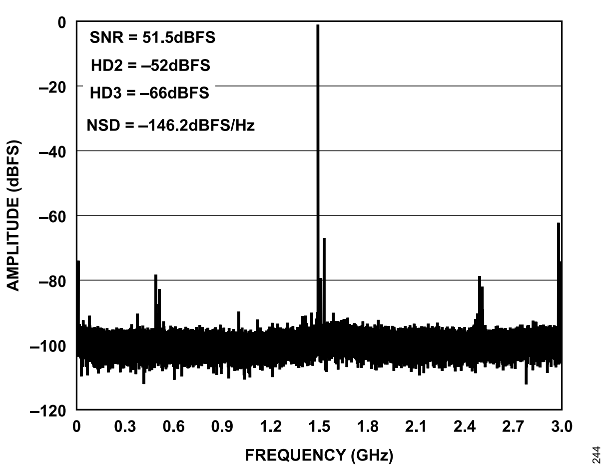


Figure 13. Single-Tone FFT at f_{IN} = 4.5 GHz

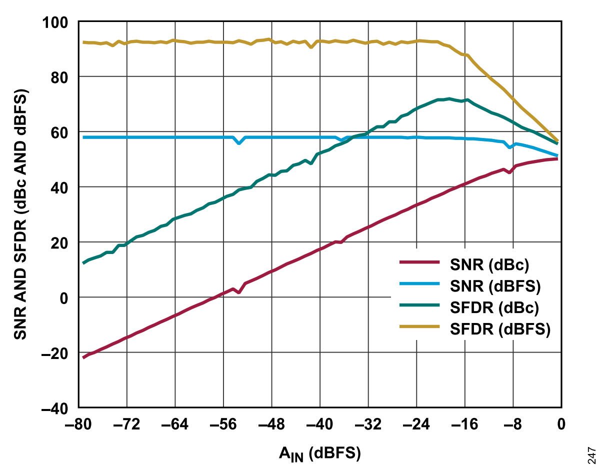


Figure 16. Single-Tone SNR and SFDR vs. A_{IN} at f_{IN} = 4.5 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

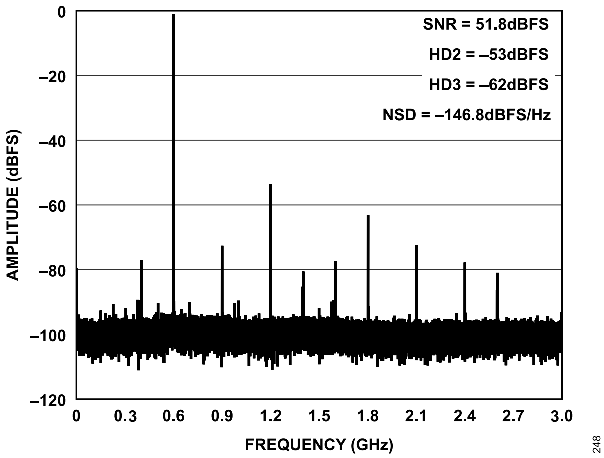


Figure 17. Single-Tone FFT at f_{IN} = 5.4 GHz

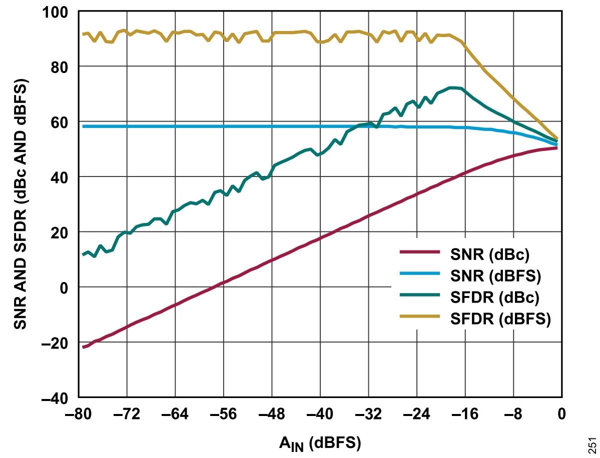


Figure 20. Single-Tone SNR and SFDR vs. A_{IN} at f_{IN} = 5.4 GHz

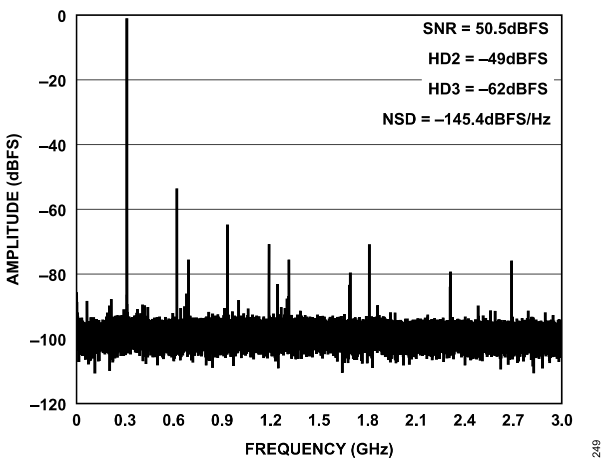


Figure 18. Single-Tone FFT at f_{IN} = 6.3 GHz

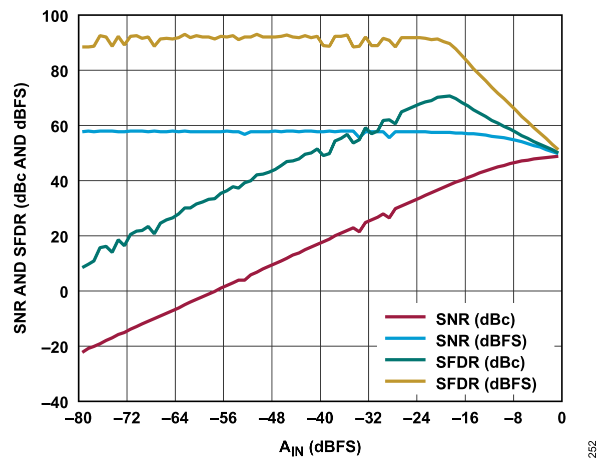


Figure 21. Single-Tone SNR and SFDR vs. A_{IN} at f_{IN} = 6.3 GHz

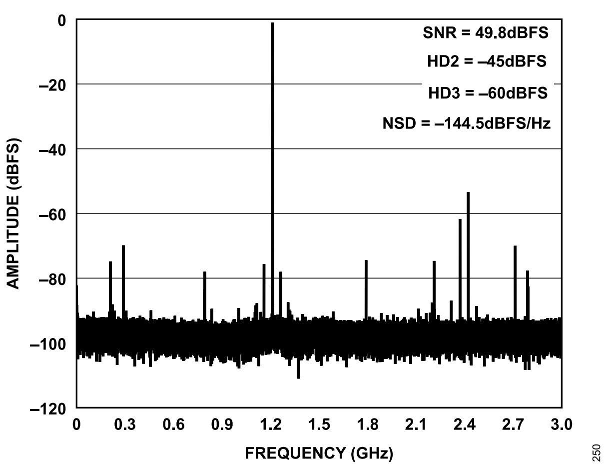


Figure 19. Single-Tone FFT at f_{IN} = 7.2 GHz

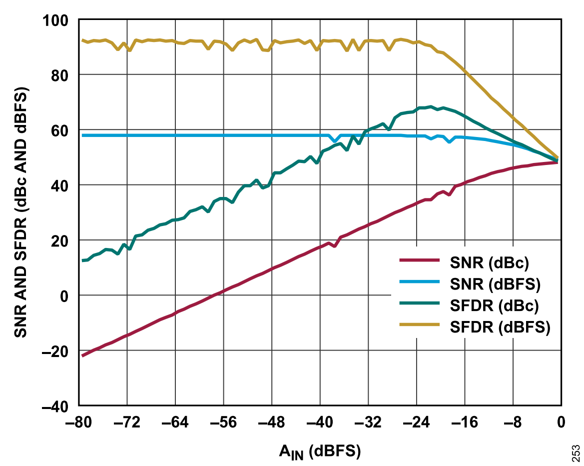


Figure 22. Single-Tone SNR and SFDR vs. A_{IN} at f_{IN} = 7.2 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

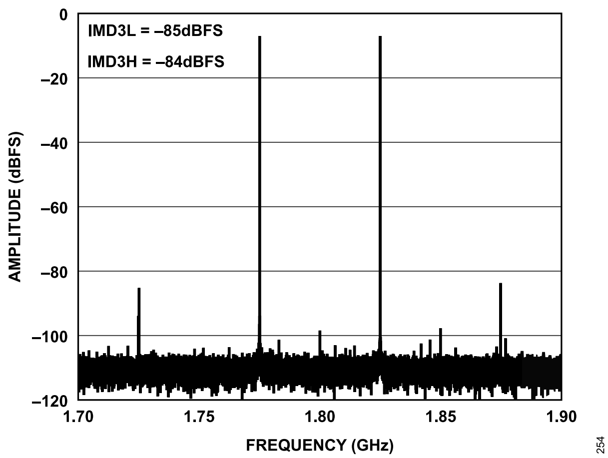


Figure 23. Two-Tone FFT, f_{IN1} = 1.775 GHz, f_{IN2} = 1.825 GHz, and A_{IN1} and A_{IN2} = −7 dBFS (Note That IMD3L and IMD3H Are the Lower and Higher IMD3 Product Components in dBFS)

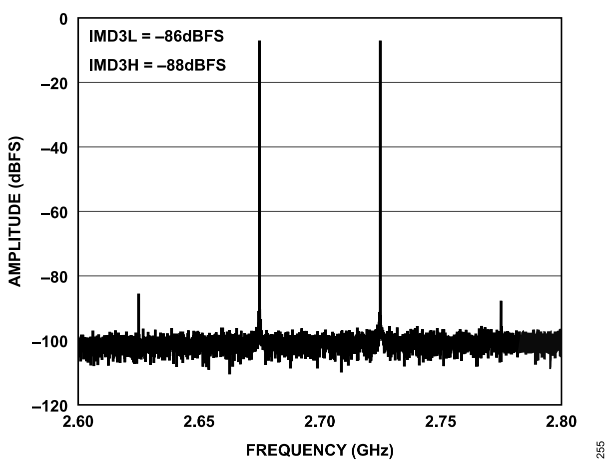


Figure 24. Two-Tone FFT, f_{IN1} = 2.675 GHz, f_{IN2} = 2.725 GHz, and A_{IN1} and A_{IN2} = −7 dBFS

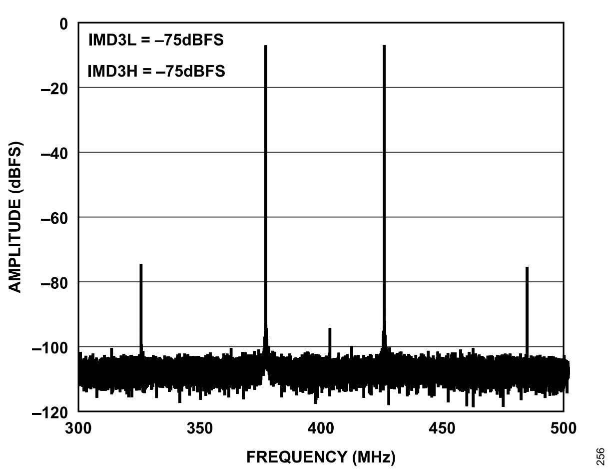


Figure 25. Two-Tone FFT, f_{IN1} = 3.575 GHz, f_{IN2} = 3.625 GHz, and A_{IN1} and A_{IN2} = −7 dBFS

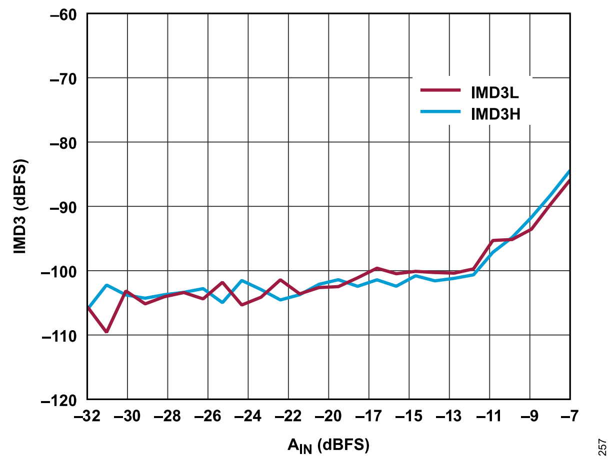


Figure 26. Two-Tone IMD3 vs. A_{IN} with f_{IN1} = 1.775 GHz, f_{IN2} = 1.825 GHz

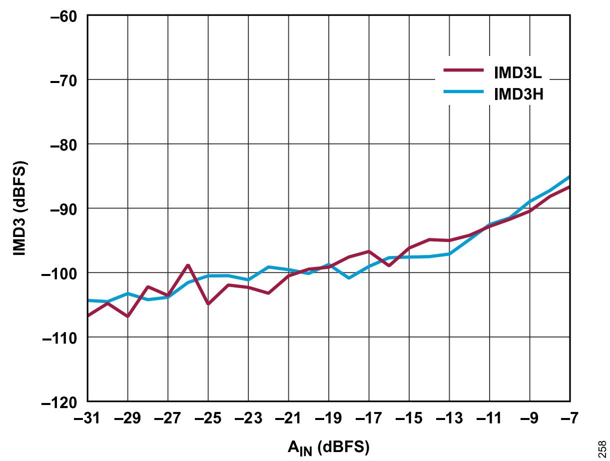


Figure 27. Two-Tone IMD3 vs. A_{IN} with f_{IN1} = 2.675 GHz and f_{IN2} = 2.725 GHz

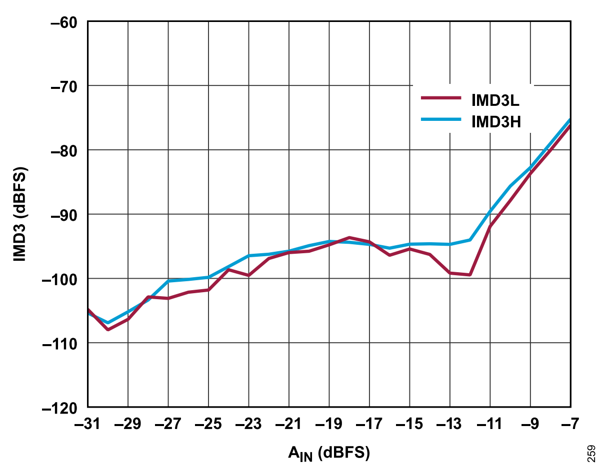


Figure 28. Two-Tone IMD3 vs. A_{IN} with f_{IN1} = 3.575 GHz and f_{IN2} = 3.625 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

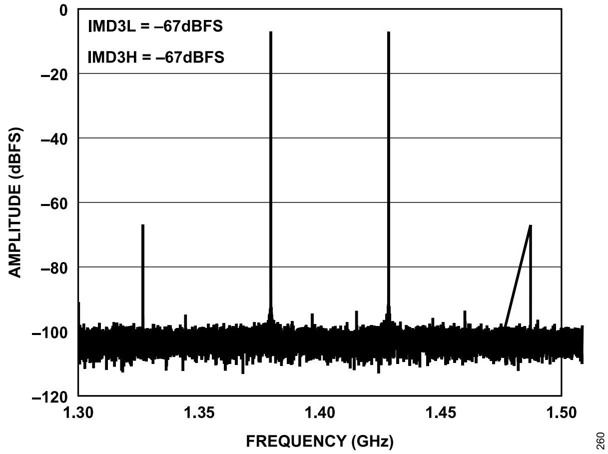


Figure 29. Two-Tone FFT, f_{IN1} = 5.375 GHz, f_{IN2} = 5.425 GHz, and A_{IN1} and A_{IN2} = −7 dBFS

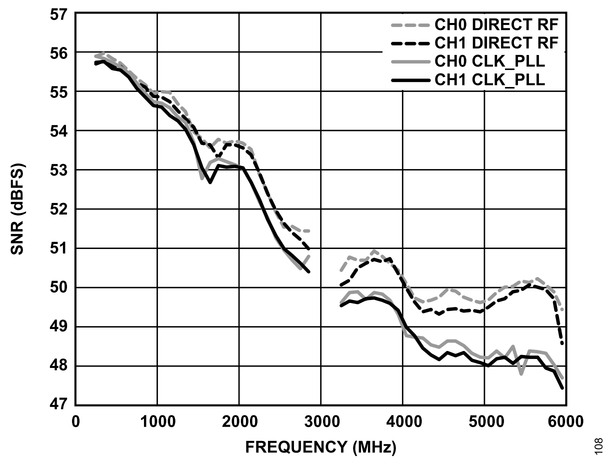


Figure 30. SNR vs. Frequency with A_{IN} =−1 dBFS Between Direct External RF Clock = 6 GHz and PLL Clock (CLK_PLL) Multiplier Enabled with Reference Input of 125 MHz

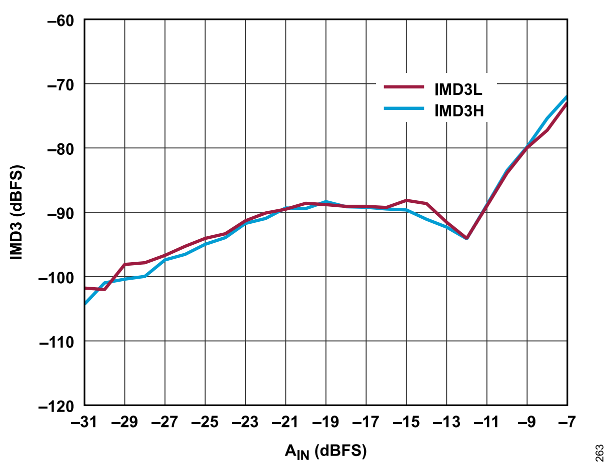


Figure 31. Two-Tone IMD3 vs. A_{IN} with f_{IN1} = 5.375 GHz and f_{IN2} = 5.425 GHz

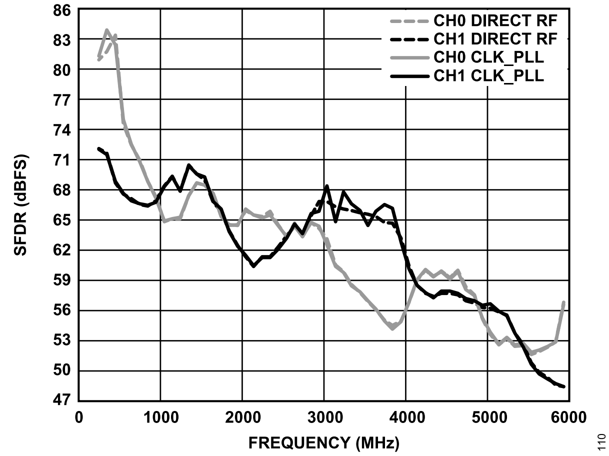


Figure 32. SFDR vs. Frequency with A_{IN} = −1 dBFS Between Direct External RF Clock = 6 GHz and PLL Clock (CLK_PLL) Multiplier Enabled with Reference Input of 125 MHz

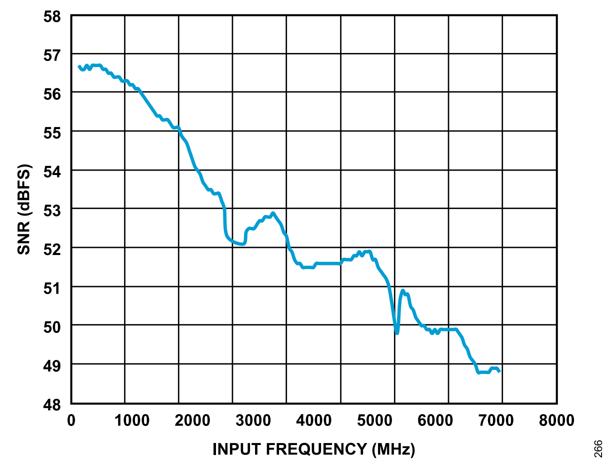


Figure 33. SNR vs. Input Frequency with A_{IN} = −1 dBFS

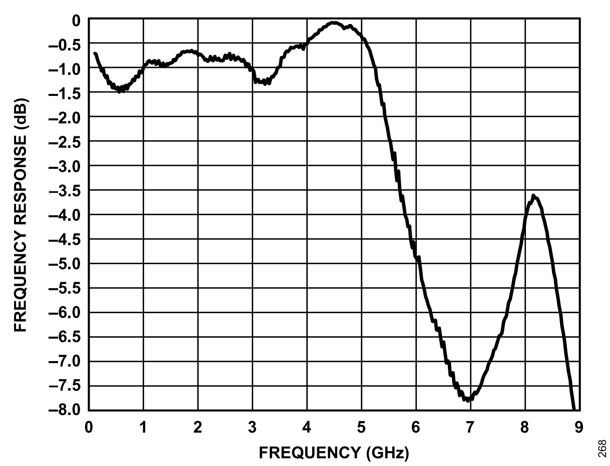


Figure 34. Measured ADC Input Bandwidth on the AD9082-FMCA-EBZ (No Matching Network)

TYPICAL PERFORMANCE CHARACTERISTICS

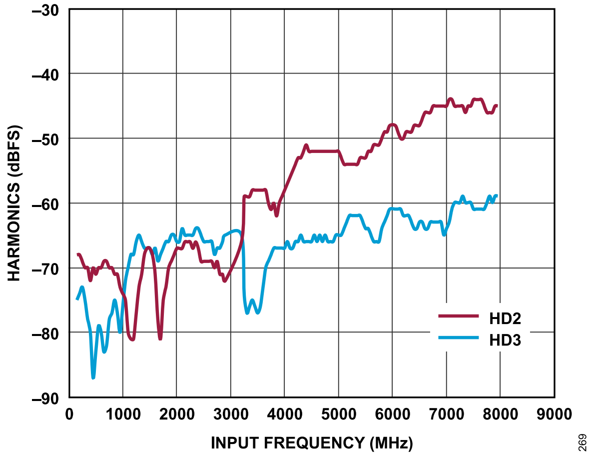


Figure 35. Harmonics (HD2 and HD3) vs. Input Frequency with A_{IN} = −1 dBFS

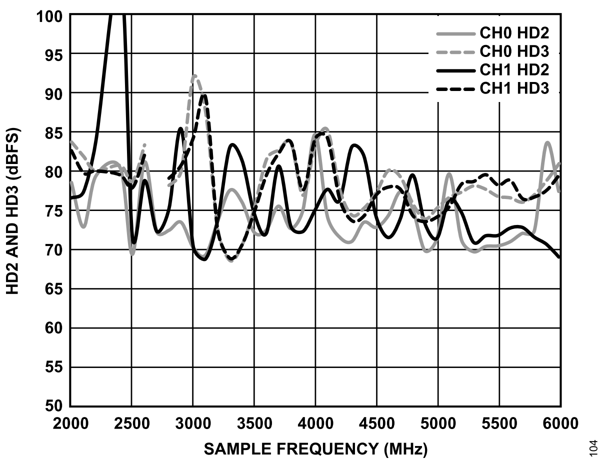


Figure 36. HD2 and HD3 vs. Sample Frequency (f_S), f_{IN} = 450 MHz, A_{IN} = −1 dBFS, f_S = 2 GSPS to 6 GSPS

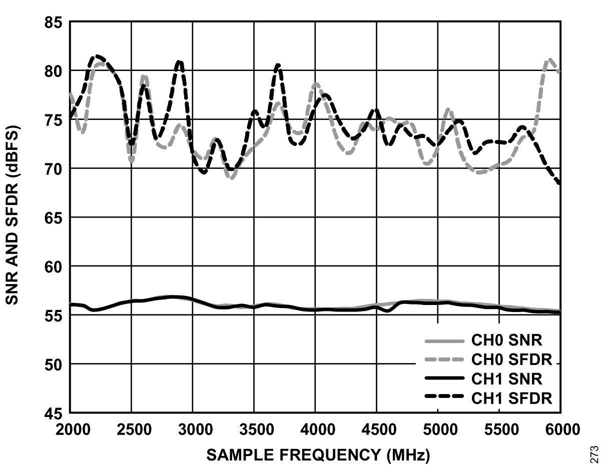


Figure 37. SNR and SFDR vs. Sample Frequency, f_{IN} = 450 MHz, A_{IN} = −1 dBFS, f_S = 2 GSPS to 6 GSPS

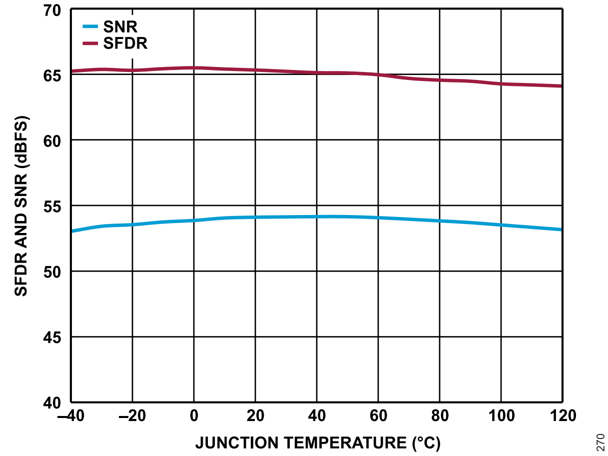


Figure 38. SFDR and SNR vs. Junction Temperature, f_{IN}= 1.8 GHz, A_{IN} = −1 dBFS

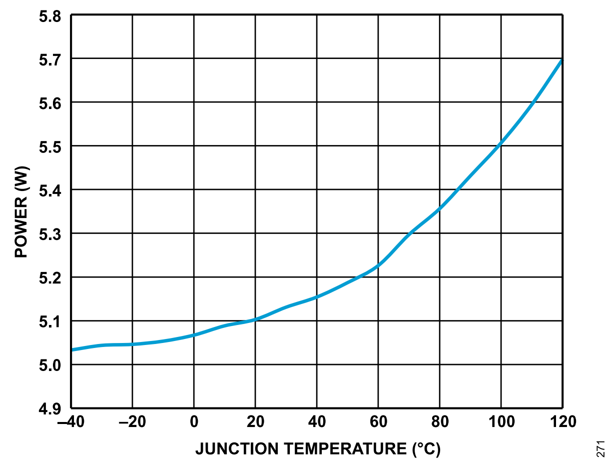


Figure 39. Power vs. Junction Temperature, f_{IN}= 1.8 GHz, A_{IN} = −1 dBFS

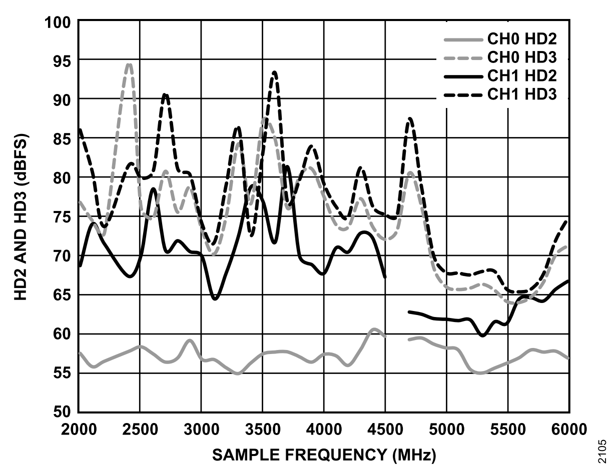


Figure 40. HD2 and HD3 vs. Sample Frequency, f_{IN} = 3450 MHz, A_{IN} = −1 dBFS, f_S = 2 GSPS to 6 GSPS

TYPICAL PERFORMANCE CHARACTERISTICS

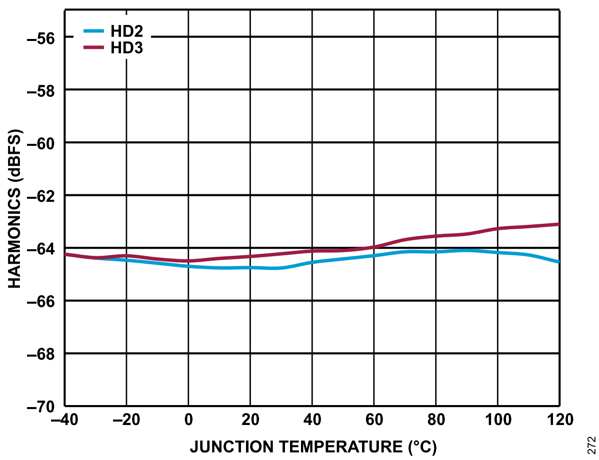


Figure 41. Harmonics vs. Junction Temperature, f_{IN}= 1.8 GHz, A_{IN} = −1 dBFS

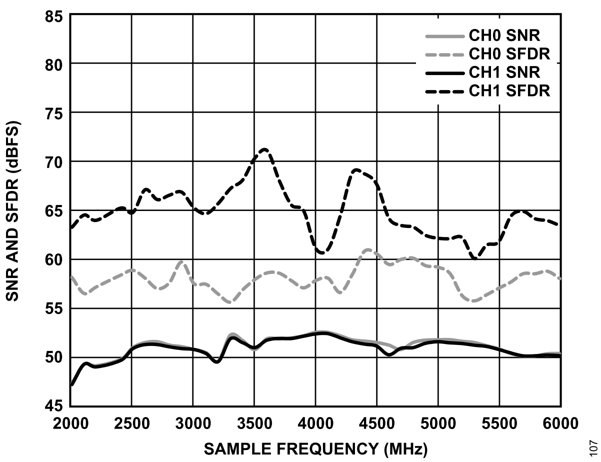


Figure 42. SNR and SFDR vs. Sample Frequency, f_{IN} = 3450 MHz, A_{IN} = −1 dBFS, f_S = 2 GSPS to 6 GSPS

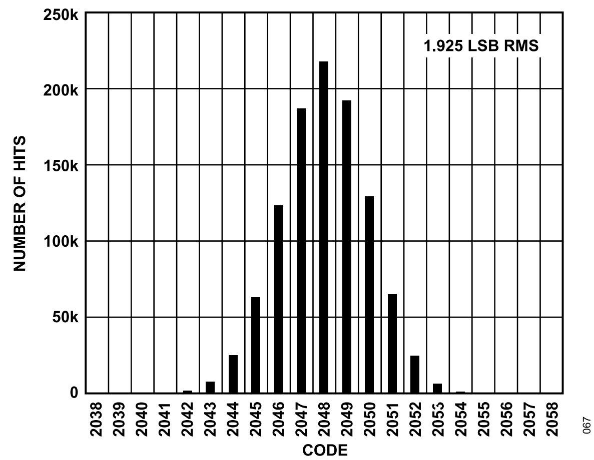


Figure 43. Input Referred Noise Histogram

THEORY OF OPERATION

The AD9207 is a highly integrated, 28 nm, RF, 2-channel, 12-bit, 6 GSPS ADC (see the Functional Block Diagram section). To enable wide bandwidth operation, a high linearity, 100 Ω differential buffer with overload protection is used to isolate the ADC core from the RF ADC driver source. An on-chip clock multiplier can be used to synthesize the RF DAC and ADC clocks or an external clock can be applied.

Flexible receive DSP paths are available to downsample the desired intermediate frequency (IF) or RF signal(s) to lower the required interface rates and efficiently align with bandwidth requirements. The channelizer datapath enables efficient data transfer to allow multiband applications where up to eight unique RF bands are supported. The receive DSP paths are symmetric and consist of four coarse DDC blocks in the main datapath along with eight fine DDC blocks in the channelizer datapath. Each DDC block includes multiple decimation stages and a 48-bit NCO that is configurable for integer mode or fractional mode of operation. The NCO in each block supports FFH and can be controlled using the GPIOx pins. The DDC blocks and the datapaths are fully bypassable to enable Nyquist operation.

Various auxiliary DSP features facilitate an improved system integration. The datapaths include adjustable delay lines to compensate for mismatch in channel delay paths that can occur external to the device. The receive datapath includes a flexible programmable 192-tap PFIR filter. This filter can be allocated across one or more ADCs for receive equalization with support for four different profiles. Profiles can be selected using the GPIOx pins. The receive datapath also includes a fast and slow signal detection capability in support of the AGC. The datapaths also include features to reduce power consumption in time division duplex (TDD) applications. In addition, all auxiliary DSP features are fully bypassable.

The data formatting of the datapaths can be real or complex (I/Q) with selectable resolutions of 8, 12, 16, and 24 bits depending on the JESD204B or the JESD204C mode.

An 8-lane JESD204 transmitter port is available to support the high data throughput rates on the receive datapaths. The transmit port supports JESD204C up to 24.75 Gbps lane rates or JESD204B up to 15.5 Gbps lane rates. The JESD204 data link layer is highly flexible to allow lane count (or rate) adjustment required to support a target link throughput. An external alignment signal (SYSREF) can be used to guarantee deterministic latency and phase alignment and to aid in multichip synchronization.

An on-chip TMU can be used to measure and read out the die temperature (via the SPI port), to guarantee better thermal stability during system operation.

OUTLINE DIMENSIONS

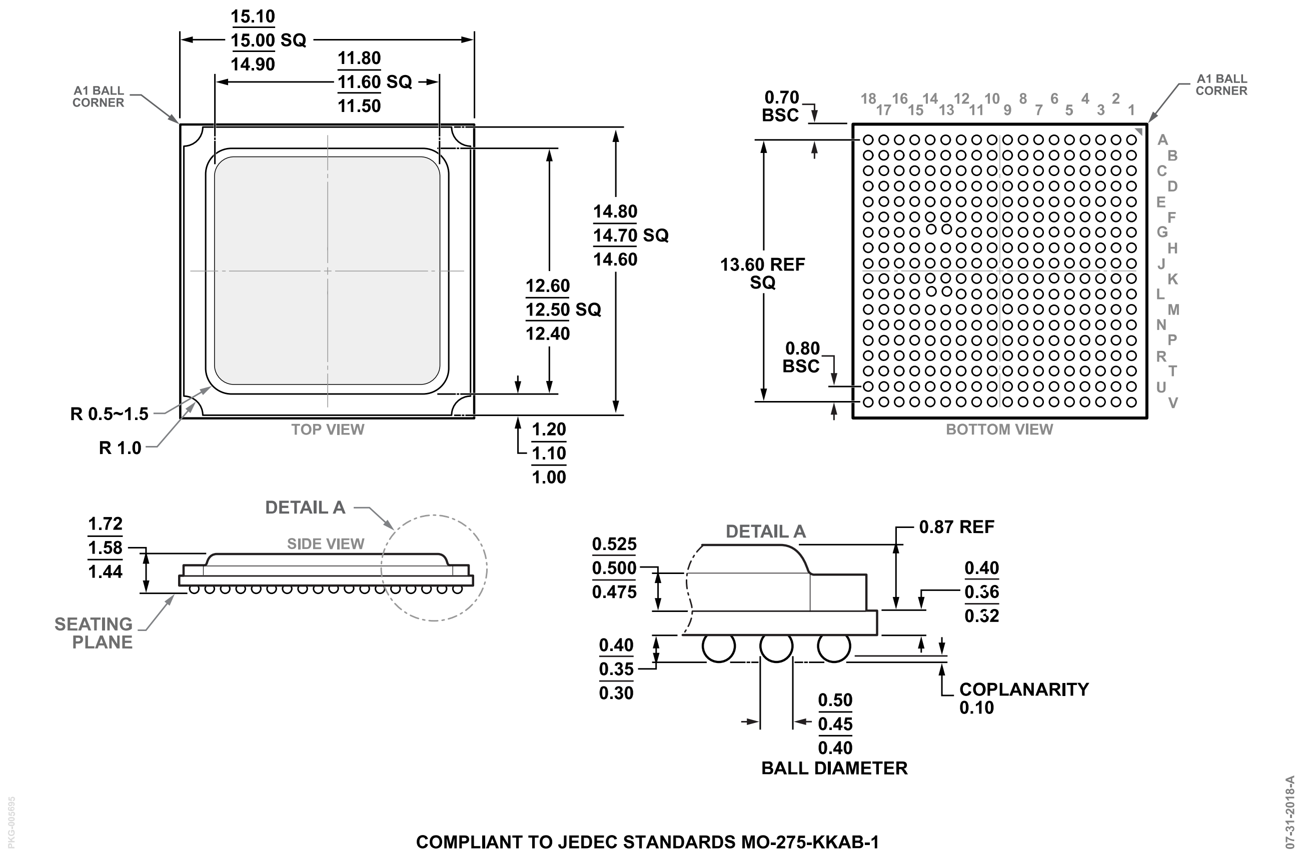


Figure 44. 324-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-324-3)
Dimensions Shown in Millimeters

Updated: September 14, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD9207BBPZ-6G	–40°C to +120°C	324-Ball BGA_ED (15 mm × 15 mm × 1.58 mm)	Tray, 126	BP-324-3
AD9207BBPZRL-6G	–40°C to +120°C	324-Ball BGA_ED (15 mm × 15 mm × 1.58 mm)	Reel, 1000	BP-324-3

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model	Description
AD9082-FMCA-EBZ[1]	AD9207 Evaluation Board with High Performance Analog Network

[1] The AD9082-FMCA-EBZ is used to evaluate the AD9207.

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